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Quantum Dot Channel Field-Effect Transistors and Non-Volatile Memories: Fabrication and Simulation

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Quantum dot channel (QDC) and Quantum dot gate (QDG) field effect transistors (FETs) have been fabricated on crystalline Si and poly Si thin films using cladded Si and Ge quantum dots. In particular, this thesis presents modeling and fabrication of quantum dot channel field effect transistors (QDC-FETs) using cladded Ge quantum dots on poly-Si thin films grown on silicon-on-insulator (SOI) substrates. $HfAlO_2$ high-k dielectric layers are used for the gate dielectric. QDC-FETs exhibit multi-state I-V characteristics which enable 2-bit processing, and reduce FET count and power dissipation, and are expected to make a significant impact on the digital circuit design. Germanium quantum dot QDC-FETs provide higher electron mobility than conventional polysilicon FETs, which is comparable to crystalline silicon.

Quantum dot channel FETs are also configured as floating gate quantum dot nonvolatile memories (QDC-QDNVMs). In NVMs, we use floating gate comprising of GeO_x-Ge quantum dots. QD nonvolatile memories (QD-NVMs) are fabricated on crystalline silicon substrates. $HfAlO_2$ high-k insulator layers are used for both tunnel gate oxide as well as control gate dielectric. QDC-NVMs not only provide significantly

higher drain current I_D, but also higher threshold voltage shifts (ΔV_{TH}), and exhibit potential for fabricating multi-bit nonvolatile memories.

Quantum Dot Channel Field-Effect Transistors and Non-Volatile Memories: Fabrication and Simulation

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APROVAL PAGE

Doctor of Philosophy Dissertation

Quantum Dot Channel Field-Effect Transistors and Non-Volatile Memories: Fabrication and Simulation

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CHAPTER 1

INTRODUCTION

1.1. Background of Metal-Oxide-Semiconductor Field-Effect Transistor

Germanium quantum dot QDC-FETs provide higher electron mobility than conventional polysilicon FETs, which is comparable to crystalline silicon.

1.1.1. Overview

The 2011 International Technology Roadmap for Semiconductors (ITRS) shows the MOS-FET scaling process technologies from 2011 to 2021 in Figure 1.1. The first row shows gate-stack materials using high-k dielectrics layer. The second row shows the methods used to improve electron mobility. These methods deal with the stress layer that causes tensile strain in Si, use of high mobility channel such as Ge and InGaAs. The third row shows a wrap-around gate fabricated on bulk Si wafer or silicon-on-insulator (SOI) wafer to improve the gate control. The fourth row shows the evolution of the wraparound gate using the silicon-on-insulator (SOI) in partially depleted (PD) and fully depleted (FD) configurations.

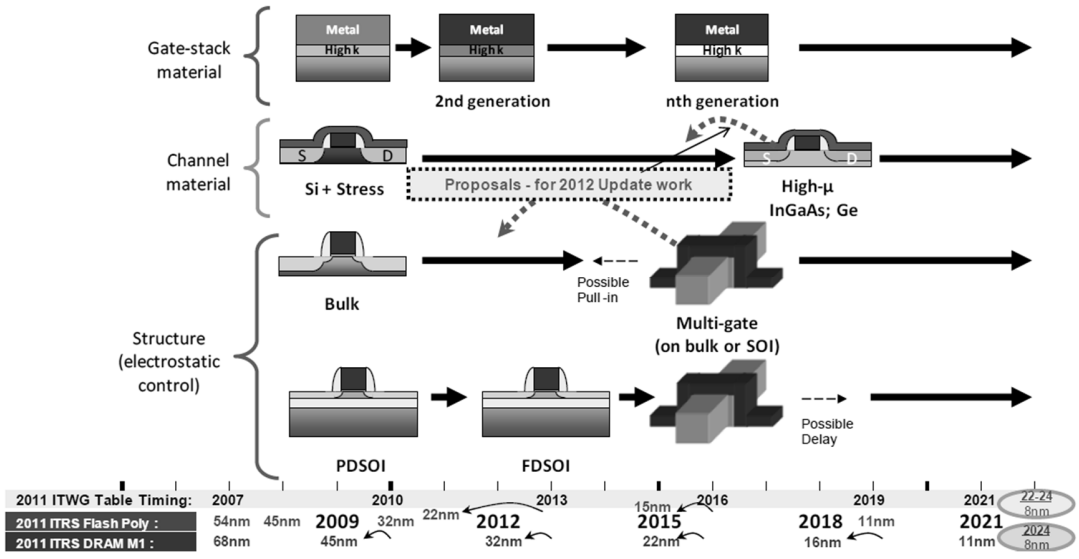

Figure 1.1. 2011 The International Technology Roadmap for Semiconductors (ITRS) [1

1.1.2. High-k Dielectric Insulator

The high-k dielectric materials include tantalum oxide (Ta_2O_3), aluminum oxide (Al_2O_3), titanium oxide (TiO_2), hafnium oxide (HfO_2), and zirconium oxide (ZrO_2) for the gate dielectric [3]. Among them, Al_2O_3 and HfO_2 have the dielectric constants of 9 and 25 [4], and the band gaps of 8.8 and 5.8 [4]. Because Al_2O_3 and HfO_2 provide these complementary characteristics, they are combined to produce hafnium aluminum oxide ($HfAlO_2$) which has a relatively large dielectric constant [5]. The MOS devices presented in this thesis use $HfAlO_2$ nanolaminate as high-k dielectric combinational layers for the gate dielectric of the QDC FETs, and the gate dielectric and the control dielectric of the QDC NVMs.

1.1.3. Wraparound Gate Insulator for QDC FETs

Quantum dot channel (QDC) field-effect transistors (FETs) with II-VI wraparound gate insulators are presented Figure 1.2 [2]. There are II-VI lattice-matched layers which serve as gate insulators to reduce the density of interface states [2]. Figure 1.2a shows the wraparound ~9nm QDC FET structure in the FinFET configuration. This device has three layers of GeO_x-cladded Ge quantum dots for the transport channel [2]. Here, ZnS-ZnMgS serves as a bottom barrier layer, ZnMgSSe serves as a top insulator layer, and ZnSSe serves as a side insulator layer [2]. Figure 1.2b shows the cross sectional view at the center line of Figure 1.2a [2], and a metal layer covers top and side insulator layers [2]. Figure 1.2c shows another QDC FET which has three layers of SiOx-cladded Si quantum dots for the transport channel [2]. The quantum dots are self-assembled on a ZnMgS layer which is lattice-matched to the p-silicon substrate [2]. HfO_2 forms the wraparound gate dielectric, and serves as top and side insulator layers, and ZnMgS serves as a bottom insulator layer [2]. The use of such a wraparound lattice-

matched epitaxial ZnMgSSe gate insulator layer in place of HfO_2 potentially reduces the interfacial trapped charge density and the threshold variability ΔV_{TH} to improve the noise margins of logic gates [2].

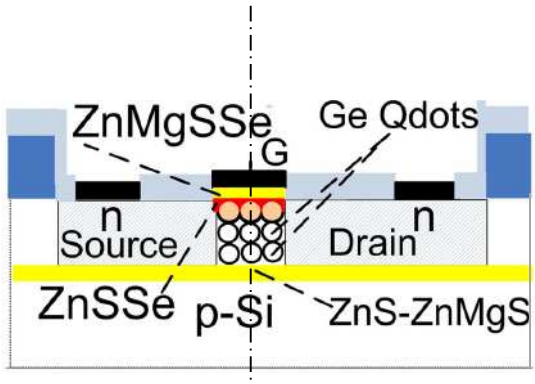

Figure 1.2a. Ge QDC FET with II-VI Wraparound Gate Insulator

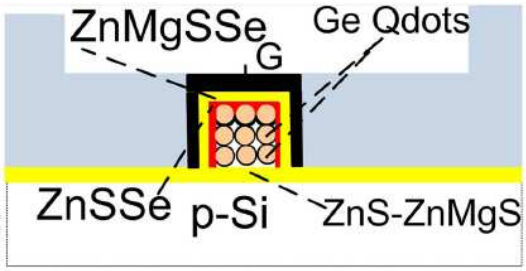

Figure 1.2b. Cross Sectional View of Ge QDC FET with II-VI Wraparound Gate Insulator

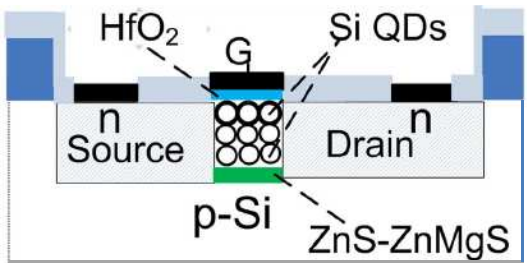

Figure 1.2c. Cross Sectional View of Si QDC FET with II-VI Wraparound Gate Insulator

1.2. Dissertation Outline

This dissertation presents the fabrication, characterization, modeling, and simulation of multi-state devices such as quantum dot channel (QDC) field effect transistors (FETs) and quantum dot channel (QDC) non-volatile memories (NVMs). Germanium QDC FETs were fabricated on poly-silicon and exhibited comparable electron mobility to silicon QDC FETs fabricated on crystal silicon. Also, silicon QDC NVM and germanium QDC NVM exhibited greater threshold shifts and potential for multi-bit operation.

Chapter 2 summarizes the fabrication and characterization procedures. The fabrication procedures include the following operations; cutting silicon wafers, silicon wafer cleaning, wet oxidation, source and drain fabrication, phosphorus diffusion, silicon nitride deposition, first gate opening, dry oxidation, second gate opening, self-assembly, opening the source and drain contacts, metallization, and interconnect. Chapter 4 also explains about four masks, a mask aligner, a high vacuum evaporator, atomic layer deposition, and a spectroscopic ellipsometer. For the characterization of FETs and NVMs, Chapter 2 explains about a high-power microscope, video camera equipment, a thin-film analyzer, a parametric analyzer, and atomic force microscopy (AFM).

Chapter 3 describes the theory and device modeling which includes energy band diagrams, various parameters, and nonvolatile memory model.

Chapter 4 presents the simulations which include the VisSim simulation and the Kronig and Penney model simulation. The VisSim simulation deals with QDG-QDC NVM, QDG-QDC FETs, and QDC FET.

Chapter 5 shows the experimental results of five devices which includes quantum dot gate quantum dot channel (QDG QDC) field effect transistor (FET), quantum dot gate quantum

dot channel (QDG QDC) nonvolatile memory (NVM) using Si quantum dots and Ge quantum dots, quantum dot channel (QDC) field effect transistor (FET), and conventional field effect transistor (FET). The structures and I_D-V_G, and I_D-V_D characteristics are explained and compared with other devices.

Chapter 6 presents the analog behavioral model (ABM) for QDC-FETs. The model has been used to simulate a quaternary inverter and a 2-bit static random access memory (SRAM).

The cross-sectional views of the FETs and the NVMs are shown from Appendix 1 to Appendix 4. The buffered oxide etch (BOE) time estimate for the gate opening is shown in Appendix 5A. The buffered oxide etch (BOE) time estimate for the contact holes is shown in Appendix 5B. Finally, the silicon wafer cleaning procedures are explained in Appendix 5C.

1.3. Summary of Fabricated QDC FETs and NVMs

A summary of QDC devices fabricated is shown below;

FET	GeO_x-Ge QDC-FET on Polysilicon	SiO_x-Si QDC-FET on Silicon	GeO_x-Ge QDC-FET on Silicon
NVM	SiO_xSi NVM on Silicon	SiO_x-Si QDC-NVM on Silicon	GeO_x-Ge QDC-NVM on Silicon

Table 1.1 Summary of QDC Devices fabricated

1.3.1. QDC Field Effect Transistors (FETs)

The published I_D-V_G characteristics of the quantum dot channel (QDC) field effect transistor (FET) is shown in Figure 1.3 [6]. The I_D current peaks are observed at the V_G voltages are equal to approximately 1.6 volts and 2.1 volts when V_D is equal to 1.5 volts. Using these two current peaks, the I_D-V_G characteristics are divided into four sections as shown in Figure 1.3, and the characteristics of this QDC FET are considered as the four state (OFF, 'I_1', 'I_2', ON). The traditional FET has the two states (OFF, ON), and two FETs are required to produce four-state characteristics. Therefore, this QDC FET dramatically reduces FET count and power dissipation. Multi-state FETs are needed in multi-valued logic (MVL) that can reduce the number of gates and transistors in digital circuits [7].

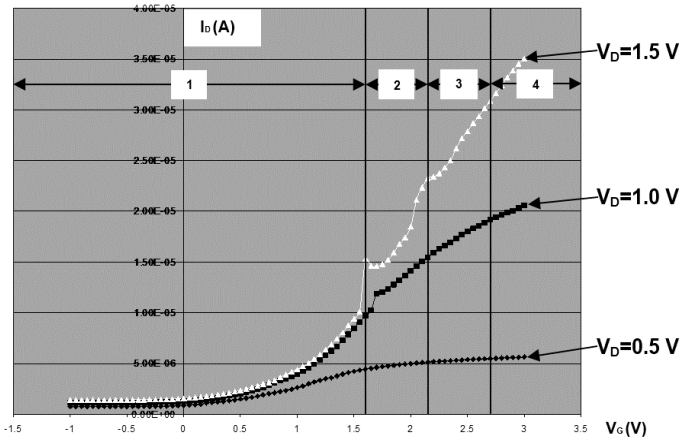

Figure 1.3. I_D-V_G Characteristics of Quantum Dot Channel (QDC) FET

The experimental I_D-V_G characteristics of silicon QDC FET fabricated on a crystal silicon substrate are shown in Figure 1.4 [8]. If the crystal silicon substrate is replaced by a poly-silicon substrate, the production cost can be dramatically reduced. But the electron mobility is also reduced. In order to compensate this disadvantage, the germanium quantum dots can be used for the transport channel of the FET. The I_D-V_G characteristics of germanium QDC FET on a poly-silicon substrate are shown in Figure 1.5. The mobility appears as the slope of the current line of the I_D-V_G characteristics, and the germanium QDC FET on a poly-silicon substrate in Figure 1.5 exhibits the mobility which is comparable to the silicon QDC FETs on a crystal silicon substrate in Figure 1.4.

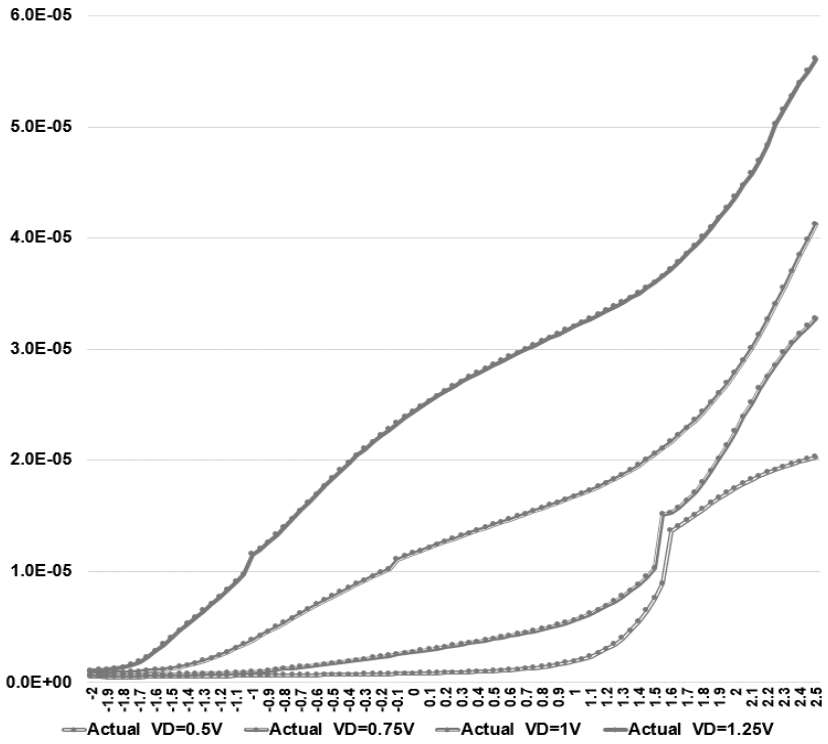

Figure 1.4. I_D-V_G Characteristics of Si QDC FET on Cristal Silicon Substrate

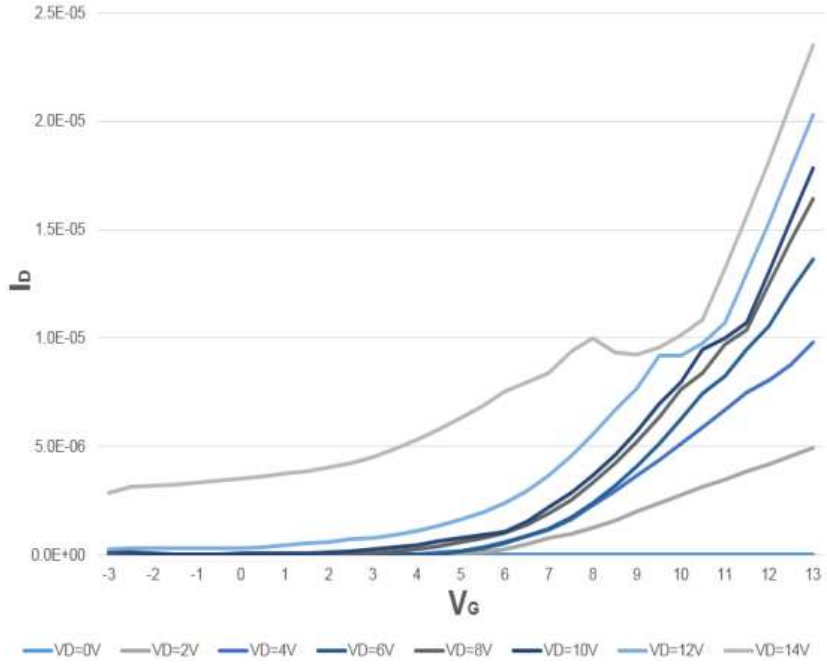

Figure 1.5. I_D-V_G Characteristics of Ge QDC FET on Poly-silicon Substrate

1.3.2. QDC Nonvolatile Memories (NVMs)

The measured I_D-V_G characteristics of the germanium quantum dot floating gate nonvolatile memory [NVM] on a crystal silicon substrate are shown in Figure 1.6 [9]. The drain pulse of 4V, duration of 400µs and the gate pulse of 15V, duration of 100µs were applied simultaneously. In Figure 1.6, the labels B4, B5 and B6 correspond the drain voltages of 4, 5, and 6V before the pulse, and the labels A4, A5 and A6 correspond the drain voltages of 4, 5, and 6V after the pulse. The maximum threshold voltage shift ΔV_{TH} was approximately 0.9V at the drain current of 246µA when V_D was equal to 6V. On the other hand, the measured I_D-V_G characteristics of the silicon quantum dot nonvolatile memory [NVM] on a crystal silicon substrate are shown in Figure 1.7 [3]. The drain pulse of 30V for 50ms and the gate pulse of 40V for 10ms were applied simultaneously. The maximum threshold voltage shift ΔV_{TH} was

approximately 1.8V at 50µA when V_D was equal to 2V. These distinctive long threshold voltage shifts prove that quantum dot channel nonvolatile memories exhibit multi-bit storage.

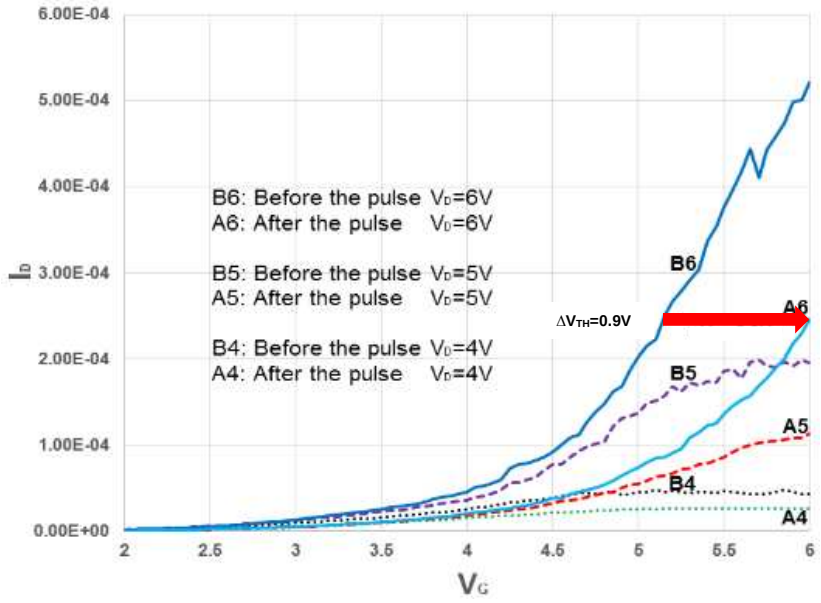

Figure 1.6. I_D-V_G Characteristics of Ge QDC NVM on Crystal Silicon Substrate

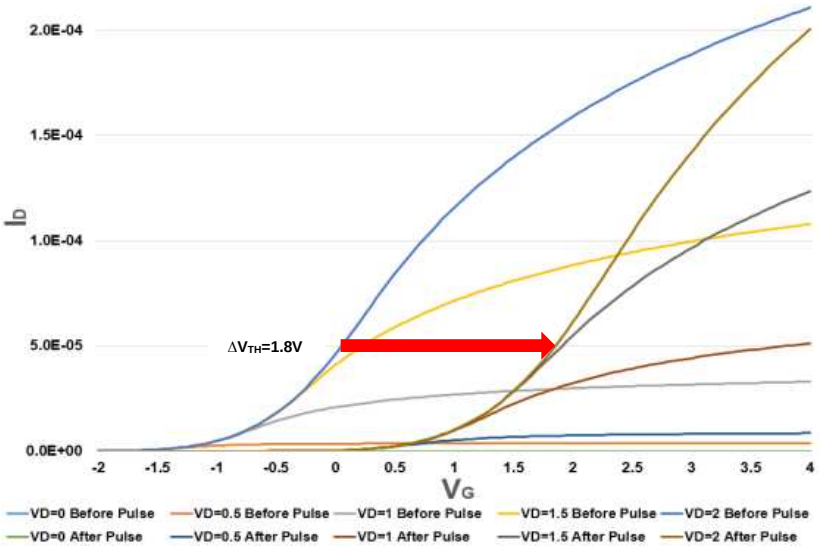

Figure 1.7. I_D-V_G Characteristics of Si QDC NVM on Crystal Silicon Substrate

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CHAPTER 2

FABRICATION AND CHARACTERIZATION OF FIELD-EFFECT TRANSISTORS AND NON-VOLATILE MEMORIES

2.1 Fabrication Procedures

The fabrication of FETs and NVMs require intricate and time consuming procedures. In this section, seventeen major fabrication procedures are explained [1].

2.1.1.1. Silicon Wafer Cleaning

The organic and metallic contaminants were removed by the silicon wafer cleaning procedures details in Appendix 5C.

2.1.1.2. Wet Oxidation

The wet oxidation furnace is shown in Figure 2.1. The purpose of the wet oxidation was to apply the silicon dioxide layer at the top of the silicon wafer. This silicon dioxide layer prevented the electron penetration during the phosphorus diffusion, and the thickness of the wet oxide layer was critical. If the wet oxide thickness was less than 1200Å, electrons could still penetrate through the wet oxide layer during the phosphorus diffusion. Therefore, the wet oxidation was conducted to obtain the optimal thickness of approximately 1250Å. But the time duration of the wet oxidation significantly depended on the room temperature, and it was not predictable. In order to achieve the optimal wet oxidation thickness, the wet oxidation required some steps, and the wet oxidation thickness was measured after each step to calculate the remaining time duration of the following step. The wet oxidation thickness varied among samples. The major factor of the thickness fluctuation was the uneven temperature distribution in the wet oxidation furnace. If the sample was placed further away from the heat center of the wet oxidation furnace, it received less heat. Therefore, the boat was placed at the heat center of the wet oxidation furnace to prevent the unevenness of the wet oxidation. The wet oxidation

thickness also varied in one sample. At the top of a sample, the temperature was higher than the bottom of the sample. Therefore, the oxidation thickness of the top of the sample was larger than the bottom of the sample. The wet oxidation diffusion boat is shown in Figure 2.2.

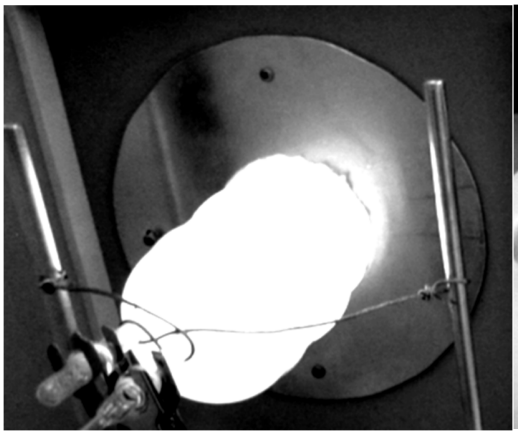


Figure 2.1. Wet Oxidation Furnace

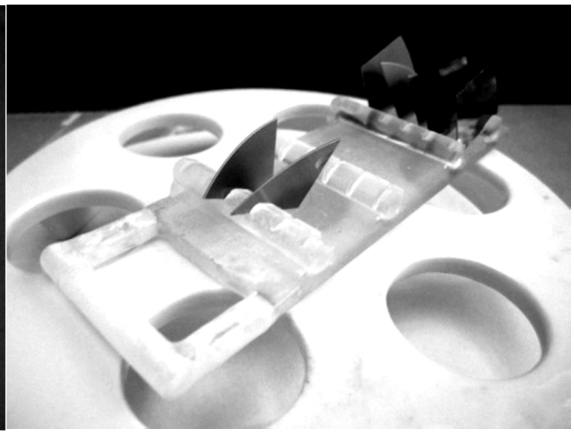


Figure 2.2. Wet Oxidation Diffusion Boat

2.1.1.3. Source and Drain Fabrication using Mask 3

Source and drain windows were fabricated by the application of Mask 3. These two windows enabled donor electrons from the phosphorus pentoxide to be absorbed into the p-type silicon substrate during the phosphorus diffusion.

2.1.1.4. Phosphorus Diffusion

The phosphorus diffusion is the rapid thermal process to establish the n-type source and the n-type drain in the p-type silicon substrate. The phosphorus diffusion furnace is shown in Figure 2.3. During the phosphorus diffusion, the silicon dioxide layer on the silicon wafer prevented the donor electron penetration, and the source and drain windows enabled donor electrons to be absorbed into the p-type silicon substrate. The sample was placed at the entrance of the furnace for 2 minutes, at the center of the furnace for 5 minutes, and at the entrance of

the furnace for 2 minutes again. Therefore, It took the total time duration of 9 minutes to complete the entire phosphorus diffusion process. Two samples were placed next to the phosphorus pentoxide and are shown in Figure 2.4.

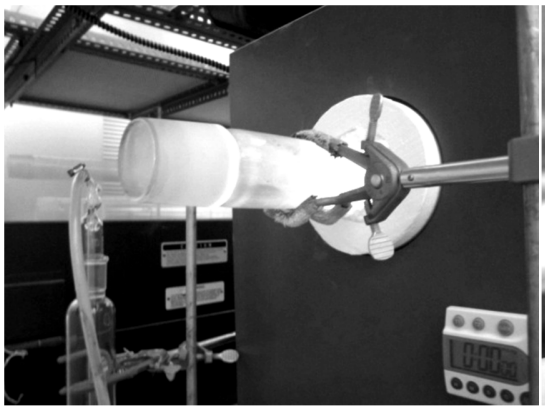


Figure 2.3. Phosphorus Diffusion Furnace

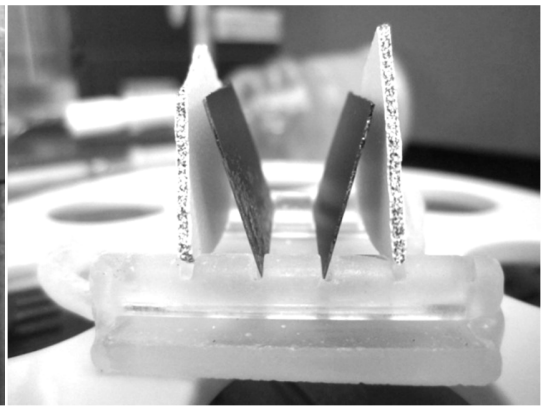


Figure 2.4. Phusphorus Diffusion Boat

2.1.1.5. Silicon Nitride Deposition

A 75Å thick silicon nitride layer was deposited on the sample using the Plasma Enhanced Chemical Vapor Deposition (PECVD) system at Harvard University, Center for Nanoscale Systems (CNS) or Yale Becton Engineering and Applied Science Center. The PECVD system at Harvard University is shown in Figure 2.5.

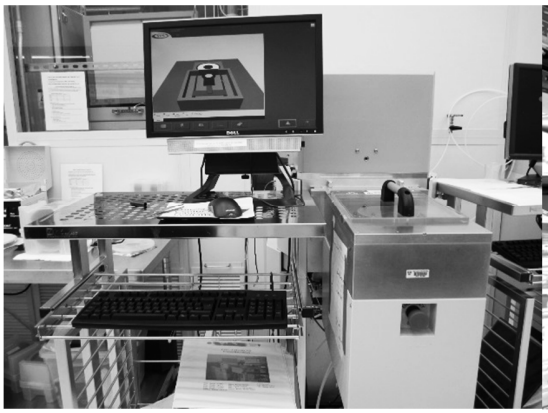


Figure 2.5. PECVD System at Harvard

Figure 2.6. Dry Oxidation Furnace

2.1.1.6. Gate Opening using Mask 4 modified, Part 1

The purpose of this procedure was to eliminate the 1250Å oxide layer and the 75 Å silicon nitride layer above the gate region to expose the gate region of the silicon wafer.

2.1.1.7. Dry Oxidation

The dry oxidation furnace is shown in Figure 2.6. The purpose of the 250Å dry oxidation was to fabricate the 125Å depth well for two layers of silicon quantum dots. If the silicon is oxidized, its volume almost doubles. Therefore, the 125Å silicon layer was consumed to produce the 250Å silicon dioxide layer. When the 250Å silicon dioxide layer was eliminated in the next procedure, the 125Å depth well was successfully fabricat to accommodate two layers of 60Å diameter silicon quantum dots. The dry oxidation timetable is shown in Table 2.2.

Quantum Dots	Furnace Temperature	Time
Si Quantum Dots	750°C	10 minutes
Ge Quantum Dots	350°C	10 minutes
SiGe Quantum Dots	425°C	10 minutes

Table 2.1. Anealing Time Table

Oxide Thickness	Furnsace Temperature	Time
20Å	800°C	1 minute 40 seconds
40Å	800°C	3 minutes 50 seconds
70Å	800°C	5 minutes
250Å	900°C/1000°C	20 minutes/10 minutes

Table 2.2. Dry Oxidation Time Table

2.1.1.8. Gate Opening using modified Mask 4

The purpose of this procedure was to eliminate the 250Å oxide layer above the gate region to provide the space for two sets of 60Å diameter silicon quantum dots.

2.1.1.9. Self-Assembly of Quantum Dots in Recessed Channel

The self-assembly consists of the following four steps: sonication, centrifugation, etching of quantum dots using dilute HF, self-assembly on p-doped semiconductor thin films or substrates. The self-assembly flow chart is shown in Figure 2.7.

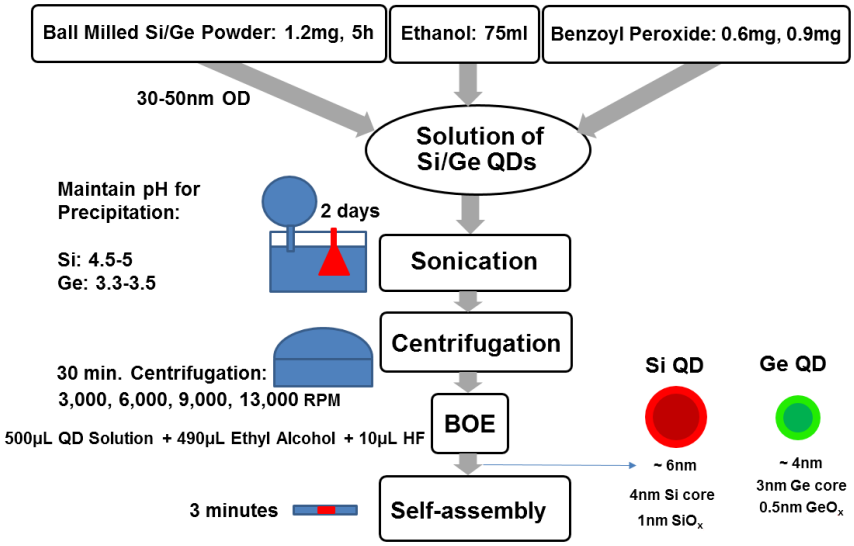


Figure 2.7. Self-Assembly Flow Chart

A. Sonication

1. 2.5g of silicon or germanium powder were placed inside of a ball milling jar, and it was left in nitrogen ambient overnight.
2. The ball milling jar was moved to a shaker, and it was shaken for 5 hours to conduct the ball milling process.

3. The quantum dot powder was scrapped from the ball milling jar, and left in a glass via in glove box which has nitrogen.
4. 75ml of Ethyl alcohol, 0.6 mg of Benzoyl peroxide for Germanium solution or 0.9 mg of Benzoyl peroxide for silicon solution and 1.2 mg of scraped silicon or Germanium powder were mixed together in a conical flask.
5. The conical flask was placed in a sonicator, and sinicated for 2 days before using the solution.
6. The pH should be maintained in the sonication. The pH is around 4.5-5 for silicon solution, and the pH is around 3.3-3.5 for Germanium solution.

B. Centrifugation

1. The germanium solution was taken in a centrifuging tube.
2. The centrifuging tube was centrifuged at 3000 RPM, 6000 RPM, 9000 RPM and 13,000 RPM for 30 Min each.
3. Remove the top part of the solution carefully so that the settled impurities won't mix in the solution again.
4. For Etching of the solution, we take a new glass via and take 500µL of Germanium or Silicon Solution + 490µL of Ethyl Alcohol + 10 µL of HF (1/1000)*.

C. Etching of Quantum Dots using dilute HF*

1. 10 µl of BOE + 10mL of Ethyl alcohol.
2. 30 µl of BOE from the above solution + 270 µl of Ethyl alcohol.

   This gives 1/1000 parts of HF.

Figure 2.8 and Equation 2.1 show the AFM measurements of two layers of silicon quantum dots and two layers of germanium quantum dots (see page 45 and page 46).

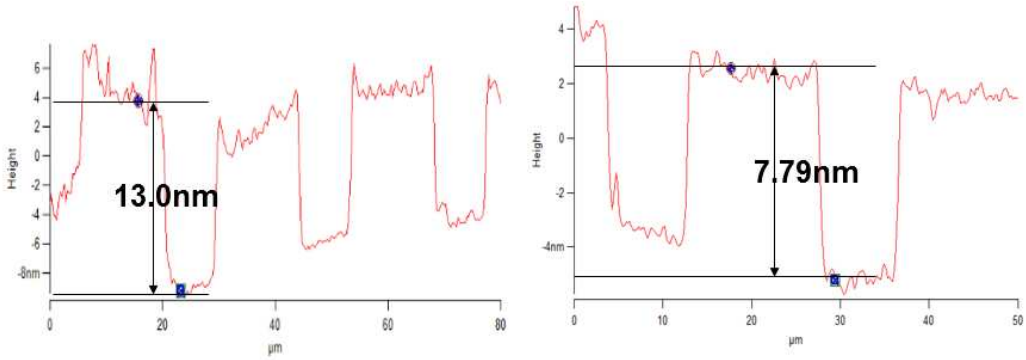


Figure 2.8. AFM Measurement Results of Si (left) and Ge (right) Quantum Dot Diameters

$$D_{Si}=\left(\frac{13.0nm}{2}\right)=6.5nm, \quad D_{Ge}=\left(\frac{7.79nm}{2}\right)\cong 3.9nm \tag{2.1}$$

D. Self-Assembly on p-doped Semiconductor thin Films or Substrates

1. The petri dish was cleaned with methanol using the cotton swabs.
2. The petri dish was dry by nitrogen gas.
3. The quantum dot solution was taken in the petri dish.
4. The sample was rinsed in DI water.
5. The sample was rinsed in Methanol.
6. The sample was dry by nitrogen gas.
7. The sample was immersed in the quantum dot solution for 3 minutes.
8. Rinse the sample in Methanol.
9. The sample was dry by nitrogen gas.
10. Annealing was conducted on the sample.

Annealing of Silicon Quantum Dot Layer:

2.1.1.10A. Annealing the Silicon Quantum Dot Layer

Quantum dot layers were annealed at 750ºC for 10 minutes in argon. The annealing timetable is shown in Table 2.1.

2.1.1.11A. Dry Oxidation

After the first two layers of the silicon quantum dots were annealed, dry oxidation was conducted upon the second layer of the silicon quantum dots. Before the oxidation, the diameter of the silicon dot core was 4 nm, the thickness of the silicon dot cladding was 1 nm, and the total diameter of the silicon dot was 6 nm [1]. After the oxidation, the diameter of the silicon dot core shrinked to 3 nm, the thickness of the silicon dot cladding expanded to 2 nm, and the total diameter of the silicon dot was 7 nm.

2.1.1.12B. Self-Assembly of Two Layers of Silicon Quantum Dots

Two more layers of Si quantum dots were self-assembled on the previous two layers of Si quantum dots of the QDG-QDC FET. This procedure is identical to 2.1.10A.

Germanium Quantum Dot Layer:

2.1.1.10B. Self-Assembly of Two Layers of Germanium Quantum Dots

The sample was immersed into the Germanium dot solution for 3 minutes.

2.1.1.11B. Annealing the Germanium Quantum Dot Layer

Quantum dot layers were annealed at 350ºC for 10 minutes in argon. The quantum dot annealing timetable is shown in Table 2.1.

2.1.1.12B. Hafnium Oxide Deposition

A hafnium oxide layer or $HfAlO_2$ nanolaminate high-k dielectric layer was deposited on the second layer of the first set of the germanium quantum dot layer to form the gate tunnel oxide.

2.1.1.13B. Self-Assembly of Two Layers of Germanium Quantum Dots

Two more layers of Germanium quantum dots were self-assembled on the previous two layers of Germanium quantum dots for QDG-QDC FET. This procedure is identical to 2.1.10B.

Source/Drain Ohmic Contact Hole Fabrication and Metallization

2.1.1.14. Opening the Source and the Drain Contacts using Mask 5

The purpose of Mask 5 was to establish the electrical connection between the metal and the source, also between the metal and the drain.

2.1.1.15. Metallization

The 2000Å aluminum was deposited on the sample to establish source, drain and gate contacts using the high vacuum evaporator, Denton Vacuum DV-502.

2.1.1.16. Metal Interconnects (Mask 6)

The purpose of Mask 6 was to separate one layer of aluminum to isolate source, drain and gate contacts. The geometrical relationship between Mask 6, the source, the drain and the gate is shown in Figure 2.12

2.1.2. Processing using a set of four Masks

The quantum dot channel FET (QDCFET) was fabricated by the lithography involved in applications of a set of four Masks. They are Mask 3, Mask 4 or Mask 4 modified, Mask 5 and Mask 6. Mask 3 was used to fabricate the source and the drain of the QDC FET. Mask 4 was used to open the source contact holes and the drain contact holes and gates. Mask 4 modified was used to open the gates. Mask 5 was used to open the source and the drain contact holes. Finally, Mask 6 was used to interconnect terminals of the source, the drain and the gate. The functions of these four masks are described as follows;

2.1.2.1. Mask 3 (Source and Drain Mask)

One segment of Mask 3 is shown in Figure 2.9. The center two columns and ten rows of devices correspond the total number of twenty transistors. These transistors have distinct source and drain shapes and distinct source and drain gap. In order to establish source and drain of the transistor, Mask 3 specified windows for the source and the drain, and electrons penetrated through these windows during the phosphorus diffusion.

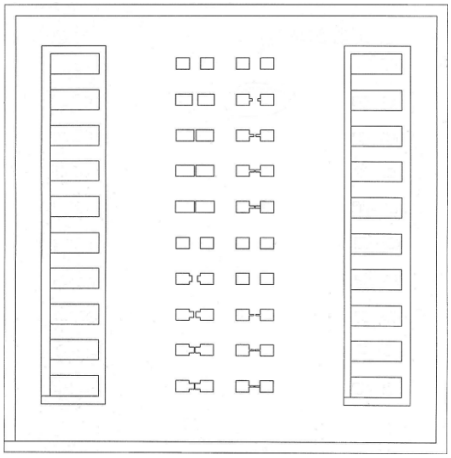


Figure 2.9. Mask 3

Left Device		Right Device	
Length	Width	Length	Width
50	50	50	50
25	50	25	10
10	50	10	10
7	50	5	10
4	50	3 1/3	10
50	50	50	50
25	26	50	50
10	26	10	26
5	26	5	6
3 1/3	26	3 1/3	6

Table 2.3. Contact Area between the Source and the Drain of Mask 3 (Units in µm)

2.1.2.2. Mask 4 and modified Mask 4

Both Mask 4 and modified Mask 4 are shown in Figure 2.10. Mask 4 has both gate openings and source and drain openings, and is used to open the gates and the source and drain contacts. On the other hand, modified Mask 4 has only gate openings, and is used to only open the gates. The gate sizes of both Mask 4 and modified Mask 4 are shown in Table 2.4. Each transistor has a distinct gate shape which corresponds the peculiarity of each transistor. Because the gate of the seventh row, the right device does not have a square nor rectangular shape, it is enlarged, and shown in Figure 2.11.

Mask 4 and modified Mask 4 were used for two times during the Buffered Oxide Etch (BOE) of the QDC FET and the QDG-QDC FET fabrications. First, two silicon dioxide layers, which were produced by the wet oxidation and the phosphorus diffusion, and one silicon nitride layer were etched by the application of Mask 4 or modified Mask 4. Second, the 250Å SiO2 layer was etched by the application of Mask 4 or modified Mask 4 to make the trench for the quantum dot self-assembly. The application of Mask 4 and modified Mask 4 were extremely difficult if the Si_3N_4 layer had more than 75A thickness, and the sample surface had little contrast to distinguish between terminals and the substrate of the QDC FET or QDG-QDC FET transistors. In this case, the application of the Mask 4 and modified Mask 4 required the video camera equipment to increase the contrast of the sample surface. The usage of the video camera equipment is described in Section 2.2.2 of this thesis.

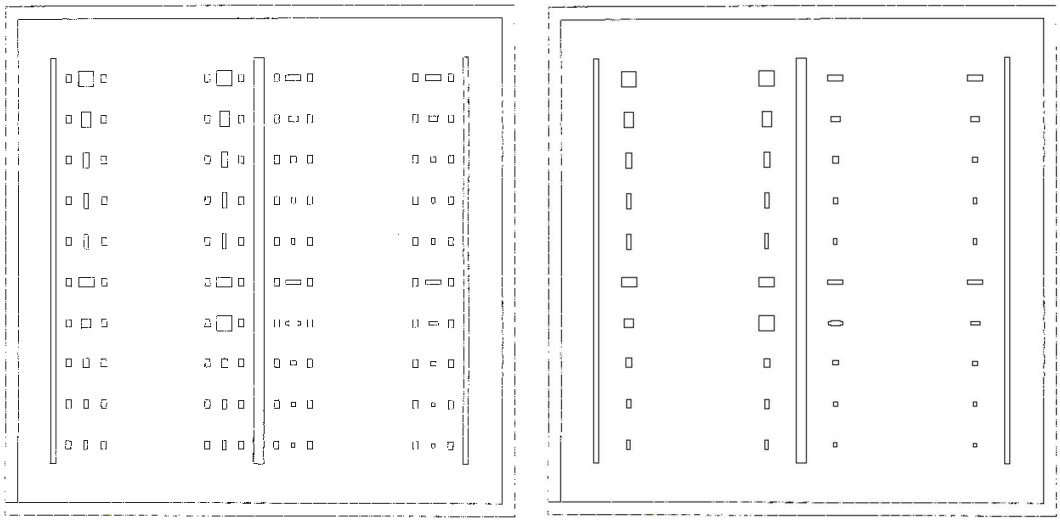


Figure 2.10. Mask 4 (left) and modified Mask 4 (right)

Left Device			Right Device		
Length	Width	Area	Length	Width	Area
60	60	3600	60	22	1320
36	60	2160	36	22	792
22	60	1320	22	22	484
16	60	960	16	22	352
14	60	840	14	22	308
60	36	2160	60	16	960
60	60	3600	60	22	1080*
22	36	792	22	16	352
16	36	576	16	16	256
14	36	504	14	16	224

Table 2.4. Gate Length, Width, and Area of Mask 4 (Units in µm) *not rectangular

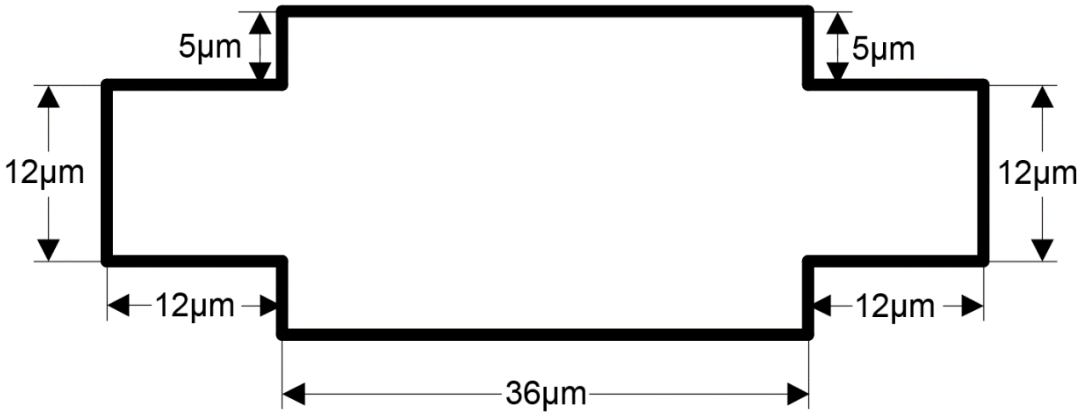


Figure 2.11. Gate Size of the Seventh Row, Right Device

2.1.2.3. Mask 5

Mask 5 was used for both fabricating contact holes for the source and the drain of the QDC FET. One segment of Mask 5 is shown in Figure 2.12. The purpose of Mask 5 was to eliminate 250 Å SiO_2 and Si_3N_4 layers to establish the electrical connection between the metal and the source, also between the metal and the drain. Because a 75 Å layer of SiN is evenly applied on the whole sample after the phosphorus diffusion, the sample das little contrast to distinguish between terminals and the substrate of the QDC FET transistor again. Therefore, the application of the Mask 5 also required the video camera equipment to increase the contrast of the sample as Mask 4 modified.

After applying UV light for 30 seconds on sample, the UV light penetrated through the source and drain contact windows, and the pattern of Mask 5 was copied to the photoresist layer on the sample. This UV exposed photoresist was developed by the 351 Developer to be eliminated. Finally, the SiO_2 layer and the 75 Å Si_3N_4 layer above the sample were etched by the Buffered Oxide Etch (BOE) for 30 seconds.

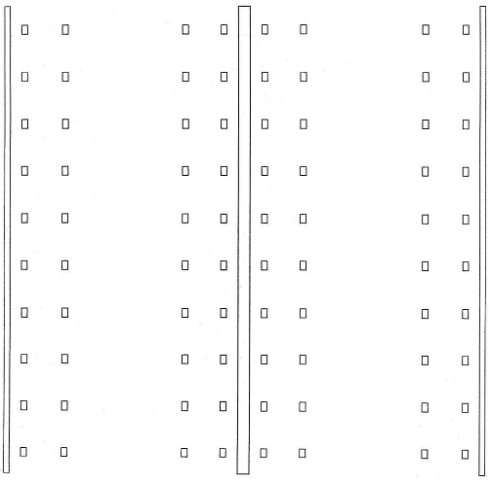


Figure 2.12: Mask 5

2.1.2.4. Mask 6

Mask 6 was applied after the completion of the metallization. Because a single layer of aluminum was coated on the source, the drain and the gate, these three terminals were connected together at this stage. Therefore, the purpose of Mask 6 was to divide one single layer of aluminum into three parts; the source, the drain and the gate. The geometrical relationship between Mask 4 and Mask 6 is shown in Figure 2.13. This Mask 6 has the common source and the common gate, and the separate drain as seen in Figure 2.13. Another type of Mask 6 is also available, and it has the separate source, the separate gate and the separate drain. This type of Mask 6 is called “Mask 4 modified.” After applying UV light for 30 seconds on sample, the UV light penetrated through the non-metalized part of the Mask 6 , and the pattern of Mask 6 was copied to the photoresist layer on the sample. This UV exposed photoresist was developed by the 351 Developer to be eliminated. At this stage, aluminum areas between terminals were exposed to outside. Finally, these exposed aluminum areas were etched by the aluminum etchant to fabricate source, drain and gate terminals of transistors. In the next step, the sample was characterized using these separate terminals.

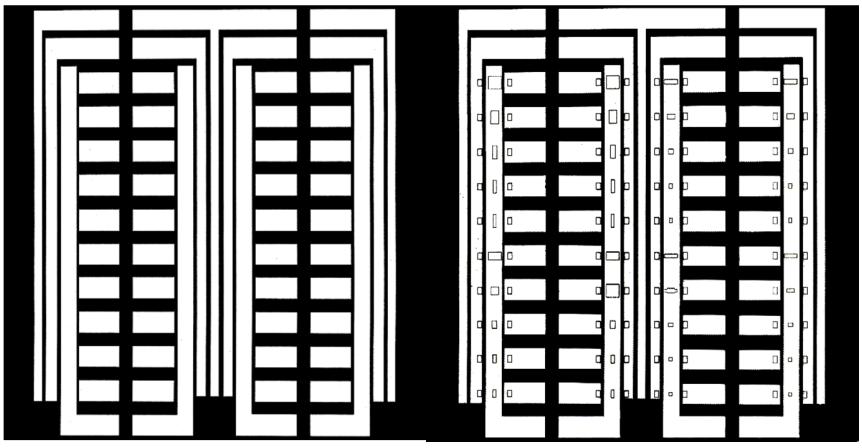


Figure 2.13. Mask 6 and Geometrical Relationship with Other Masks

2.1.3. Mask Aligner

The purpose of the mask aligner is to precisely align the position of the present mask to the previous mask image on the sample. The mask aliment procedures are summarized as follows; First, both the mask and the sample were brought into focus by adjusting the height adjustment knob for the lens. Second, the angle of the mask was adjusted by the angular adjustment knob for the mask to position the mask perfectly straight to the sample. Third, the sample was raised to minimize the gap between the top photoresist surface of the sample and the bottom chrome surface of the mask using the height adjustment dial for the sample. Fourth, the mask was perfectly aligned to the sample by angular adjustment knob for the sample. Fifth, the sample was perfectly aligned to the mask by adjusting angular, horizontal, and vertical adjustment dials for the sample. Finally, the UV light was projected on the mask. The adjustment knobs and dials are shown in Figure 2.14.

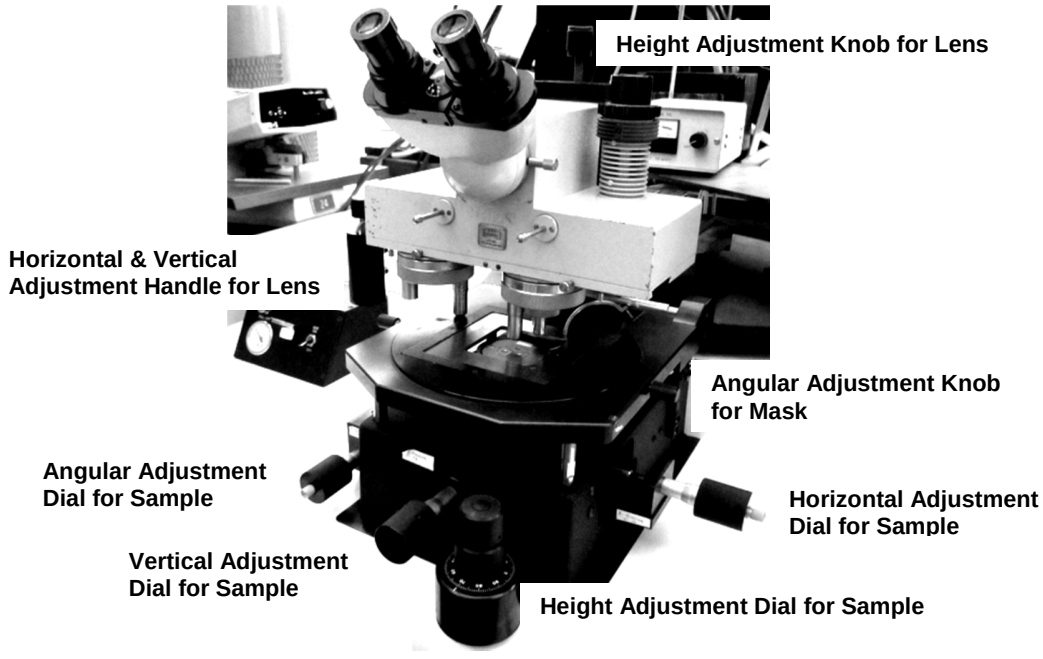


Figure 2.14. Mask Aligner Adjustment Knobs and Dials

2.1.4. High Vacuum Evaporator

The metallization was conducted using the Denton Vacuum DV-502A high vacuum evaporator shown in Figure 2.16. For the preparation procedure, frozen nitrogen was poured into the nitrogen inlet of the Denton Vacuum DV-502A to reduce the pressure inside the bell jar, and this operation is shown in Figure 2.19. The rest of the metallization procedures are summarized as follows;

Metallization Procedures (Valve Operations are shown in Table 2.5)

1. Sample Insertion

   The sample was inserted into the sample holder, and placed under the bell. The sample holder under the bell jar is shown in Figure 2.17. Then the bell jar was lowered and closed. The top control switch was set to “Manual Mode”, and this switch position is shown in Figure 2.18.

2. Vacuum the pressure in the bell jar using the mechanical pump.

   The pressure in the bell jar was decreased by the mechanical pump until the vacuum gauge indicated approximately 50 millitorr.

3. Vacuum the pressure in the diffusion pump using the mechanical pump

   The pressure in the diffusion pump was decreased by the mechanical pump before the diffusion pump was used to decrease the pressure in the bell jar.

4. Vacuum the pressure in the bell jar using the diffusion pump

   The pressure in the bell jar was decreased by the diffusion pump below 50 millitorr. In order to measure extremely low pressure very accurately, the range selector was used to measure low pressure in different ranges. The final pressure was 2×10^{-6} torr.

5. Metal Evaporation

   High current was applied to the melting pot inside the bell jar to heat the aluminum coil, which was eventually evaporated and accumulated on the surface of the sample. The aluminum coil in the melting pot is shown in Figure 2.20. The accumulation rate and the thickness of the aluminum layer were measured by Maxtek Thickness Monitor Model TM-100, which is shown in Figure 2.20. The amount of the current flow was approximately 30-40Å/sec. The final thickness of the aluminum layer was approximately 2000Å (200nm)

6. Ventilation

   The pressure in the bell jar was increased to the atmosphere pressure using "AUTO VENT". It required approximately 20 minutes to complete the ventilation operation.

7. Sample Removal

   The bell jar was lifted up, and the sample holder was removed from the bell jar. Finally, a sample was removed from the sample holder.

	Rough Valve	Back Valve	Hi-Vac Valve	Vent Valve
Step 2	**ON**	OFF	OFF	OFF
Step 3	OFF	**ON**	OFF	OFF
Step 4	OFF	**ON**	**ON**	OFF
Rest Position	OFF	**ON**	OFF	OFF

Table 2.5. Valve Operation Table for Denton Vacuum DV-502A

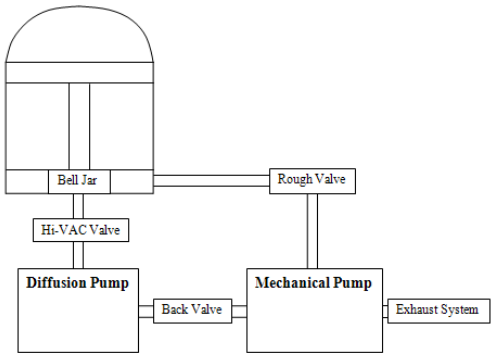


Figure 2.15. System Schematic of Denton Vacuum DV-502A

Figure 2.16. Denton Vacuum DV-502A

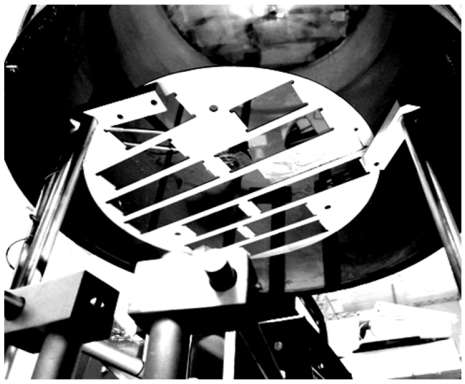


Figure 2.17. Sample Holder in Bell Jar

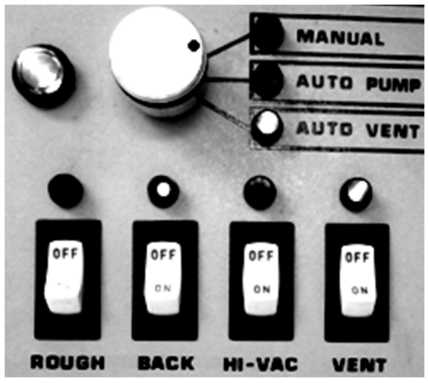


Figure 2.18. Control Switches

Figure 2.19. Frozen Nitrogen Pouring

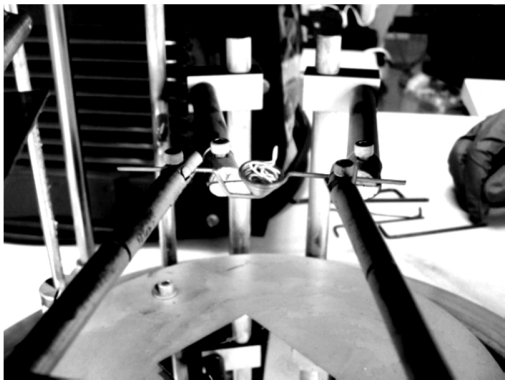


Figure 2.20. Aluminum Coil in the Pot

Figure 2.21. Maxtek Thickness Monitor

2.1.5. Atomic Layer Deposition

Figure 2.22 shows Cambridge Nanotech Savanna 200 and th controller used for this project. The atomic layer deposition (ALD) can provide exceedingly high conformality, and the aspect ratio ranges from 100 to 100,000 which is significantly higher than the chemical vapor deposition (CVD) which provides the aspect ratio ranges from 3 to 5. It can also provide excellent uniformity which is less than 1% over a 8 inch wafer. But the major disadvantage of the atomic layer deposition is the deposition rate ranges from 4Å to 6Å/minute. It is significantly lower than the chemical vapor deposition which can provide the deposition rate ranges from 100nm to 1,000nm/minute. Figure 2.23 shows the 26Å $HfAlO_2$ nanolaminate high-k dielectric combinational layer deposition for the QDG-QDC NVM gate dielectric. Table 2.6 shows the computer program used for the deposition. Figure 2.24 shows the snazzy software interface used to control the process.

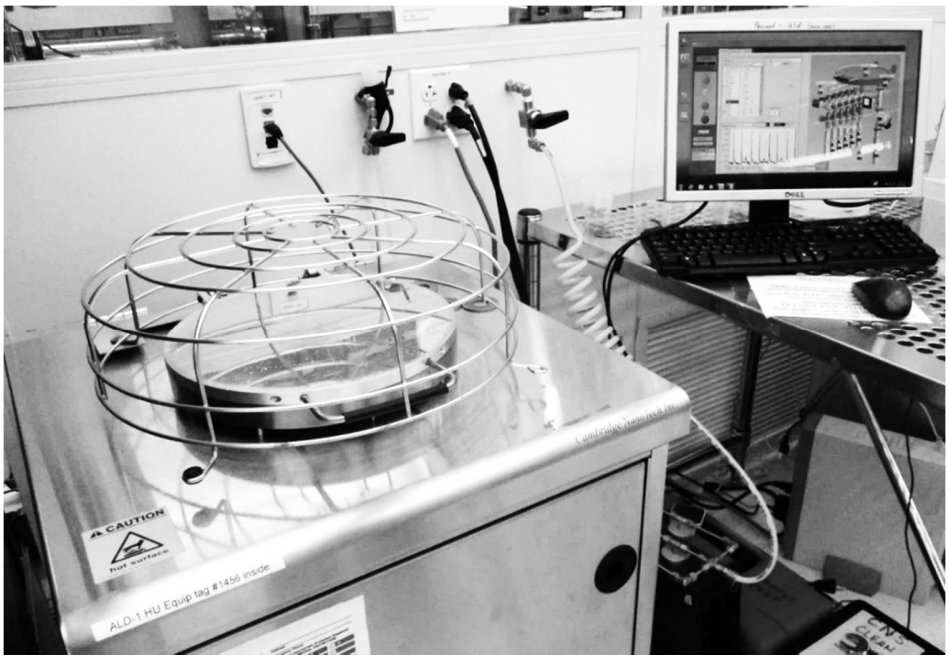


Figure 2.22. Cambridge Nanotech Savanna 200

The program was executed twelve cycles to deposit the 26Å control dielectric. The reactants and the precursors are introduced concurrently in the regular chemical vapor deposition. But the reactants and the precursors are introduced in alternating pulses in the atomic layer deposition. First, water was pulsed into the reactor to form a monolayer. The fourth and eighth instructions correspond these procedures in Table 2.6. Second, the precursor was pulsed into the reactor to react with the first monolayer, and the first monolayer was consumed. The sixth and tenth instructions correspond these procedures in Table 2.6. These four chemical pulses are also indicated in Figure 2.24. The trimethylaluminum (TMA) and the tetrakis (dimethylamino) hafnium (TDMAH) were used for the precursors for aluminum oxide (Al_2O_3), and hafnium oxide (HfO_2).

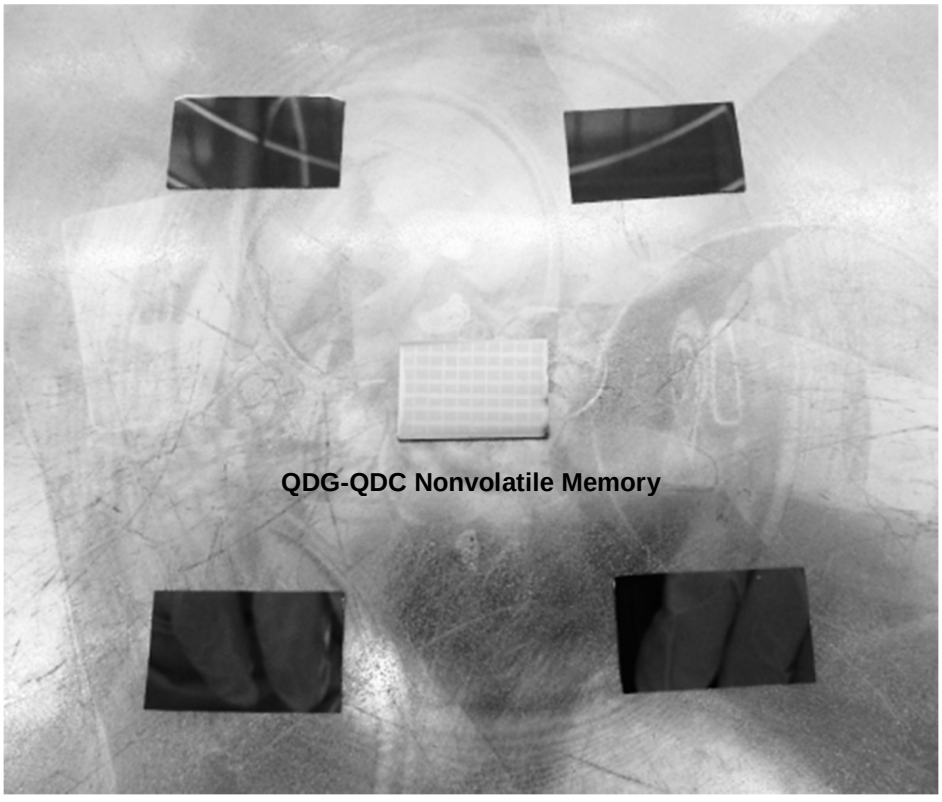


Figure 2.23. 50Å Control Dielectric Deposition using Cambridge Nanotech Savanna 200

	Instruction	#	Value	
0	Flow		20	
1	Heater	9	200	
2	Heater	8	150	
3	Stabilize	9		
4	Pulse	0	0.015	Water
5	Wait		7	
6	Pulse	3	0.015	TMA (Al_2O_3 Precursor)
7	Wait		7	
8	Pulse	0	0.015	Water
9	Wait		7	
10	Pulse	1	0.3	TDMAH (HfO_2 Precursor)
11	Wait		10	
12	Goto	4	12	
13	Wait		10	

Table 2.6. ALD Computer Program for the 50Å Control Dielectric Deposition

Figure 2.24. Snazzy Software Interface

2.1.6. Spectroscopic Ellipsometer

Woollam Spectroscopic Ellipsometer is shown in Figure 2.25. Ellipsometry measures a change in polarization as light reflected by or light transmit through a material structure. The polarization change is represented as an amplitude ratio, ψ, and the phase difference, Δ. The measured response depends on optical properties and thickness of individual materials. Therefore, ellipsometry is primarily used to determine film thickness and optical constants. Data analysis procedures are stated as follows:

1. After a sample is measured, a model is constructed to describe the sample. The model is used to calculate the predicted response from Fresnel's equations which describe each material with thickness and optical constants. If these values are not known, an estimate is given for the purpose of the preliminary calculation.
2. The calculated values are compared to experimental data. Any unknown material properties can then be varied to improve the match between experiment and calculation.
3. Finding the best match between the model and the experiment is typically achieve through regression. The Mean Square Error (MSE) is used to quantify the difference between curves. The unknown parameters are allowed to vary until the minimum MSE is reached.

Using Woollam Spectroscopic Ellipsometer, the indexes of refraction of $HfAlO_2$ nanolaminate high-k dielectric combinational layers with many different thickness were measured, and shown in Figure 2.26. The indexes of refraction are stable and the values are between 1.83 and 1.88 at the thickness between 200Å and 300Å.

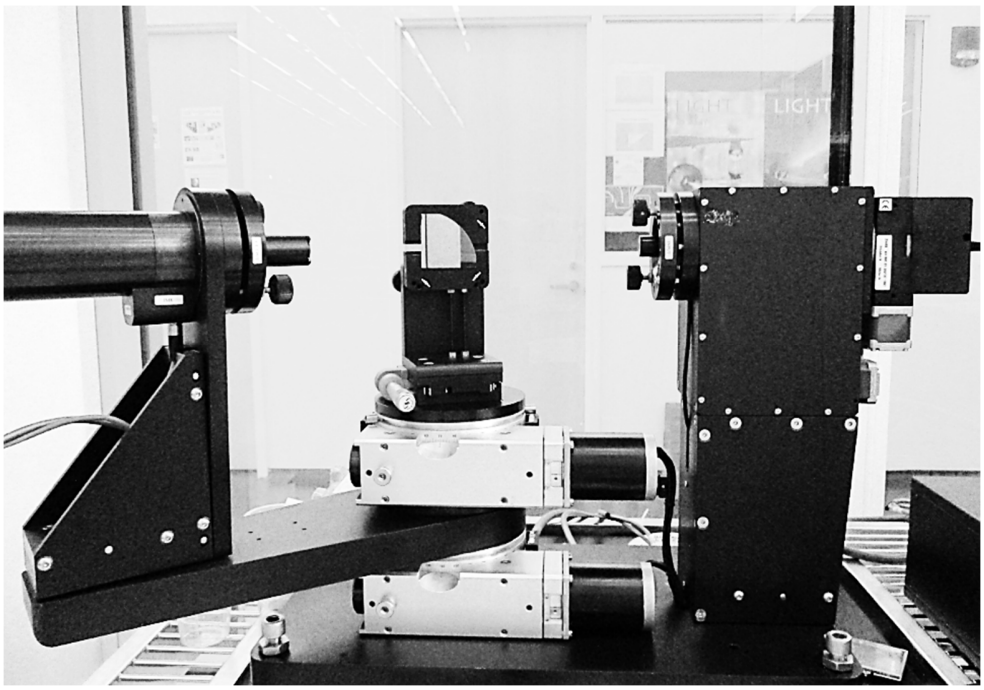


Figure 2.25: Woollam Spectroscopic Ellipsometer

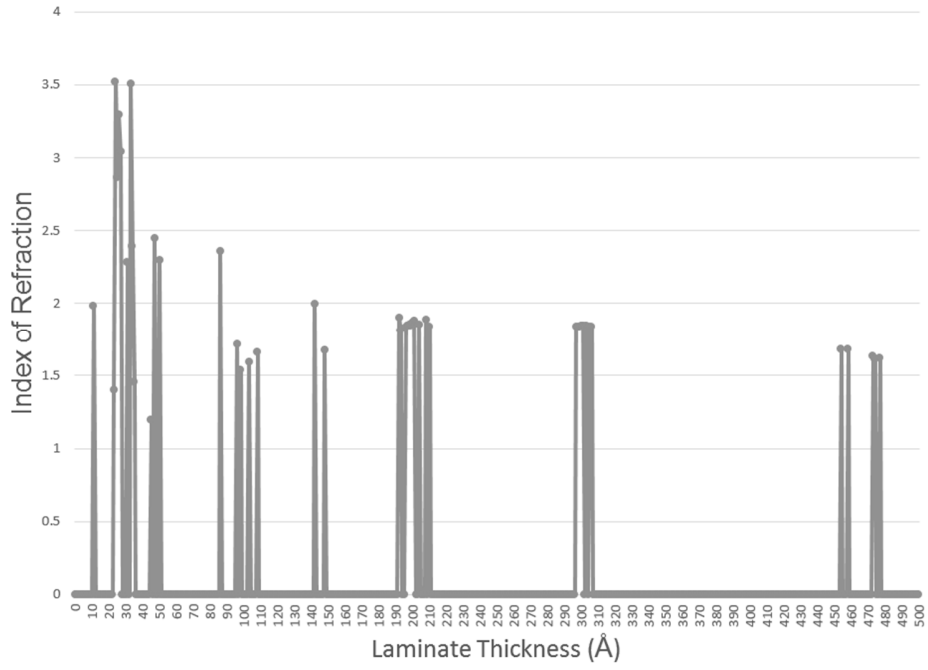


Figure 2.26. Index of Refraction versus Laminate Thickness

2.2. Characterization

2.2.1. FET Probing Station

The Mitutoyo FS70 high power microscope is used widely for many inspection and quality assurance applications, and shown in Figure 2.27. The microscope is equipped with four objective lenses; M Plan Apo 2x, M Plan Apo 10x, M Plan Apo 20x and M Plan Apo 50x. The M Plan Apo 2x objective lens and the M Plan Apo 10x objective lens were often used for this project. This microscope has also a built-in video camera, which is cable of projecting an image on the computer screen. When a device is tested, source, drain and gate terminals are connected to three probes of HP16058-60003 personality board, which is connected to a PC computer to plot I_D-V_G and I_D-V_D characteristics. The three-probe connection is shown in Figure 2.28.

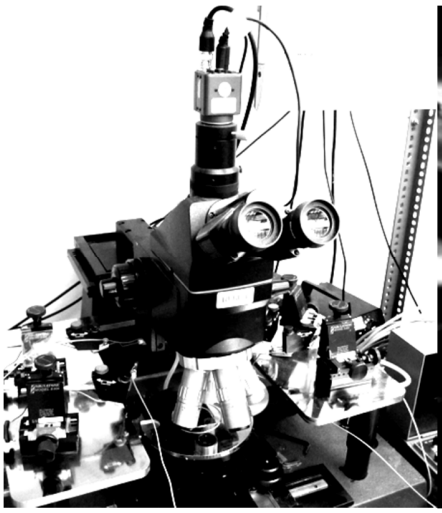


Figure 2.27. Mitutoyo FS70

Figure 2.28. Three Probe Connection

2.2.2. Video Camera to facilitate Mask Alignment

One example of silicon nitride samples is shown in Figure 2.29. Because a 75 Å layer of Si_3N_4 is applied on the sample after the phosphorus diffusion, the sample has little contrast between terminals and the substrate of the QDC FET transistor. Therefore, the application of the Mask 4 is extremely difficult, and requires video camera equipment to enhance the contrast between the foreground and the background of the image. The Sony XC-77 monochrome machine vision camera module, the Diagnostic Instruments HR100-CMT high-resolution coupler, the Hitachi VM-906U video monitor were used for this purpose. The Sony XC-77 monochrome machine vision camera module and the Diagnostic Instruments HR100-CMT high-resolution coupler are shown in Figure 2.30. The mask aligner with these video equipment is shown in Figure 2.31. The user can increase the contrast between the foreground and the background by adjusting the contrast adjustment of the monitor, and the images of the gate area of the device R4 is shown in Figure 2.32. The contrast enhancement is a must for applying Mask 4 and Mask 4 modified.

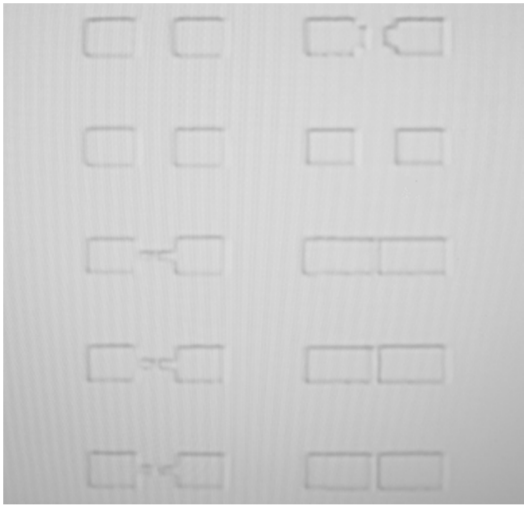


Figure 2.29. Silicon Nitride Sample

Figure 2.30. Sony XC-77 Monochrome Machine Vision Camera Module (Diagnostic Instruments HR100-CMT High Resolution Coupler attached)

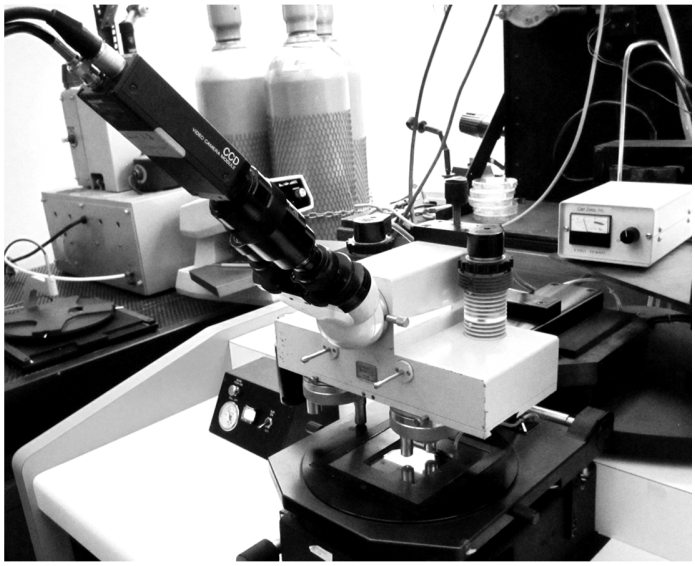


Figure 2.31. Video Camera Equipment attached to the Mask Aligner

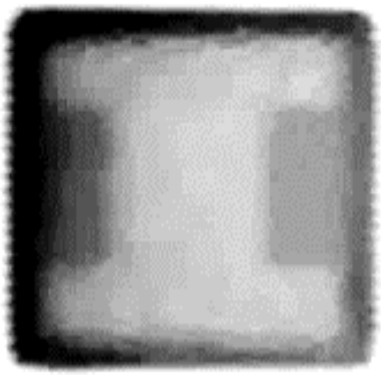


Figure 2.32. Gate Image projected on the Video Monitor

2.2.3. Thin-Film Thickness Measurements

The silicon oxide thickness is one of the most important factors which determine the performance of the QDC-QDG FFT. In order to determine the thickness of thin films accurately, the Filmetrics F20-VIS thin-film analyzer has played a vital role in all nanotechnology related projects at the University of Connecticut for past 15 years, and is shown in Figure 2.33.

2.2.3.1. Film Refractive Index

The electric magnetic field, which describes light traveling through a material at fixed time, is expressed as follows [3];

$$E = A * \cos\left(n * \frac{2\pi}{\lambda} * x \right) * e^{\left(-k * \frac{2\pi}{\lambda} * x \right)} \tag{2.1}$$

$A \equiv \text{Constant}$

$n \equiv \text{Film Refractive Index}$

$\lambda \equiv \text{Wavelengthof Light}$

$x \equiv \text{Distance}$

$k \equiv \text{Extinction Coefficient}$

The refractive index ‘n’ is defined as the ratio of the speed of light in a vacuum to the speed of light in the material. The extinction coefficient ‘k’ is defined as a measure of how much light is absorbed in the material. Therefore, the film refractive index’n’ can be determined by measuring the spectral reflectance ‘R’ and using the following equation [5];

$$R = \frac{(n-1)^2 + k^2}{(n+1)^2 + k^2} \tag{2.2}$$

2.2.3.2. Determination of Film Thickness

After the film refraction index n is determined, the next step is to determine the film thickness d using the following equation [3];

$$R = A + B * \cos\left(\frac{4 * \pi}{\lambda}\right) * n * d \qquad (2.3)$$

$R \equiv \text{Spectral Reflectance}$

$A \equiv \text{Constant}$

$B \equiv \text{Constant}$

$\lambda \equiv \text{Wavelength of Light}$

$n \equiv \text{Film Reflactive Index}$

$d \equiv \text{Thickness of Film}$

From this equation, the following statements are concluded;

1. The reflectance of a thin film varies periodically with the reciprocal of the wavelength [3].
2. If the film thickness d is increases, the spectral reflectance exhibits a greater number of oscillations over a given wavelength range [3].
3. If the film thickness d is decreases, the spectral reflectance exhibits a smaller number of oscillations over a given wavelength range [3].

2.2.3.3. Film Thickness Measurement

The procedures of film thickness measurements using Filmetrics F20-VIS are summarized as follows;

1. In order to calibrate the instrument, the following two measurements are required. The first reference measurement was conducted when the reference sample was placed on the stage. Thus, the sample was perpendicular to the light beam. This setup is showed in Figure 2.34. The second dark measurement was conducted when the reference sample was held at an angle of 10º-80º to the light beam.

2. In order to measure the film thickness of a sample, a sample was placed on the stage, and the film thickness was measured. The measurement procedures are shown in Appendix 8, and the measurement results are shown in Figure 2.35. The horizontal axis corresponds for the reflectance (%), and the vertical axis corresponds for the wavelength (nm). Actual measurement values and calculated values for the film reflectance (%) and the wavelength (nm) were displayed. The top line indicates the calculated values, and the bottom line indicates actual measured values. If the measurement was successful, the calculated values are very close to the measured values. Reflections are either in-phase or out-of-phase depends on the wavelength of the light and the thickness and properties of the layer. In Figure 2.35, the top portions correspond reflections in-phase, and bottom portions correspond reflections out-of-phase. If reflections are in-phase, the wavelength is expressed as follows;

$$\lambda = \frac{2 * n * d}{i} \qquad (2.4)$$

$\lambda \equiv$ Wavelength
$n \equiv$ ReflectiveIndex
$d \equiv$ Layer Thickness
$i \equiv$ Integer

Therefore, the layer thickness can be determined by solving Equation 2-1. The film thickness was calculated, and shown on the right side of the screen, and this particular sample had the thickness of 257.9Å.

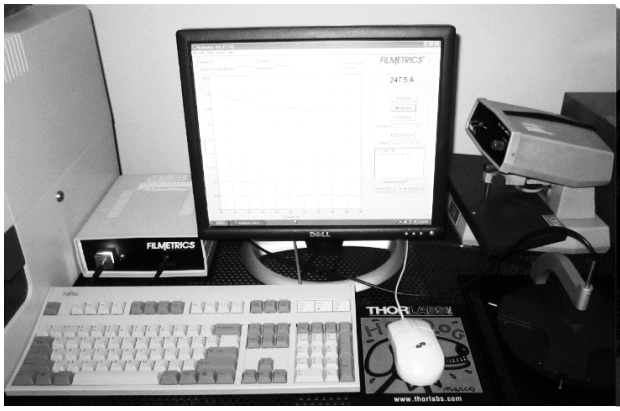


Figure 2.33. Filmetrics F20-VIS

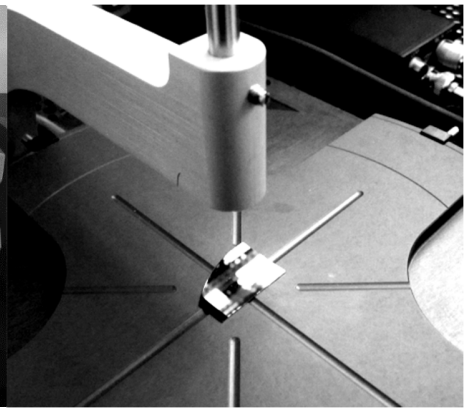


Figure 2.34. Sample on the Filmetrics Stage

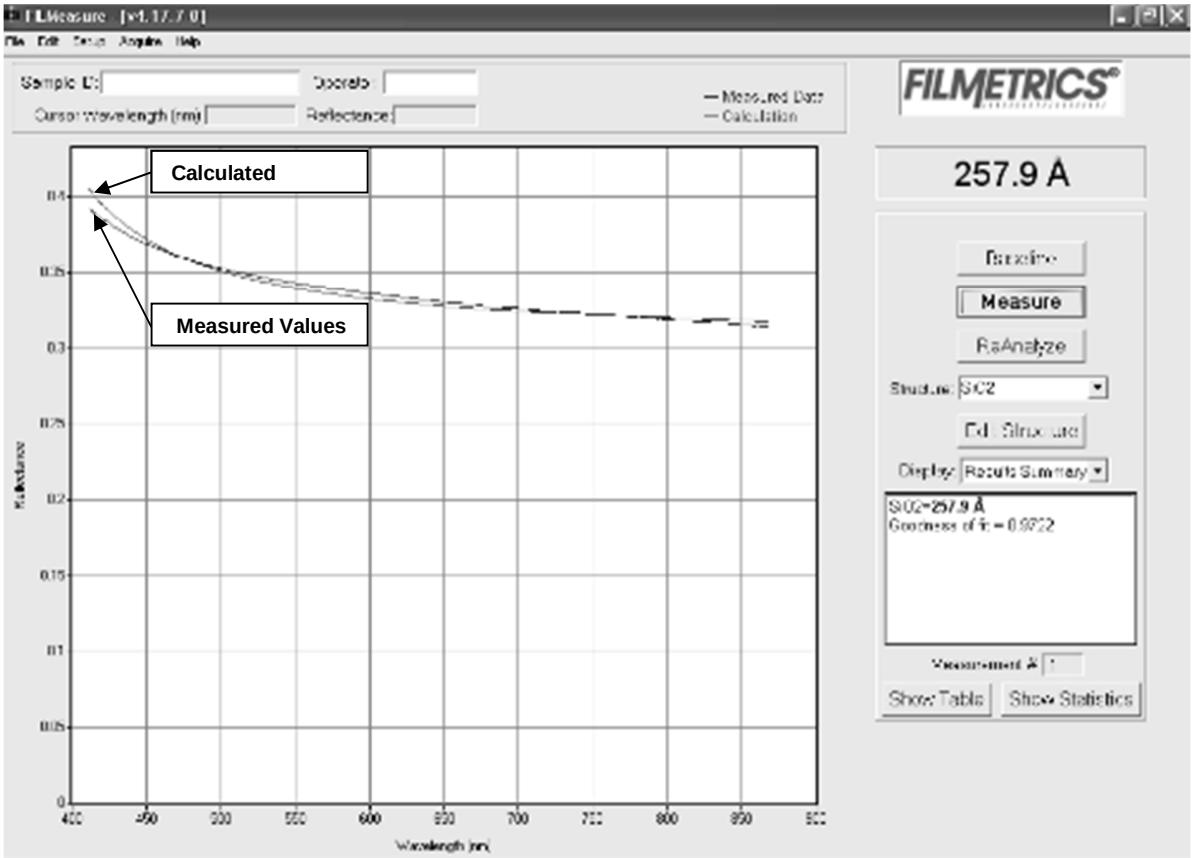


Figure 2.35. Filmetrics F20-VIS Computer Display

2.2.4. Parametric Analyzer to measure I-V Characteristics

The conventional FET, QDC FET, QDG-QDC FET were tested for I_D-V_G and I_D-V_D characteristics using HP4145B in ITE 413. I_D-V_G and I_D-V_D characteristics were plotted using LabVIEW 8.5, and the measurement results were saved as data files in the computer. HP4145B is shown in Figure 2.36.

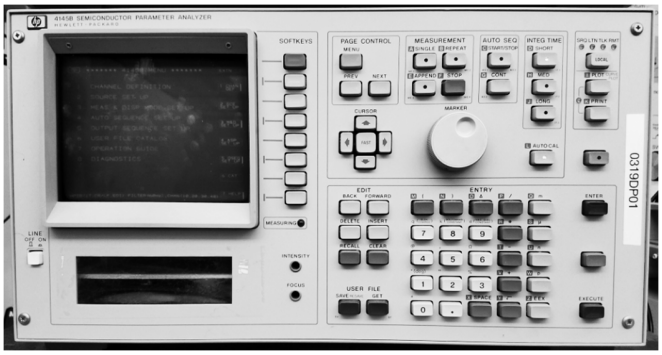


Figure 2.36. HP4145B

The QDG-QDC Nonvolatile Memories was tested in ITE325. The drain pulse and the gate pulse were simultaneously applied to the device using a pulse generator. Before and after the pulses, I_D-V_G and I_D-V_D characteristics were measured using HP4156C to obtain the treshold shift of the device. HP4156C is shown in Figure 2.37.

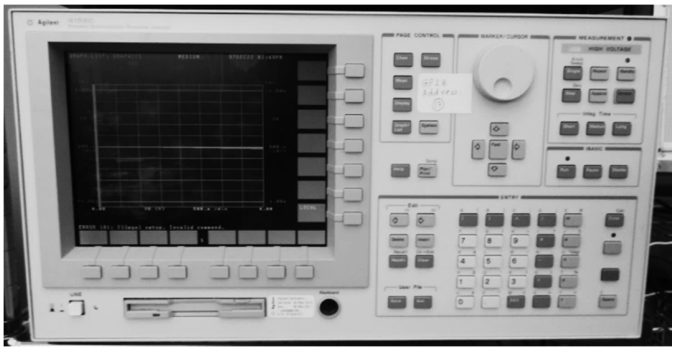


Figure 2.37. HP4156C

2.2.5. Atomic Force Microscopy (AFM)

AFM measurements were conducted using Asylum Research MFP-3D in Room 22 at Institute of Materials Science (IMS). Figure 3.38 shows the instrument, and Figure 3.39 shows the structure [5]. A laser beam impinges upon the back surface of the cantilever, and the reflected beam goes through the recollimation lens. It is reflected by the PD mirror, and impinges on the photodetector to convert the movement of the cantilever to the output voltage.

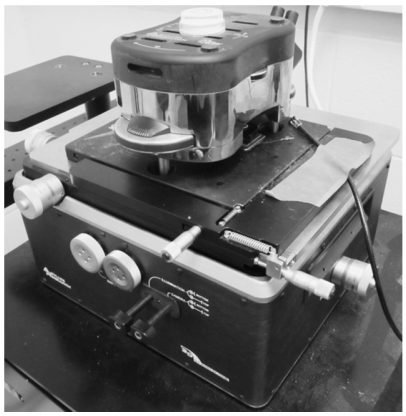


Figure 2.38. Asylum Research MFP-3D

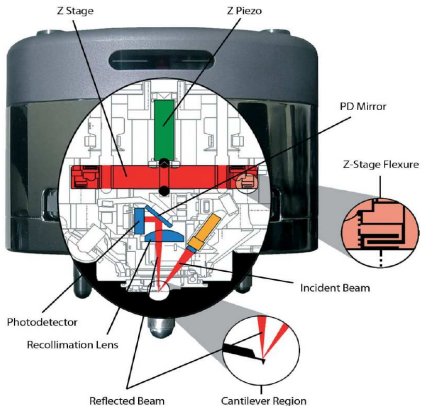


Figure 2.39. Structure of MFP-3D [5]

There are two objectives to use MFP-3D; the verification of the dimensions of the FET and NVM cross-sectional views and the measurement of the diameters of silicon and germanium quantum dots. Figure 2.40 and Table 2.7 show the AFM measurement results of FET gate and drain region. Figure 2.8 shows the AFM measurement results of silicon and germanium quantum dot diameters. They are calculated as below, and the diameter of the silicon quantum dot was 6.5Å, and the diameter of the germanium quantum dot was 3.9Å.

$$D_{Si}=\left(\frac{13.0nm}{2}\right)=6.5nm,\quad D_{Ge}=\left(\frac{7.79nm}{2}\right)\cong 3.9nm \tag{2.1}$$

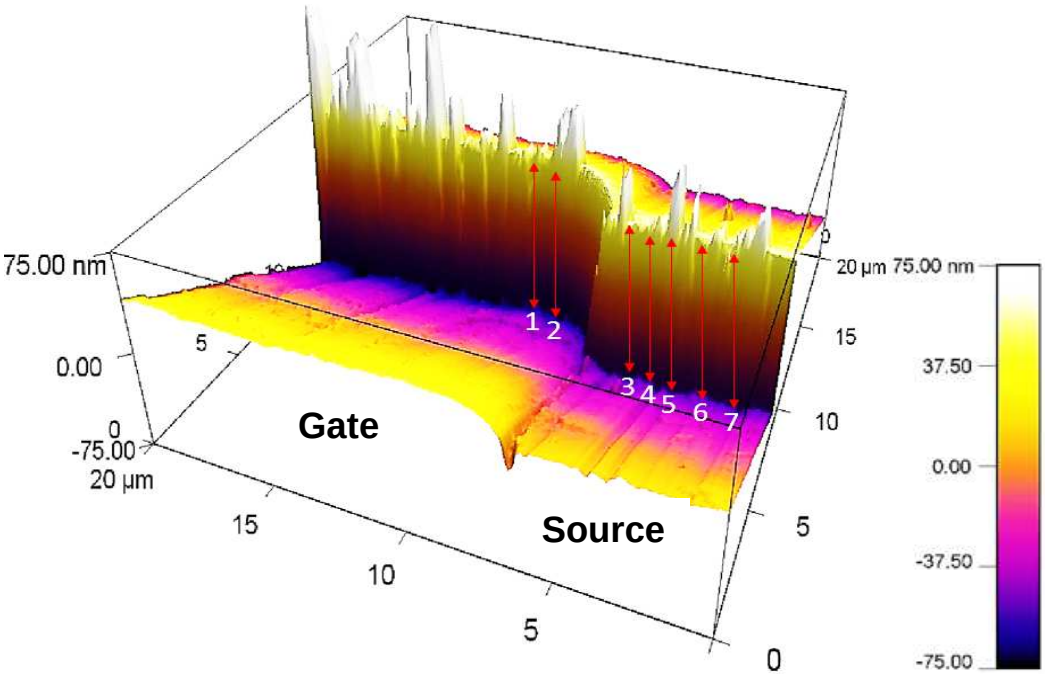


Figure 2.40. AFM Measurement Results of FET Gate and Drain Regions

Test Number	Results
Test 1	1337Å
Test 2	1348Å
Test 3	1213Å
Test 4	1197Å
Test 5	1211Å
Test 6	1215Å
Test 7	1199Å

Table 2.7. AFM Measurement Results of FET Gate and Drain Regions

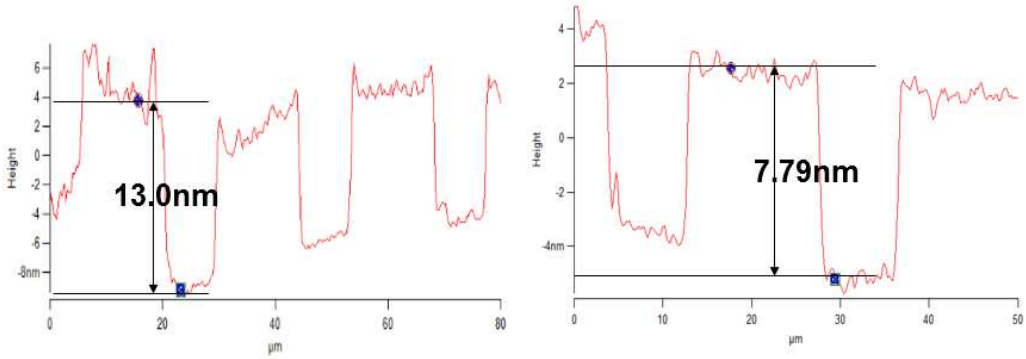


Figure 2.8. AFM Measurement Results of Si (left) and Ge (right) Quantum Dot Diameters

2.7 References

[1] Karmakar, Supriya "Novel Three-state Quantum Dot Gate Field Effect Transistor: Fabrication, Modeling and Applications", University of Connecticut, 2011.

[2] Phely-Bobin, Thomas, Debjit Chattopadhyay, Fotios Papadimitrakopoulos. "Characterization of Mechanically Attrited Si/SiO_x Nanoparticles and Their Self-Assembled Composite Films", Chemistry of Materials, pp. 1030-1036, 2002.

[3] "Taking the Mystery out of Thin-film Measurement", FILMETRICS. http://www.filmetrics.com/pdf/tmo%20v3N.pdf (accessed April 14 2012).

[4] J. Kondo, M. Lingalugari, P.-Y. Chan, E. Heller, and F. Jain, "Quantum Dot Channel (QDC) Field Effect Transistors (FETs) and Floating Gate Nonvolatile Memory Cells", *J. Electronic Materials*, 44, 9, pp. 3188-3193, 2015.

[5] "Asylum Research Atomic Force Microscopes MFP-3D Stand Alone", Asylum Research, www.AsylumResearch.com (accessed April 14, 2012).

CHAPTER 3

QUANTUM DOT CHANNEL FIELD EFFECT TRANSISTORS

THEORY AND DEVICE MODELING

3.1. MOS Introduction

In this section, parameters for NMOS devices are discussed. These include work function (Φ_{pSi}), surface potential (Φ_S), flat band voltage (V_{FB}).

The work function Φ_{pSi} is shown in Figure 3.1.

$$\Phi_{pSi} = \chi + [E_C - E_F] \quad (3.1)$$

$$\Phi_{pSi} = \chi + \left[\frac{E}{2} + \frac{k * T}{q}\ln\left(\frac{N_a}{ni}\right)\right] \quad (3.2)$$

For Al-SiO_2-pSi MOS device, the electron affinity is $\chi = 4.15\text{eV}$, the energy bandgap is $E_c - E_v = E_g = 1.1\text{eV}$, the Boltzman constant is $k = 1.3806 * 10^{-23} J/K$, the temperature is $T = 300K$, the acceptor concentration is $N_a = 10^{15}$, the intrinsic concentration is $n_i = 1.5 * 10^{10}$.

Therefore, the work function is substantially calculated as follows;

$$\Phi_{pSi} = 4.15\text{eV} + \left[\frac{1.1}{2} + 0.0259 * \ln\left(\frac{10^{15}}{1.5 * 10^{10}}\right)\right]$$

$$\Phi_{pSi} = 4.15\text{eV} + [0.55\text{eV} + 0.28768\text{eV}] = 4.15\text{eV} + 0.83768\text{eV}$$

$$\Phi_{pSi} = 4.98768\text{eV} \cong 4.9877\text{eV for long channel FETs}$$

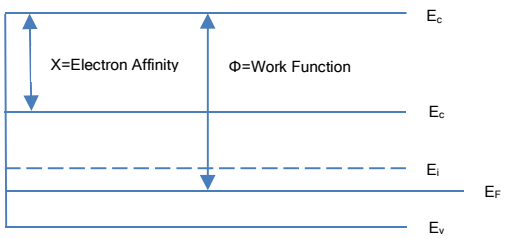


Figure 3.1. Surface-Induced Energy Band Diagram of p-type Semiconductor

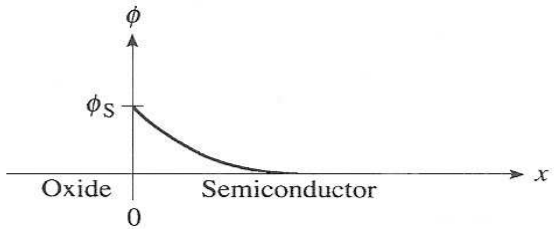
Surface Potential: Φ_S

The internal electrostatic potential inside the semiconductor is expressed as Φ(x) [1]. The potential Φ(x) is actually the function of a given point x which is the depth into the semiconductor. Therefore, the surface potential Φ_S is the Φ(x) where x is equal to zero [1]. If the electrostatic potential Φ(x) increases, the band-bending occurs downward. The potential Φ(x), and the surface potential Φ_S are expressed as follow [1];

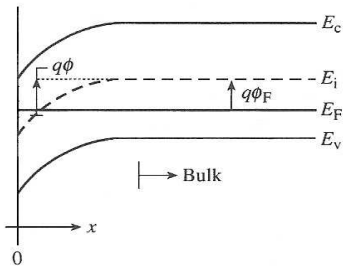
$$\Phi(x) = \frac{1}{q} * [E_i(bulk) - E_i(x)] \qquad (3.3)$$

$$\Phi_S = \frac{1}{q} * [E_i(bulk) - E_i(surface)] \qquad (3.4)$$

Also, the relationship between the electrostatic potential Φ(x) and band-bending is shown in Figure 3.2 [5].



a. Electrostatic Potential: Φ



b. Band-Bending

Figure 3.2. Relationship between the Electrical Potential Φ (a) and the Band-bending (b)
Source: R. Pierret, *Semiconductor Device Fundamentals*. New York: Addison Wesley Longman, pp. 573, 1996.

Flat Band Voltage: V_{FB}

The energy band diagram shows "Flat band" when no gate voltage was applied, and this phenomenon is compared with "Accumulation", "Depletion" and "Inversion", and showed in Figure 3.3 [1]. The flat band voltage is expressed as follows;

$$V_{FB} = \phi_{ms} - \frac{Q_{OX}}{C_{ox}} - \frac{Q_M * \gamma_M}{C_{ox}} - \frac{Q_{IT}}{C_{ox}} \tag{3.5}$$

$$\therefore V_{FB} \cong \phi_{ms} - \frac{Q_{OX}}{C_{ox}} \tag{3.6}$$

$Q_{OX} \equiv$ Oxide Charge

$C_{ox} \equiv$ Oxide Capacitance, $Q_M \equiv$ Mobile Ion Charge in the Oxide,

$\gamma_M \equiv$ Mobile Ion Distribution in the Oxide

$Q_{IT} \equiv$ Interfacial Traps Charge

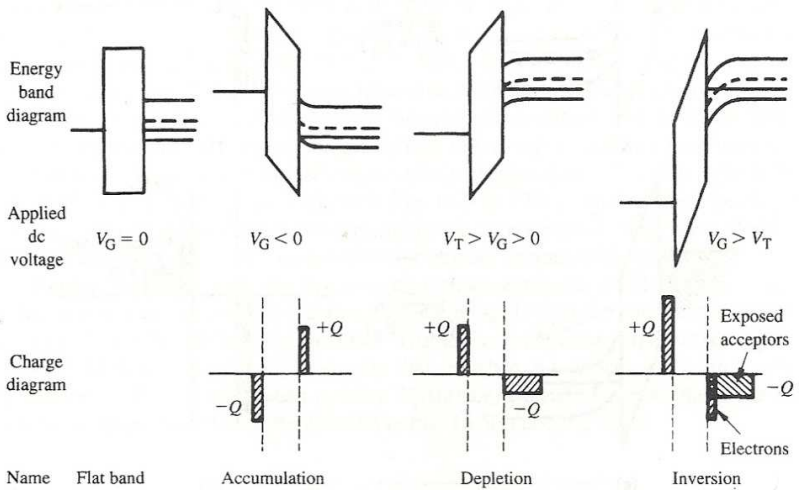


Figure 3.3. Energy Band Diagram and Charge Density Plots for P-Type Device
Source: R. Pierret, *Semiconductor Device Fundamentals*. New York: Addison Wesley Longman, pp. 570, 1996.

3.2. Energy Band Diagram

3.2.1. Quantum Simulations in QDC FETs

An array of individually cladded quantum dots (e.g. SiO_x-cladded Si and GeO_x-Ge), results in a quantum dot superlattice (QDSL) when the barrier separation between dots is ~1 nm [2]. Unlike Si-SiGe, GaAs-AlGaAs, InGaAs-InP, InGaN-GaN and other semiconductor superlattice where the band discontinuities (ΔE_c and ΔE_v) are not very high, SiOx-Si and GeOx-Ge QDSL exhibits very narrow energy mini-bands that are separated with the energy >0.2eV, which is much higher than in nanowires [2].

Figure 3.4 shows the band structure of Si/SiO_2 QDSL using 3-D Kronig-Penny Model, with inset showing expanded view of the 2nd mini-band [2]. Figure 3.5(a) shows the density of states (DOS) of Si/SiO_2 QDSL with inset showing expanded view of the 8th mini-band [2]. The energy mini-bands, intra-band separations and mini-band energy widths for Si and Ge QDs are shown in Figure 3.5(b) using 1-D Kronig-Penny model [2]. The parameters used are shown in Table 3.1 [2]. Here, electron affinity is χ, energy band gap is E_g, electron and hole effective masses are m_e and m_h, and dielectric constant is ε_r [2].

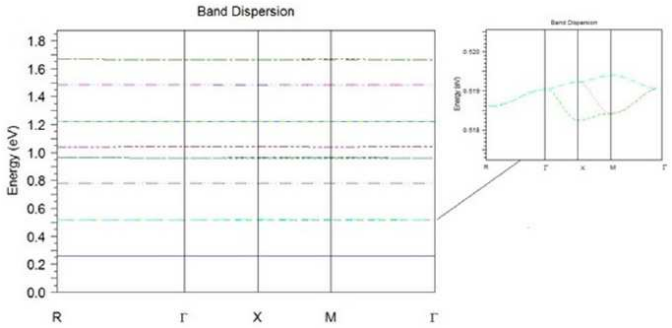


Figure 3.4. Band Structure of $Si–SiO_2$ Quantum Dot Superlattice (QDSL) obtained using the 3D Kronig–Penny Model; inset shows expanded view of second mini-band [2

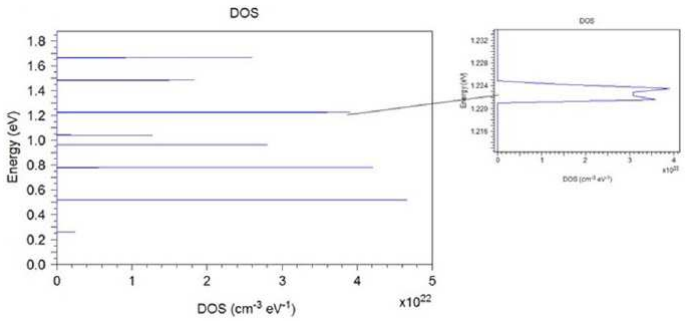


Figure 3.5(a). Density of States (DOS) of Si–SiO2 QDSL obtained using the 3D Kronig–Penny Model; inset shows expanded view of eighth mini-band [2]

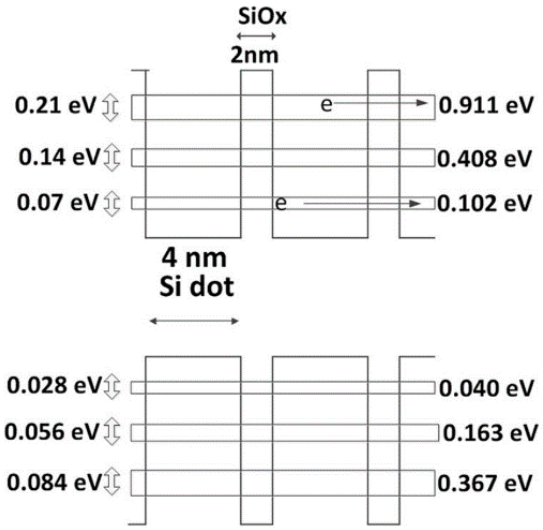


Figure 3.5(b). Schematic Representation of Energy Mini-band Location, Separation, and Width for Si–SiO2 QDSL [2]

Layer	Thickness (nm)	χ (eV)	E_g (eV)	m_e	m_h	ε_r
SiO_x	1	0.9	9.0	0.5	0.5	3.9
Si QD	4	4.15	1.12	0.19	0.49	11.9

Table 3.1. Parameters used to compute SiO_x–Si QDSL Parameters [2]

After the band structure of QDSL is computed, we calculate the 2-dimnsional electron distribution in the coupled quantum dot layers representing the transport channel (treating them as quantum wells) by solving the 1-D Poisson's and Schrödinger's [Equation 3.7 and Equation 3.9] self-consistently [3,4,5]. Here, ϕ is the electrostatic potential, n_{QM} is the 2D electron gas in the quantum well, n and are the 3D electron and hole concentrations, and N_D^+ and N_A^- are the ionized donor and acceptor concentrations. The 2-D contribution is given by Equation 3.8, where E_F is the Fermi level, E_n and ψ_n define the eigen energy and wavefunction of bound states, and Θ defines the Heaviside Step function. E_n and ψ_n are determined by the Schrödinger's Equation 3.9.

$$\nabla \cdot (\varepsilon \nabla \phi) = q(n_{QM} + n - N_D^+ + N_A^- - p) \qquad (3.7)$$

$$n_{QM} = \sum_n \frac{m^*}{\pi\hbar^2}\Theta(E_F - E_n)\ln\left[1+\exp\left(\frac{E_f - E_n}{kT}\right)|\psi_n|^2\right] \qquad (3.8)$$

$$\frac{\hbar^2}{2}\nabla \cdot \left(\frac{1}{m^*}\nabla\Psi w\right) + (E_n - V)\Psi w = 0 \qquad (3.9)$$

Here, V is determined by the band offsets at the well-barrier interface and electrostatic potential. Figure 3.6(a) and Figure 3.6(b) show the simulation of electron wavefunction in GeOx-Ge quantum dot superlattice (QDSL) transport QDC channel at gate voltages of -1.3 and -0.3V, respectively. The voltage range can be adjusted by varying the work function used. The parameters are shown in Table 3.2.

HfO_2	0.0000	2.4 (calc)	5.3-5.7	0.22	0.15	20.0	0.0e00	0.0e00
Al_2O_3	0.0000	1.95	6.95	0.2	0.25	9.34	0.0e00	0.0e00

Table 3.2. Parameters used for $HfAlO_2$ gate oxide (average)

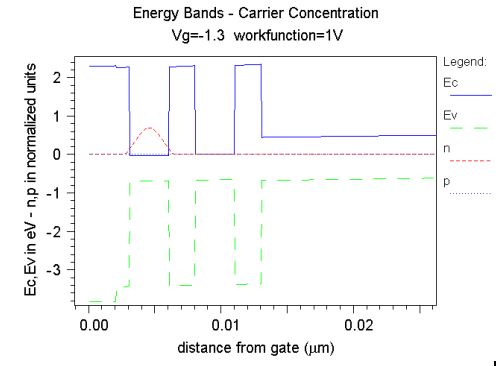


Figure 3.6(a). Electron wavefunction at V_G= -1.3 V in floating gate

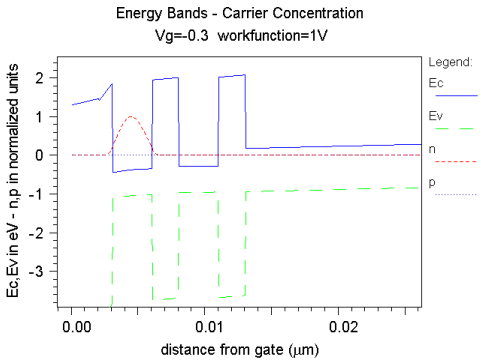


Figure 3.6(b). Electron wavefunction at V_G= -0.3 V in floating gate

As the gate voltage is increased from -1.3V to -0.3V, the magnitude of charge in floating gate increases

Layer	**Thick(um)**	**Chi(eV)**	**Eg(eV)**	**me**	**mh**	**er**	**Nd**	**Na**
1. $HfAlO_2$	0.0020	2.2	6.13	0.21	0.20	14.7	0.0e00	0.0e00
2. GeO_X	0.0010	2.25	5.70	0.16	0.16	4.4	0.0e00	0.0e00
3. Ge – QD 1	0.0030	4.55	0.67	0.08	0.28	16.0	0.0e00	0.0e00
4. GeO_X	0.0020	2.25	5.70	0.16	0.16	4.4	0.0e00	0.0e00
5. Ge – QD 2	0.0030	4.55	0.67	0.08	0.28	16.0	0.0e00	0.0e00
6. GeO_X	0.0020	2.25	5.70	0.16	0.16	4.4	0.0e00	0.0e00
7. Si	0.1000	4.15	1.12	0.19	0.49	11.9	0.0e00	1.0e16

Table 3.3. Parameters for GeO_x-Ge quantum dot channel FET

3.2.2. Energy Band Diagram across the Channel and the Gate

In this section, the energy band diagrams are shown along the channel (x) and the gate (y). First, the diagram is shown across the source and the drain which is shown by the horizontal arrow in Figure 3.7. Second, the diagram is shown across the gate which is shown by the vertical arrow in Figure 3.7.

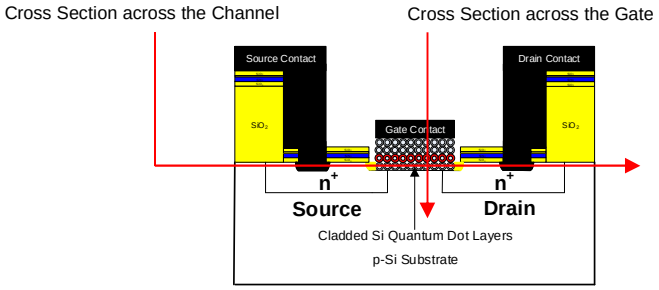


Figure 3.7. Two Cross Sections across the QDC-QDG FET

The relationship between the V_D and positions of mini-bands was sequentially shown in Figure 3.8 [3]. In Figure 3.8 (a), there is no V_D, and none of the mini-bands are under the Fermi level. In Figure 3.8 (b), if V_D is applied, and the first mini-bands are under the Fermi level. Thus, electrons are able to be transferred to above the first mini-band. In Figure 3.8 (c), additional V_D is applied, and the second mini-bands are under the Fermi level. Thus, electrons are able to be transferred to above the second mini-band. In Figure 3.8 (d), additional V_D is applied, and the third mini-bands are under the Fermi level. Thus, electrons are able to be transferred to above the third mini-band. Therefore, electrons move above the next mini-band if V_D increases. The relationship between the V_G and positions of mini-bands is shown in Figure 3.9. if V_G is applied, and the first mini-band in the second well is under the first mini-band in the first well. Thus, electrons are able to be transferred from the first mini-band in the first well to the first mini-band in the second well.

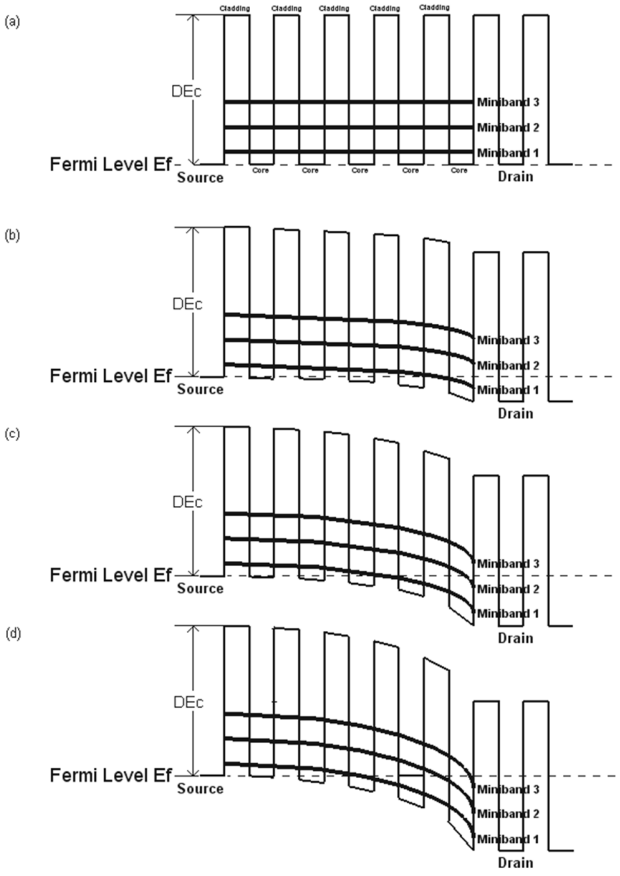


Figure 3.8. Energy Band Diagram across the Channel

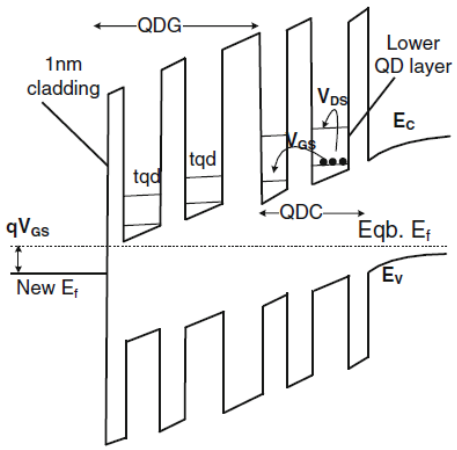


Figure 3.9. Energy Band Diagram across the Gate

3.3.Nonvolatile Memory Model

During the write operation of the memory, a gate voltage pulse and a drain voltage pulse are applied simultaneously to transfer charge from the inversion channel to the Ge quantum dot layers at the floating gate. The charge in the floating gate shifts the threshold voltage once the 'Write' operation is carried out. The threshold voltage (V_{TH}) of a quantum dot floating gate nonvolatile memory, $V_{TH\text{-}QDNVM}$ is dependent on the amount of charge present in the QD floating gate, and expressed as Equation 3.10 [6-12].

$$V_{TH-QDNVM} = V_{TH} + \Delta V_{TH} \tag{3.10}$$

The threshold voltage shift (ΔV_{TH}), which is due to the charges present in the QDs, is expressed as Equation 3.11 [9]. *C* is the capacitance between the control gate and the QD floating gate.

$$\Delta V_{TH} = \frac{Q}{C} = \frac{\int_{o}^{t_w} j(t)Adt}{C} \tag{3.11}$$

Here, *j(t)* is the current per unit area flowing during the charging time (t_w) of the QD floating gate while performing the write or program operation, and expressed as Equation 3.12.

$$j(t) = q * n_{dot} * N_{QD} * P_{W \to d} \tag{3.12}$$

Here, *q* is the charge of the electron, n_{dot} is the number of electrons per dot (bound as well as the electrons trapped at the QDs interface), N_{QD} is the density of QDs, and $P_{w \to d}$ is the tunneling rate of carriers from the channel (QDSL treated as quantum well) to the quantum dots. The tunneling transition rate of electrons from the QDSL channel to the floating gate quantum dots can be expressed in the transfer Hamiltonian form as Equation 3.13 [13,14].

$$P_{w \to d} = \frac{4\pi}{\hbar} \sum_{w,d} \left| \langle \psi_d | H - H_w | \psi_w \rangle \right|^2 (f_w - f_d) \delta(E_d - E_w) \tag{3.13}$$

ψ_w and ψ_d are the wave functions for the QDSL. f_w and f_d are the Fermi functions for the occupation probability of states in the quantum well and quantum dot. The total Hamiltonian, H can be expressed as Equation 3.14.

$$H = -\frac{\hbar^2}{2m^*}\nabla^2 + V_w(z) + V_d(r) \qquad (3.14)$$

The electron distribution in an inversion channel/QDSL well can be calculated by solving the 1-D Schrödinger's and the Poisson's equations self-consistently, and expressed as Equation 3.15 [15].

$$\frac{\hbar^2}{2}\nabla\cdot\left(\frac{1}{m^*}\nabla\Psi w\right) + (E_n - V)\Psi w = 0 \qquad (3.15)$$

m^* is the effective mass of the electron, ψ_w and E_n define the bound states, and V is determined by the band offsets at the interfaces in combination with the electrostatic potential.

$$\nabla\cdot(\varepsilon\,\nabla\phi) = q(n_{QM} + n - N_D^+ + N_A^- - p) \qquad (3.16)$$

ε is the permittivity of Si, ϕ is the electrostatic potential, q is the charge of the electron, n_{QM} is the electron gas in the inversion channel, n and p are the 3-D electron and hole concentrations, N_D^+ and N_A^- are the ionized donor and acceptor concentrations.

3.4. Quantum Simulation

The electron distribution in a transport channel/quantum well is calculated by solving the 1-D Schrödinger's and the Poisson's equations self-consistently [16]. In this simulation, the gate dielectric thickness of 50Å, and the control dielectric thickness of 20Å are used [16]. Table 3.4 shows the parameters used for the simulation of device characteristics for the QDC NVM, and Table 3.5 shows the parameters used for the simulation of the Ge QDC NVM with $HfAlO_2$ combinational layers [16]. Figure 3.10 shows the simulation of charge transfer to Ge QDs, 'Writing' bit '1', and a part of electrons is migrated from the inversion channel to the lower Ge QD layer of the floating gate [16]. Figure 3.11 shows the charge density in the transport channel, and the plateau part of the charge density line indicates that there is onset of tunneling from the transport channel to the floating gate [16].

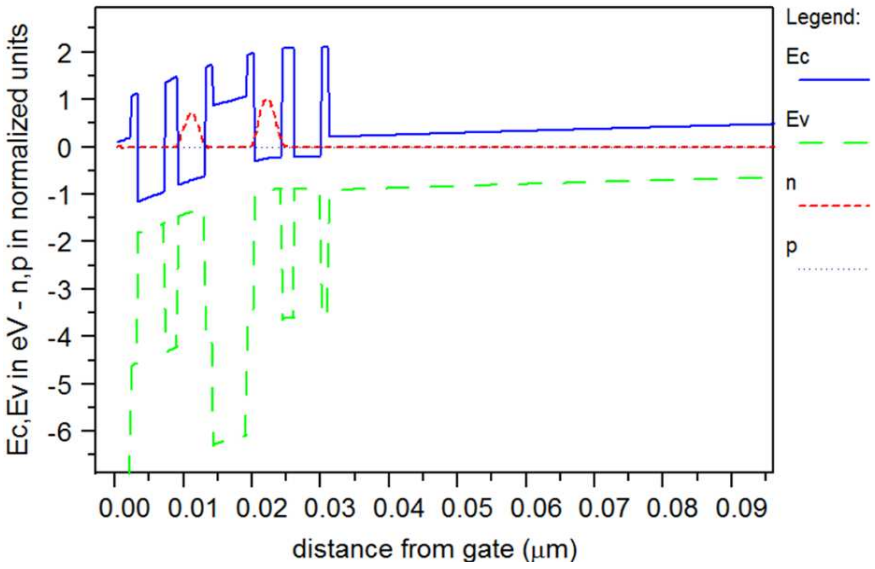


Figure 3.10. Electron Wavefunctions in Quantum Dot Layers

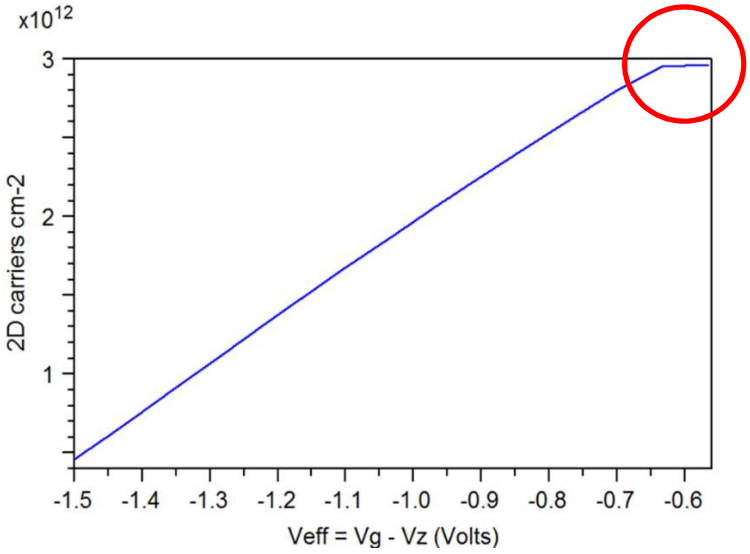


Figure 3.11. Charge Density in the Inversion Channel
Circle shows onset of tunneling from the inversion layer (formed in the QDC transport channel) to the floating gate.

Parameter	Unit	Value	Note
W	µm	60	
L	µm	60	
v1	cm^2/V-s	80	State 1
v2	cm^2/V-s	96	State 2 (1.2 x v1)
ε_{eff}	———	3.9	Silicon
ε_0	F/cm	8.854×10^{-14}	
t	cm	1.2×10^{-6}	
C_{ox}	F/cm^2	8.854×10^{-7}	

Table 3.4. Parameters used for the Simulation of Device Characteristics for QDC NVM

Layer	Thickness (µm)	χ (eV)	E_g (eV)	m_e	m_h	e_r
HfAlO2	0.002	3 0.12	7.15	0.10	0.20	17.0
GeOx	0.0010	2.25	5.70	0.16	0.16	12.0
GeQD	0.0040	4.55	0.67	0.08	0.28	16.0
GeOx	0.0020	2.25	5.70	0.16	0.16	12.0
GeQD	0.0040	4.55	0.67	0.08	0.28	16.0
GeOx	0.0010	2.25	5.70	0.16	0.16	12.0
HfAlO2	0.005	3.12	7.15	0.10	0.20	17.0
GeOx	0.0010	2.25	5.70	0.16	0.16	12.0
GeQD	0.0040	4.55	0.67	0.08	0.28	16.0
GeOx	0.0020	2.25	5.70	0.16	0.16	12.0
GeQD	0.0040	4.55	0.67	0.08	0.28	16.0
GeOx	0.0010	2.25	5.70	0.16	0.16	12.0
p-Si(1.0e16)	0.5000	4.15	1.12	0.19	0.49	11.9

Table 3.5. Parameters used for the Simulation of Ge QDC NVM with $HfAlO_2$ Layers

3.5. References

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CHAPTER 4

Simulation of Quantum Dot Superlattice using

Kronig-Penney Model

4.1. Multistate I_D-V_G Characteristics

This section describes quantum simulations, empirical I-V models for multiple energy mini-bands. Quantum simulations of Ge QDC FET (Figure 1.2a) have been carried out. Figure 4.1 shows the charge density in QDC transport channel as a function of V_G (or Fermi level) [1]. If V_G (or Fermi level) increases, the charge density in the mini-band increases and saturates. If V_G (or Fermi level) increases more, the charge density in the next mini-band also increases and saturates. Thus, the quantum transport model explains the participation of various mini-energy bands resulting in step like characteristics. Figure 4.2 shows I_D-V_D characteristics at different V_G [1]. The drain current I_D in a QDC FET depends on the number of conducting energy mini-bands, which depends on the magnitude of V_{GS} and V_{DS} [1]. Higher mini-bands participate as V_G and V_D increase. Table 4.4 shows the parameters used for these simulations [1].

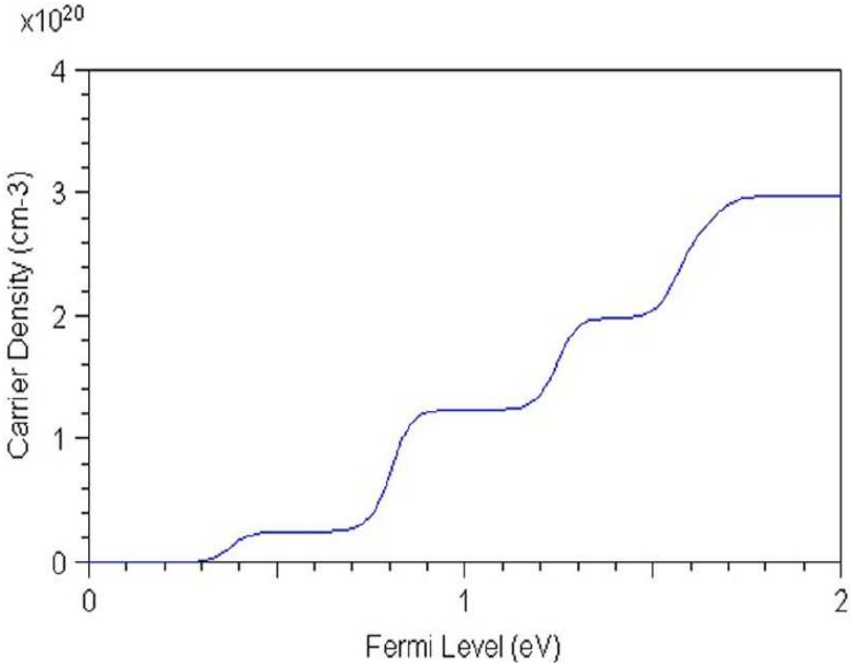


Figure 4.1. Charge Density in QDC Transport Channel as a function of V_G (or Fermi Level)

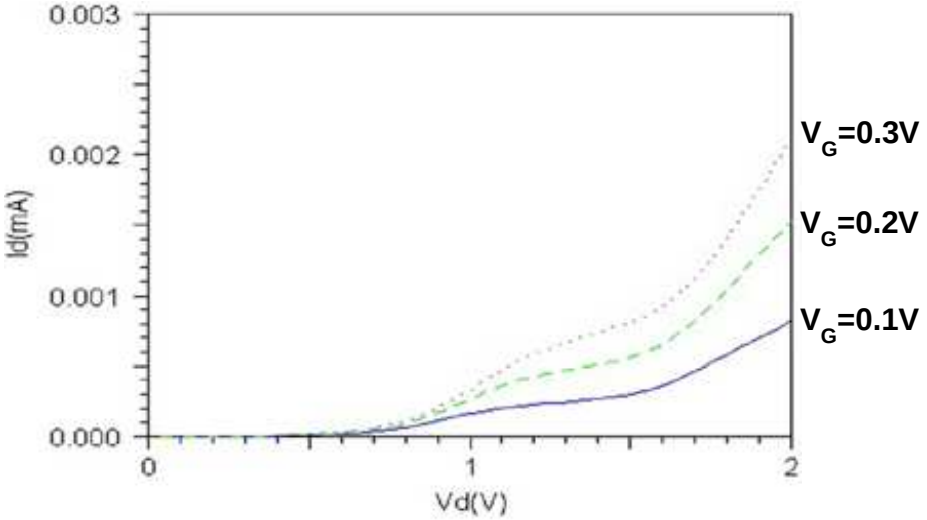


Figure 4.2. I_D-V_D Characteristics at different V_G

	Layer	Thickness (μm)	Χ (eV)	Eg (eV)	m_e	m_h	ε_r	N_d (cm^{-3})	N_a (cm^{-3})
1	ZnMgSSe	0.0020	2.05	4.0	0.16	0.50	8.5	0.0	0.0
2	GeOx	0.0010	2.25	5.70	0.16	0.16	4.4	0.0	0.0
3	Ge QD1	0.0030	4.55	0.67	0.08	0.28	16.0	0.0	0.0
4	GeOx	0.0020	2.25	5.70	0.16	0.16	4.4	0.0	0.0
5	Ge QD2	0.0030	4.55	0.67	0.08	0.28	16.0	0.0	0.0
6	GeOx	0.0020	2.25	5.70	0.16	0.16	4.4	0.0	0.0
7	Ge QD3	0.0050	4.55	0.67	0.08	0.28	16.0	0.0	0.0
8	GeOx	0.0010	2.25	5.70	0.16	0.16	4.4	0.0	0.0
9	ZnMgSSe	0.0050	2.05	4.00	0.16	0.50	8.5	0.0	0.0
10	Si	0.1000	4.15	1.12	0.19	0.49	11.9	0.0	1.0×10^{15}

Table 4.1. Simulation Parameters for Multistate I-V Characteristics

4.2. Quantum Simulation of Current Transport in QDC

4.2.1. Simulation Tools

4.2.1.1. Empirical Equation for I_D-V_D Characteristics

The following two published empirical equations were converted to the VisSim block diagrams to simulate the I_D-V_D and I_D-V_G characteristics of QDC and QDG-QDC FETs [2];

$$I_D = \left(\frac{W}{L}\right) C_o'' \ \mu_n \left[\sum_{i=0}^{m}\sum_{j=0}^{n}\left\{V_G - \left(V_{THi} + \Delta V_{THi}\right) - \frac{1}{2}V_{DSj}\right\} V_{DSj}\right] \quad (4.1)$$

$$I_D(sat) = \frac{1}{2}\left(\frac{W}{L}\right) C_o'' \ \mu_n \left[\sum_{i=0}^{m}\left\{V_G - \left(V_{THi} + \Delta V_{THi}\right)\right\}\right]^2 \quad (4.2)$$

4.2.1.2. VisSim Simulation

The following four major steps were taken to obtain the I_D-V_G and I_D-V_D characteristics of QDG-QDC FET fabricated in 2012. First, the I_D-V_D characteristics were obtained from the fundamental empirical equations 1 and 2, and the VisSim program is shown in Figure 4.3. This particular VisSim program was simulated for V_G of 2V. Second, the VisSim program was simulated with different V_G voltages until it covers the entire V_G range for the I_D-V_G characteristics. Figure 4.13 shows the results of this procedure, and V_G covers from -1V to 2V. The two-dimensional presentation of Figure 4.13 is shown in Figure 4.14. Third, the I_D-V_G characteristics were derived from Figure 4.13 by swapping the V_G axis and the V_D axis by using the "Switch Row/Colum" function of the Excel program, and Figure 4.15 shows the results of this procedure. Please note that Figure 4.13 and Figure 4.15 contain the exactly identical data. But Figure 4.13 has the V_D for the horizontal axis, and Figure 4.15 has the V_G for the horizontal axis. The two-dimensional presentation of Figure 4.15 is shown in Figure 4.16. The characteristics of the V_D equal to 1.5V and 0.5V were extracted from Figure 4.16, and shown in Figure 4.17.

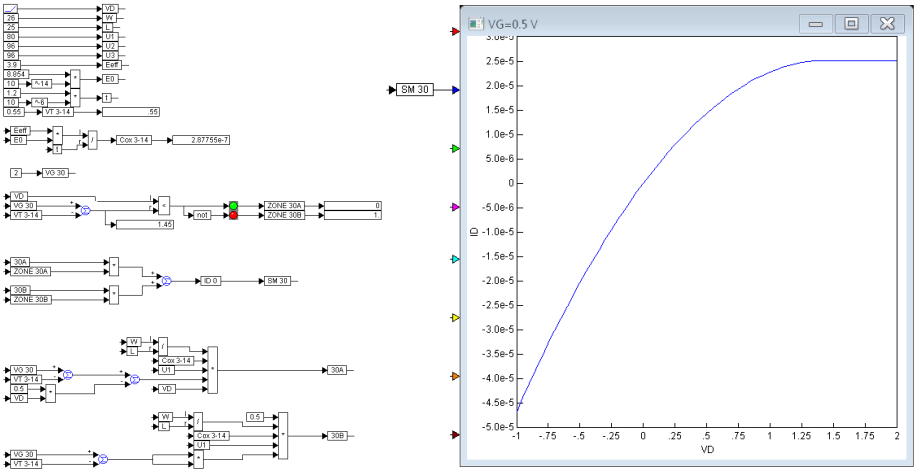


Figure 4.3. I_D-V_D VisSim Simulation of QDG-QDC FET, V_G=2V

4.2.1.3. Current Jump Factor

The idea of the current jump factor was originated from the first QDG-QDC FET in 2009. The I_D-V_G characteristics are shown in Figure 4.4, and the first current peak B-1 had very peculiar current jump characteristics [3]. The current jump factor is defined as follows;

$$Current\ Jump\ Factor\,(2009) = \frac{Jump\ Current}{Drain\ Current} = \frac{5.178\times10^{-6}}{1.10126\times10^{-6}} \cong 0.511 \quad (4.3)$$

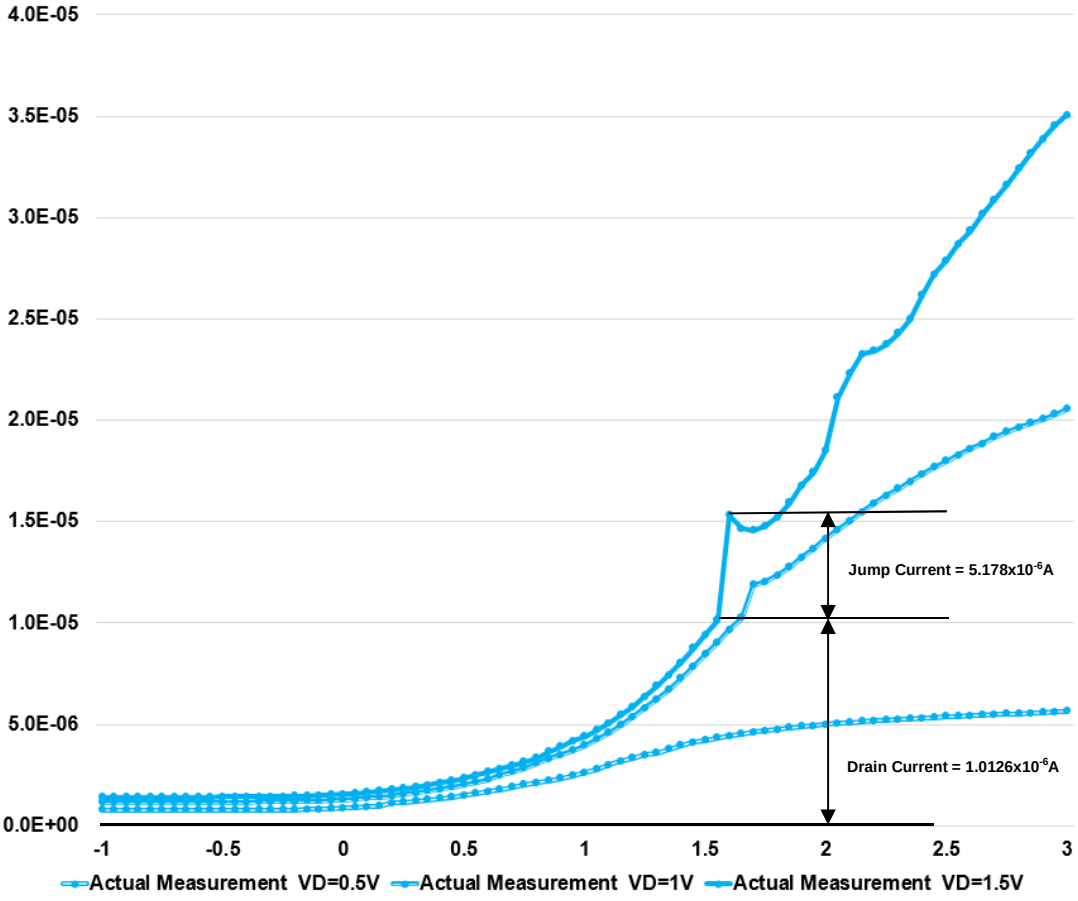


Figure 4.4. Design of Jump Characteristic

4.2.2 Four State Simulation: QDG-QDC FET in 2009

4.2.2.1. Parameters

The parameters for the simulation are stated as follows;

$W = 0.544\mu m\ (50\mu m)^*$

$L = 4\mu m$

$v_1 = 80 cm^2 V^{-1} s^{-1}\ (\text{State } 1)$

$v_2 = 1.2 \times v_1 = 96 cm^2 V^{-1} s^{-1}\ (\text{State } 2)$

$v_3 = 1.2 \times v_1 = 96 cm^2 V^{-1} s^{-1}\ (\text{State } 3)$

$\varepsilon_{eff} = 12\ (\text{Silicon Quantum Dot})$

$\varepsilon_0 = 8.854 \times 10^{-14} F/cm$

$t = 1.2 \times 10^{-8} m = 1.2 \times 10^{-6} cm$

4.2.2.2. Width*

The right side 6th device (R6) of the Yale mask was used to fabricate this device. The W/L ratio was 50/4. But this W/L ratio was modified to 0.544/4 to produce the equivalent drain current flow.

4.2.2.3. Capacitance

The capacitance of the oxide layer was determined using the following equation;

$$C_{ox} = \frac{e_{eff} * e_0}{t} = \frac{12 * (8.854 * 10^{-14})}{120 * 10^{-8}} = 8.854 * 10^{-7}\ \text{F/cm}^2 \qquad (4.4)$$

4.2.2.4. Threshold Voltage

The actual measurement of I_D-V_G characteristics are shown in Figure 4.5, and the current peak information is shown in Table 4.2 to determine threshold voltages.

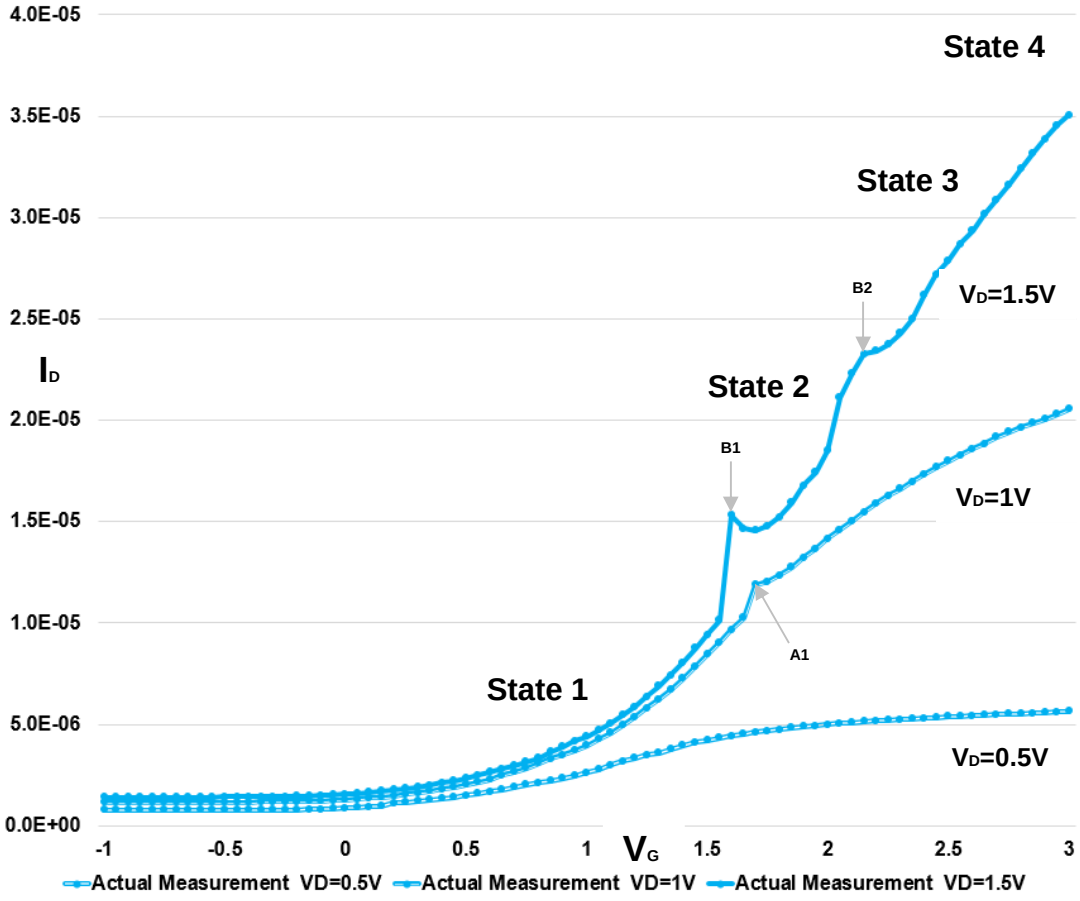


Figure 4.5. Threshold Voltage for Three State Simulation

Current Label	I_D (µA)	V_D (V)	V_G (V)	V_{TH} (V)
I_{A1}	11.88	1	1.7	1.7
I_{B1}	15.304	1.5	1.6	1.6
I_{B2}	23.26	1.5	2.15	2.15

Table 4.2. Peak I_D Curren Information of QDG-QDC FET (2009)

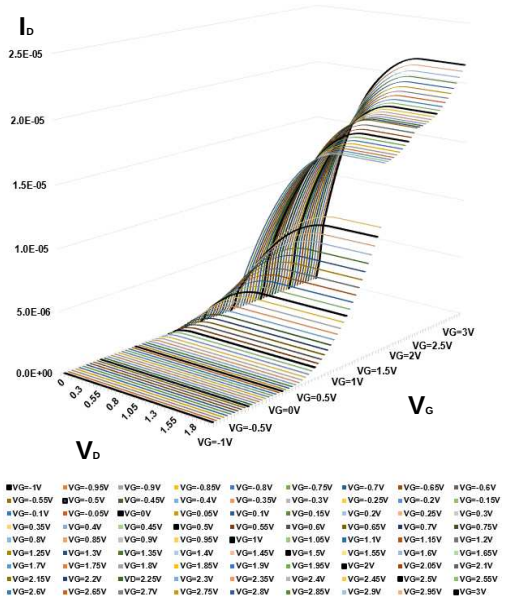


Figure 4.6. 3-D I_D-V_D Simulation

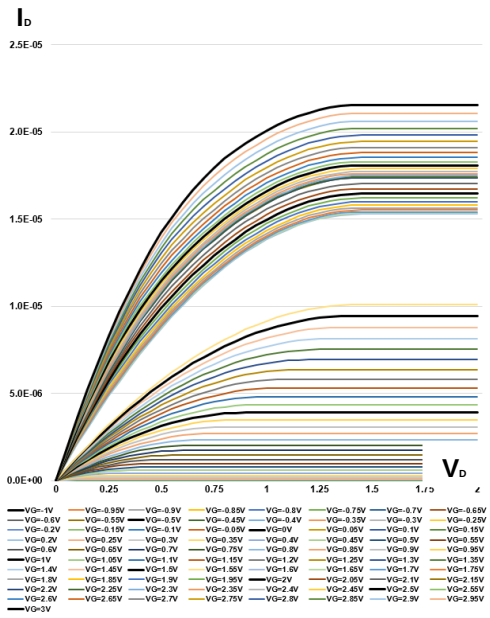


Figure 4.7. 2-D I_D-V_D Simulation

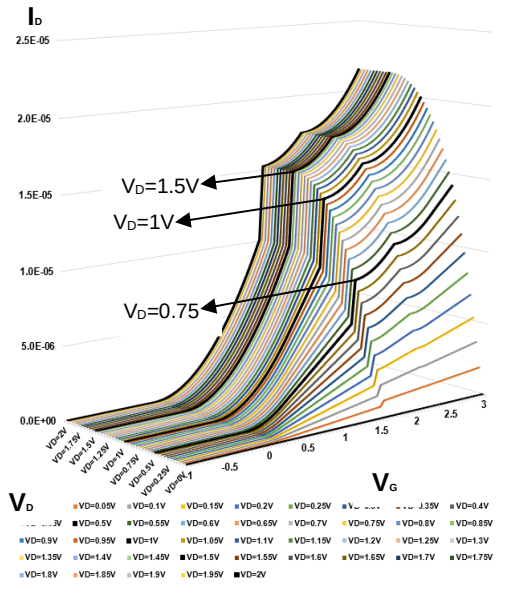


Figure 4.8. 3-D I_D-V_G Simulation

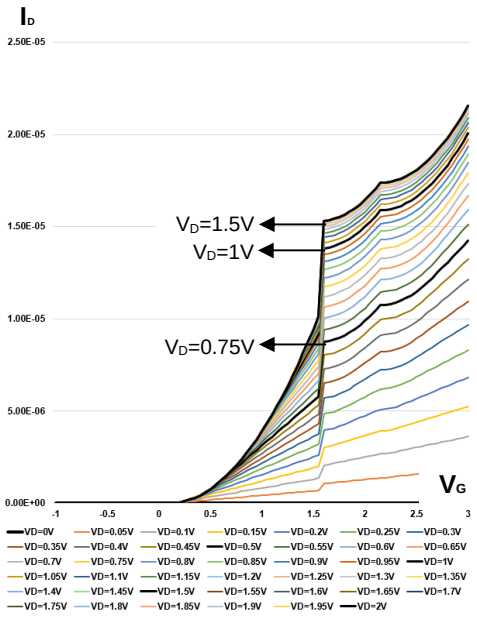


Figure 4.9. 2-D I_D-V_G Simulation

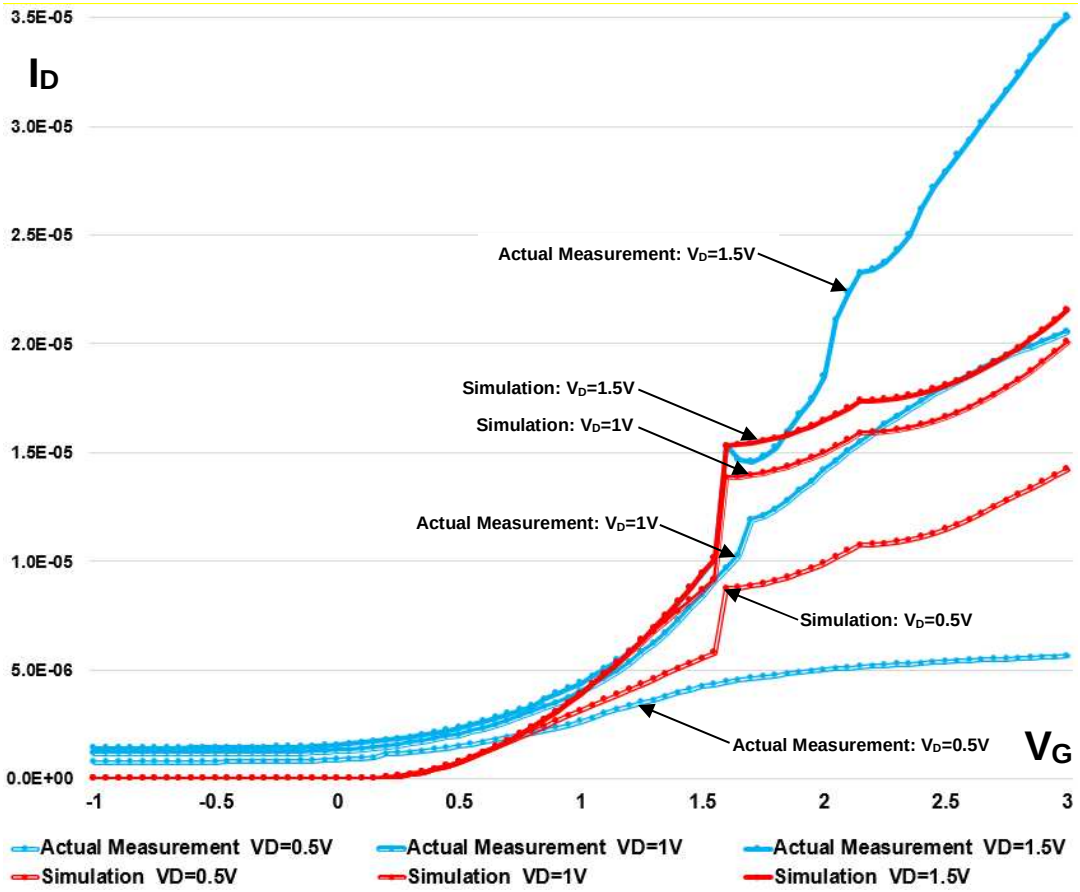


Figure 4.10. Actual Measurement and Simulation

4.2.2.5. Actual Measurement and Simulation

When V_D voltages are equal to 0.5 volts, 1 volt and 1.5 volts, the actual measurements and the simulations of I_D-V_G characteristics are two-dimensionally shown in Figure 4.10. When V_D is 1.5 volts, the simulation is very close to the actual measurement before the major current peak. Right after the major current peak, the actual measurement once decreased, and then increased exceeding the simulation to form the second current peak without the current jump characteristics.

4.2.3. Four State Simulation: QDG-QDC FET in 2012

4.2.3.1. Parameters

The parameters for the simulation are stated as follows;

$W = 220\mu m\ (60\mu m)^*$

$L = 60\mu m$

$v_1 = 80 cm^2 V^{-1} s^{-1}\ (\text{State } 1)$

$v_2 = 1.2 \times v_1 = 96 cm^2 V^{-1} s^{-1}\ (\text{State } 2)$

$v_3 = 1.2 \times v_1 = 96 cm^2 V^{-1} s^{-1}\ (\text{State } 3)$

$\varepsilon_{eff} = 12\ (\text{Silicon Quantum Dot})$

$\varepsilon_0 = 8.854 \times 10^{-14} F/cm$

$t = 1.2 \times 10^{-8} m = 1.2 \times 10^{-6} cm$

4.2.3.2. Width*

The actual width of the Yale mask was 60µm as shown in Table 2.4. But it was expanded to 220µm to match two current peak values for both actual measurement and simulation when V_D was equal to 1.5 volts, and V_G was equal to 0.55 volts.

4.2.3.3. Capacitance

The capacitance of the oxide layer was determined using the following equation;

$$C_{ox} = \frac{e_{eff} * e_0}{t} = \frac{12 * (8.854 * 10^{-14})}{120 * 10^{-8}} = 8.854 * 10^{-7}\ F/cm^2 \qquad (4.4)$$

4.2.3.4. Threshold Voltagea

The actual measurement of I_D-V_G characteristics are shown in Figure 4.11 and Figure 4.12 in order to determine threshold voltages. Because a minor current peak (B1) was found at V_G was equal to -0.45 V, there were three peaks when V_D was equal to 1.5V.

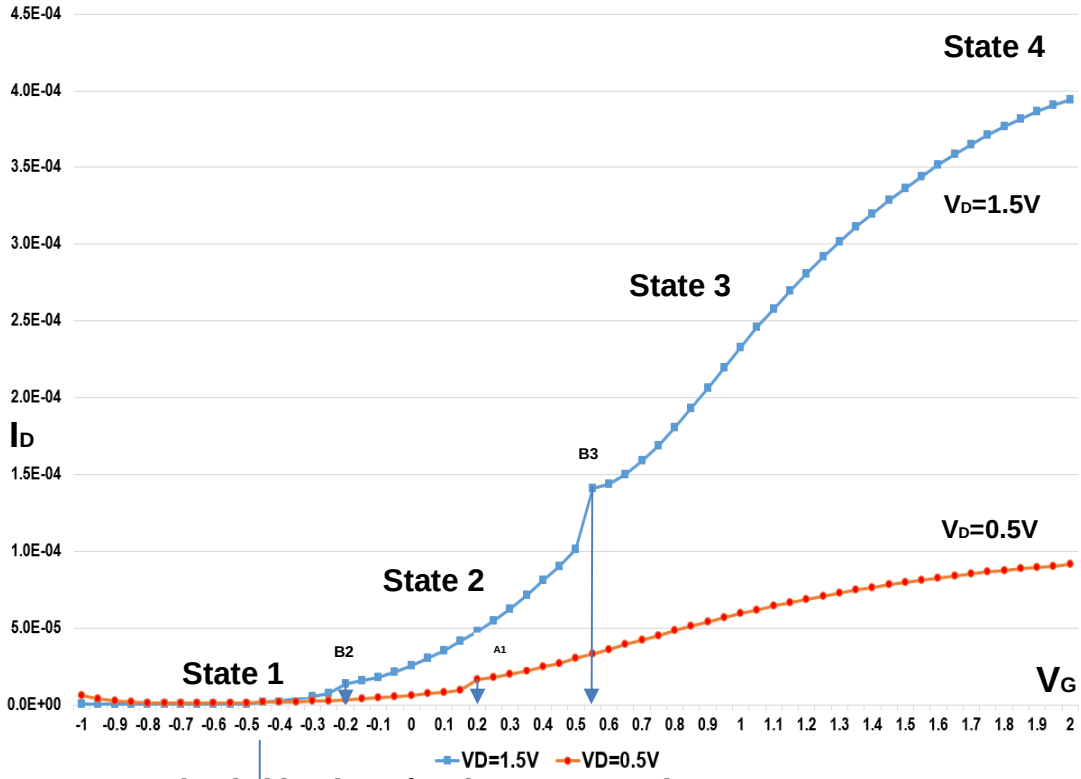


Figure 4.11. Threshold Voltage for Three State Simulation 1

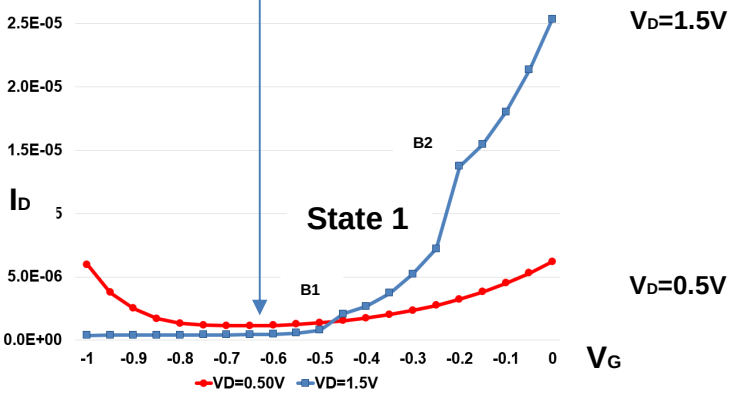


Figure 4.12. Threshold Voltage for Three State Simulation 2

Current Label	**I_D (µA)**	**V_D (V)**	**V_G (V)**	**V_{TH} (V)**
I_{A1}	16.555	0.5	0.20 V	0.20 V
I_{B1}	2.0835	1.5	-0.45 V	-0.45 V
I_{B2}	13.745	1.5	-0.20 V	-0.20 V
I_{B3}	140.80	1.5	0.55 V	0.55 V

Table 4.3. Peak I_D Current Information of QDG-QDC FET (2012)

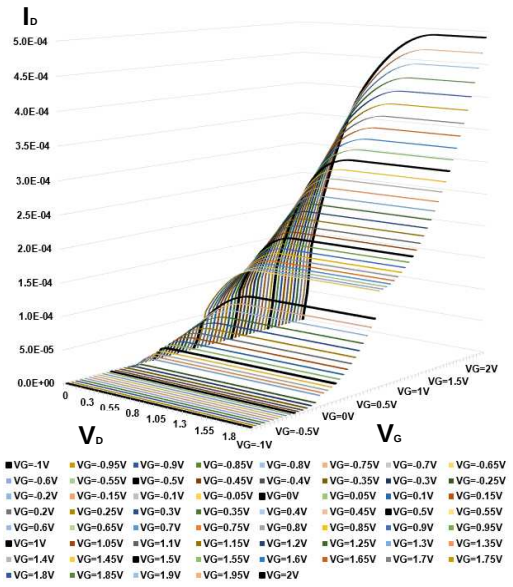


Fig 4.13. 3-D I_D-V_D Simulation

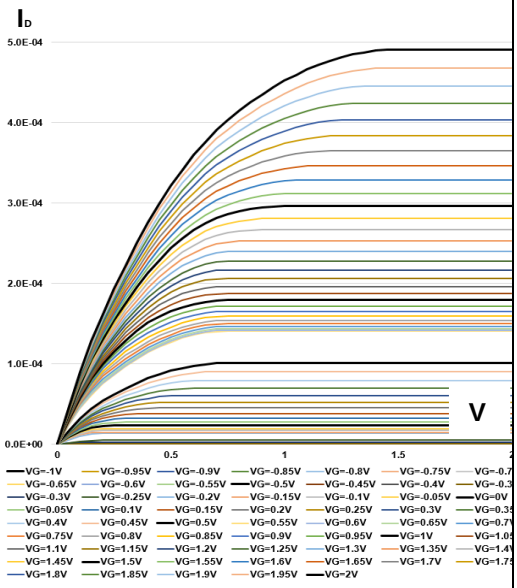


Figure 4.14. 2-D I_D-V_D Simulation

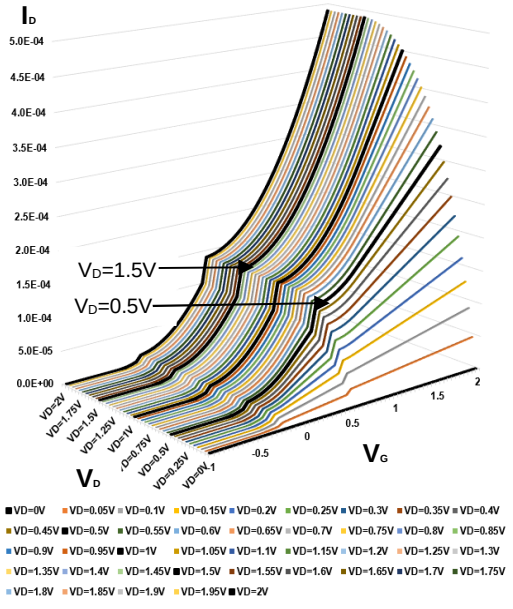


Figure 4.15. 3-D I_D-V_G Simulation

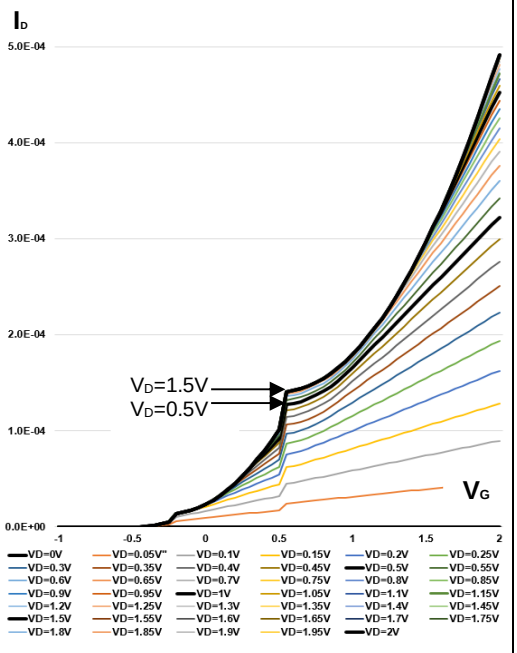


Figure 4.16. 2-D I_D-V_G Simulation

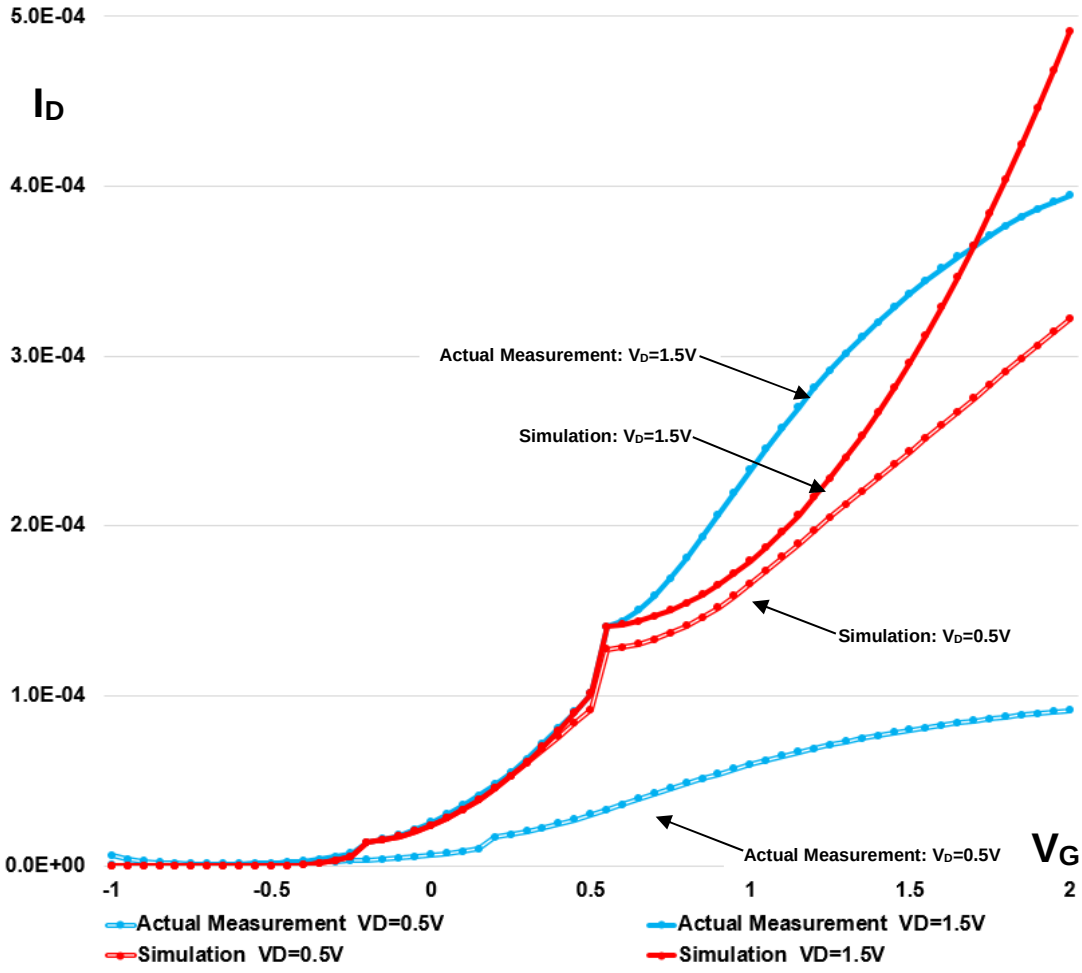


Figure 4.17. Actual Measurement and Simulation

4.2.3.5. Actual Measurement and Simulation

When V_D voltages are equal to 0.5 volts and 1.5 volts, the actual measurements and the simulations of I_D-V_G characteristics are two-dimensionally shown in Figure 4.17. When V_D is 1.5 volts, the simulation is very close to the actual measurement before the major current peak. After the major current peak, the actual measurement has the shape of concave down. But the simulation is keeping on increasing, and has the shape of concave up.

4.2.4 Three State Simulation: QDC FET in 2014

4.2.4.1. Parameter

The parameters for the simulation are stated as follows;

$W = 4.36\mu m\ (30\mu m)^*$
$L = 18\mu m$
$v_1 = 80 cm^2 V^{-1} s^{-1}\ (\text{State 1})$
$v_2 = 1.2 \times v_1 = 96 cm^2 V^{-1} s^{-1}\ (\text{State 2})$
$\varepsilon_{eff} = 12\ (\text{Silicon Quantum Dot})$
$\varepsilon_0 = 8.854 \times 10^{-14} F/cm$
$t = 1.2 \times 10^{-8} m = 1.2 \times 10^{-6} cm$

4.2.4.2. Width*

The actual width of the sensor mask was 30µm. But the width was reduced to 4.36µm to match two current peak values for Simulation 1, and the width was reduced to 1.90µm to match two current peak values for Simulation 2.

4.2.4.3. Capacitance

The capacitance for the oxide layer was determined using the following equation which includes the permittivity of the silicon quantum dots, the permittivity of the free space, and the thickness of two silicon quantum dot layers.

$$C_{ox} = \frac{e_{eff} * e_0}{t} = \frac{12 * (8.854 * 10^{-14})}{120 * 10^{-8}} = 8.854 * 10^{-7}\ \text{F/cm}^2 \qquad (4.4)$$

4.2.4.4. Threshold Voltage

The actual measurement of I_D-V_G characteristics are shown in Figure 4.18, Figure 4.19, and Figure 4.20 in order to determine threshold voltages.

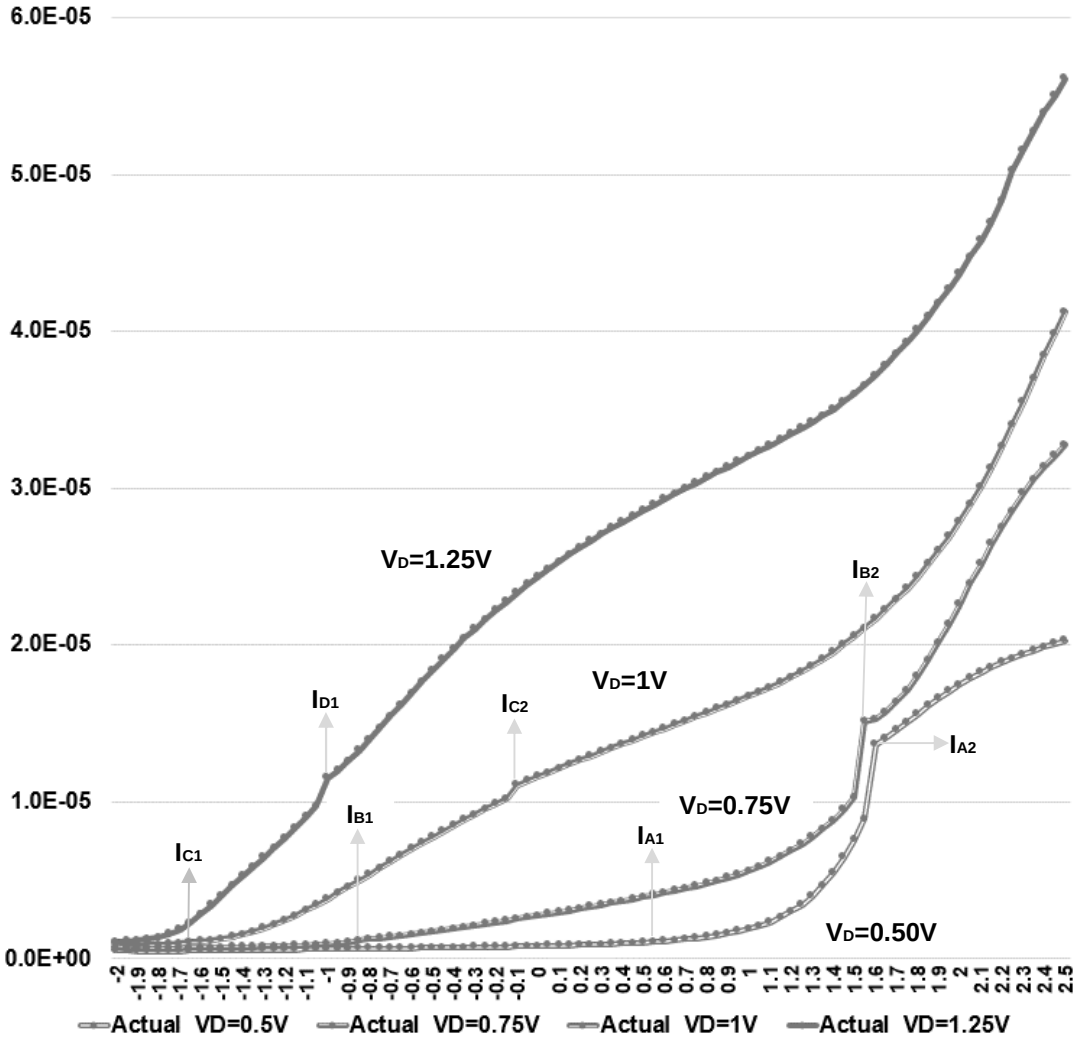


Figure 4.18. Current Peaks for QDC FET (2014)

Peak Label	**I_D (µA)**	**V_D (V)**	**V_G (V)**	**V_{TH} (V)**
I_{A1}	1.095	0.50	0.55 V	0.55 V
I_{A2}	13.64	0.50	1.60V	1.60 V
I_{B1}	1.1815	0.75	-0.85 V	-0.85 V
I_{B2}	15.125	0.75	1.55 V	1.55 V
I_{C1}	1.0725	1.00	-1.65	-1.65
I_{C2}	11.075	1.00	-0.10 V	-0.10 V
I_{D1}	11.53	1.25	-1.00 V	-1.00 V

Table 4.4. Peak I_D Current Information of QDC FET (2014)

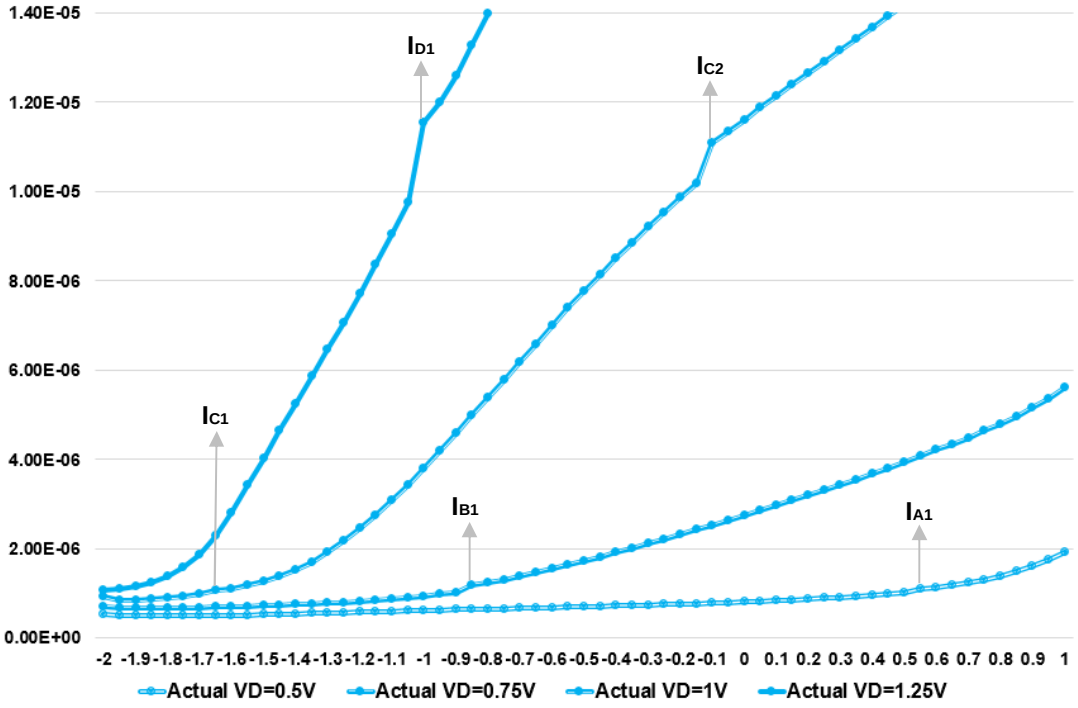


Figure 4.19. Current Peaks for QDC FET (2014)

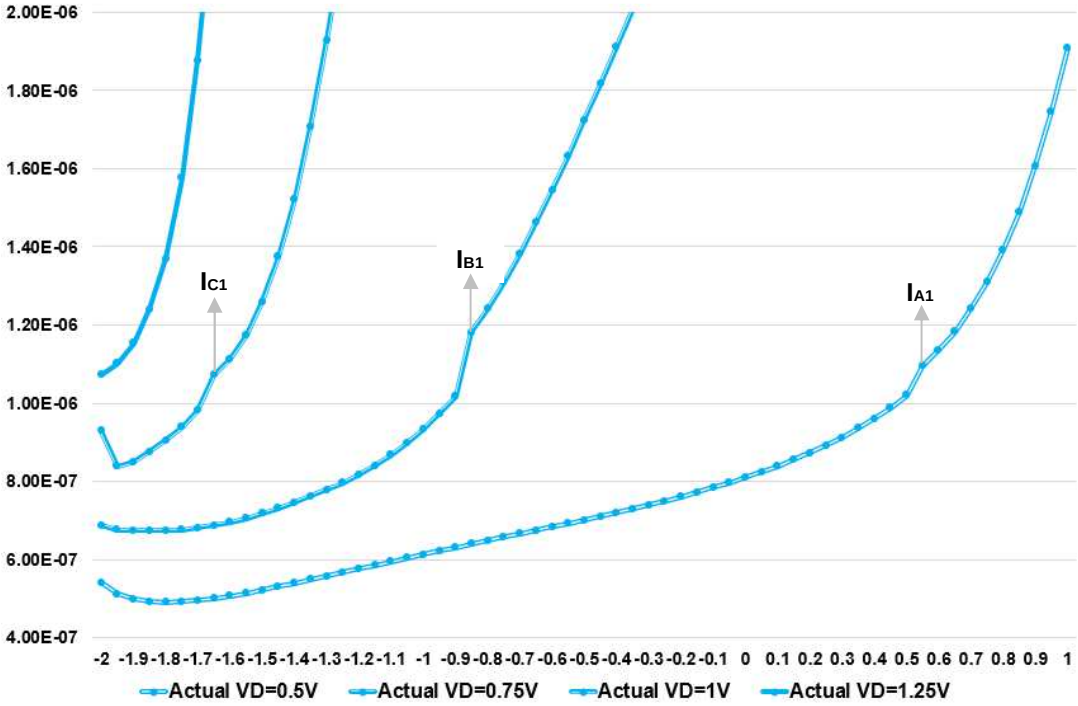


Figure 4.20. Current Peaks for QDC FET (2014)

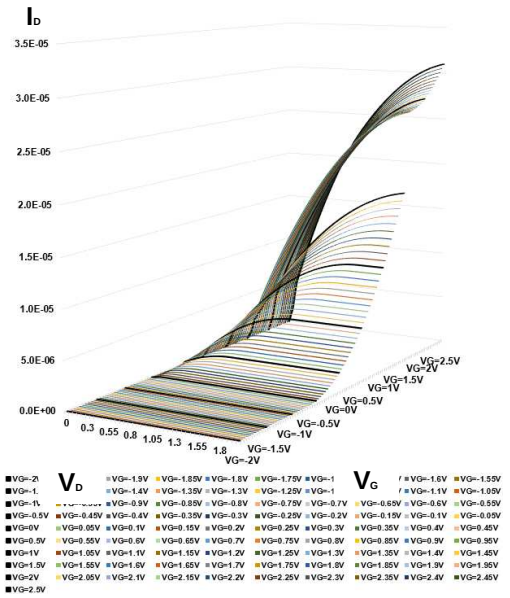


Figure 4.21. 3-D I_D-V_D Simulation

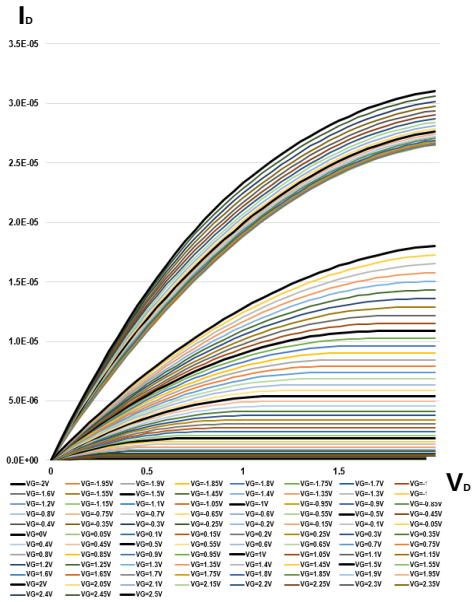


Figure 4.22. 2-D I_D-V_D Simulation

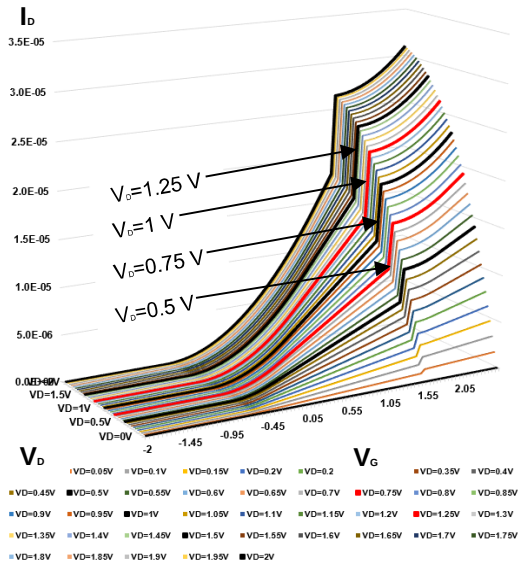


Figure 4.23. 3-D I_D-V_G Simulation

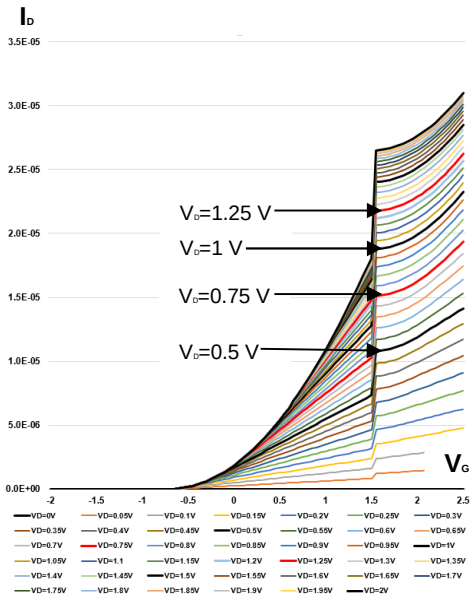


Figure 4.24. 2-D I_D-V_G Simulation

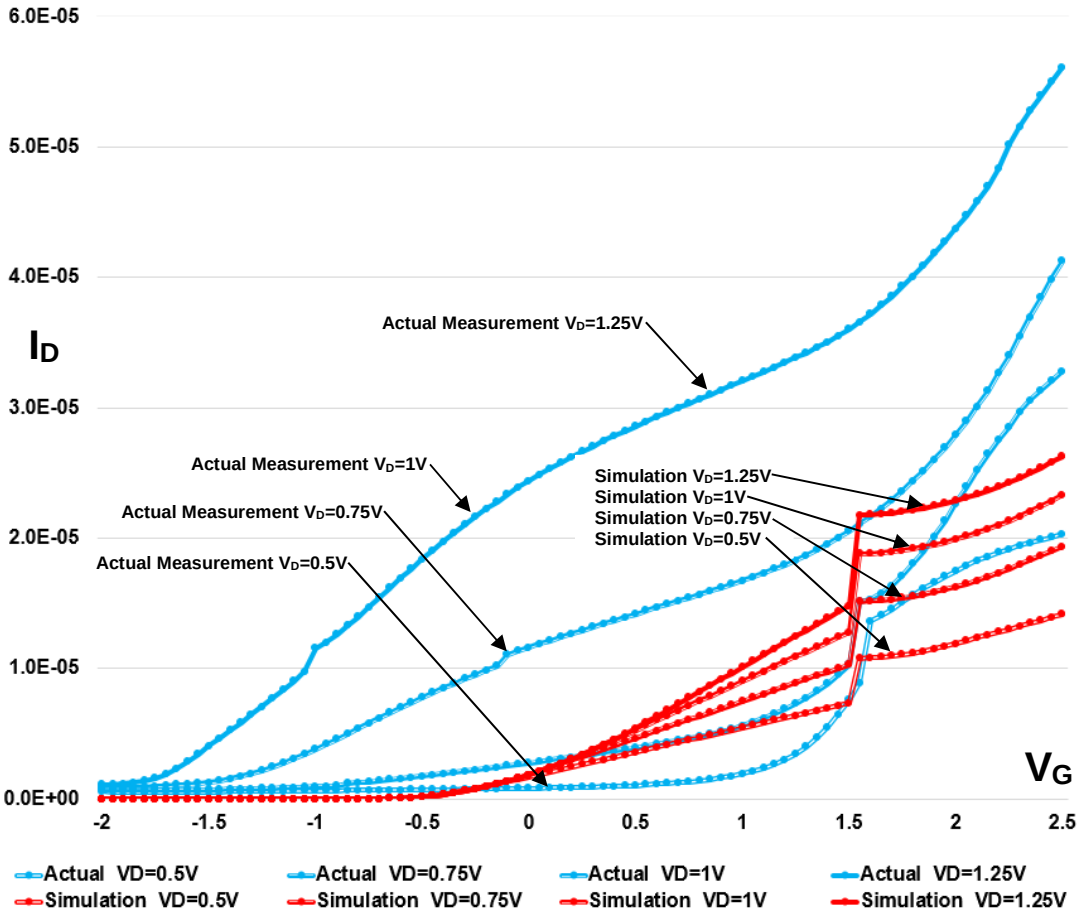


Figure 4.25. Actual Measurement and Simulation of I_D-V_G Characteristics

4.2.4.5. Actual Measurement and Simulation

When V_D was equal to 0.5, 0.75, 1 and 1.25 volts, the actual measurements and simulations of the I_D-V_G characteristics are shown in Figure 4.25. When the V_D voltages were 0.5 volts and 0.75 volts, actual measurements and simulation results were fairly close. When the V_D voltages were 1 volt and 1.25 volts, actual measurements and simulation results were totally different. These two groups were independent, and showed totally different I_D-V_G characteristics.

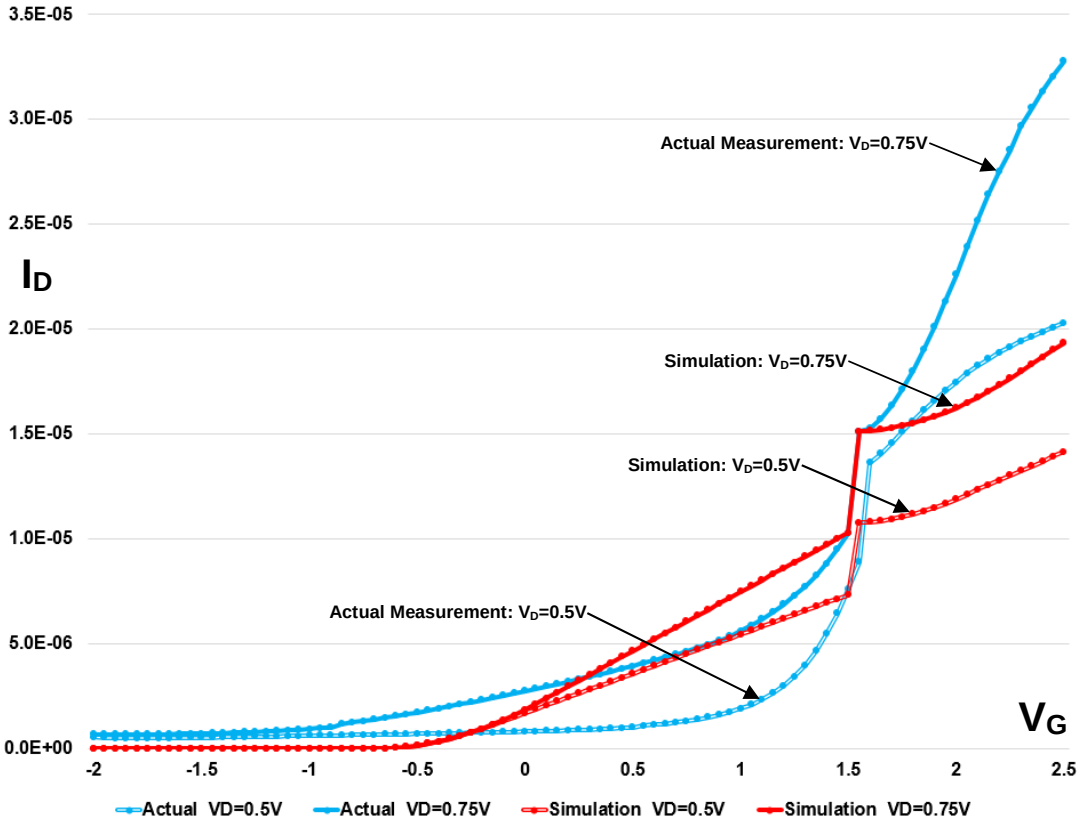


Figure 4.26. Actual Measurement and Simulation of I_D-V_G Characteristics

In order to closely investigate the difference between the actual measurements and simulation results when the V_D voltages are 0.5 volts and 0.75 volts, these two current lines were extracted from Figure 4.25, and are shown in Figure 4.26. Just before the major current peaks, the actual measurement lines and simulation lines have huge leaps. But the actual measurement lines are concave up, and the simulation lines are almost straight. On the other hand, just after the major current peaks, the actual measurement lines are concave down, and the simulation lines are concave up.

4.2.5. Conclusion

For QDG-QDC FET in 2009 and QDG-QDC FET in 2012, their characteristics were considered as the four state (OFF, 'I_1', 'I_2', ON) as Section 2.3.3 of this thesis. For QDC FET in 2014, the the actual measurement of I_D-V_G and the simulation of two empirical current equations are shown in Figure 4.23, and both plots show a distinct current peak when the V_D voltage was equal to 0.5 volts and 0.75 volts. A current peak of 13.6μA was observed at the V_G voltages of 1.60 volts when the V_D voltage was equal to 0.5 volts. On the other hand, a current peak of 15.1μA was observed at the V_G voltages of 1.55 volts when the V_D voltage was equal to 0.75 volts. These two I_D current peak differentiated the first state and the second state, and the current saturation state was considered as the third state. Therefore, the characteristics of this QDC FET in 2014 were considered as the three state (OFF, 'I_1', ON). The multi-state FETs have advantages over the conventional FETs. For example, multi-state FETs are used for the multi-valued logic (MVL) in order to reduce the number of gates and transistors [4]. Therefore, they can reduce power dissipation in digital circuits.

4.3. Kronig and Penney Model for Quantum Dot Superlattice

We have used the Kronig and Pennney model to simulate a 3-dimentional cladded quantum dot array. As in bulk semiconductors, the Kronig and Penney model gives formation of energy mini-bands in a 3-dementional quantum dot superlattice (QDSL). We see formation of energy mini-bands in conduction and valence bands. In the quantum dot superlattice (QDSL), decreasing the barrier thickness and introducing more wells lead to the creation of a continuous band of states called the energy mini-band [5]. The Kronig and Penney model was used to determine locations and widths of the energy mini-bands, and the equation is expressed as follows [3,6];

$$P*\frac{\sin(\beta*a)}{\beta*a}+\cosh(\alpha*b)*\cos(\beta*a)=\cos(k*a) \qquad (4.5)$$

The simulation parameters are defined as follows;

$$i \equiv \text{SimulationVariable}; 0 < i < 10{,}000$$
$$\text{Pi} \equiv \pi = 3.14159265359 \text{ rad}$$
$$q \equiv \text{Fundanmental Charge} = 1.60217656535 \times 10^{-19} \text{ C}$$
$$\hbar \equiv \text{Reduced Plank's Constant} = 1.05457172647 \times 10^{-34} \text{ J - s}$$
$$m_0 \equiv \text{Rest Mass of Electron} = 9.1093821545 \times 10^{-31} \text{ kg}$$
$$m_B \equiv \text{Electron Effective Mass in Barrier} = 0.3$$
$$m_W \equiv \text{Electron Effective Mass in Well} = 0.19$$
$$V_0 \equiv \text{Well Depth} = 3.4\text{V}$$

The VisSim program for the simulation parameters is shown in Figure 4.27.

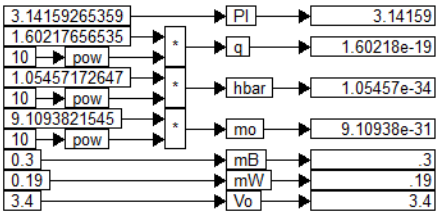


Figure 4.27. Simulation Parameters

4.3.1. Variables

Five variables in the VisSim computer program are stated as follows;

1. Simulation Variable: k*a
2. Electron Energy: E
3. Electron Momentum: P
4. Wave Amplitude Parameter of the Barrier: α
5. Wave Amplitude Parameter of the Well: β

The definitions for these five variables are stated as follows;

$$k \equiv \text{Wave Number} \tag{4.6}$$

$$E \equiv \text{Total Energy of the Electron} = \frac{\hbar^2 * (k * a)^2}{2 * a^2 * mW * mo * q} \tag{4.7}$$

$$P \equiv \text{Particle Momentum} = \left(\alpha - \frac{\beta^2}{\alpha} \right) * \frac{a}{2} * \sinh(\alpha * b) \tag{4.8}$$

$$\alpha \equiv \text{Wave Amplitude Parameter for the Barrier} = \frac{\sqrt{2 * mB * mo * q * (Vo - E)}}{\hbar} \tag{4.9}$$

$$\beta \equiv \text{Wave Amplitude Parameter for the Well} = \frac{\sqrt{2 * mW * mo * E * q}}{\hbar} \tag{4.10}$$

$Vo \equiv$ Well Depth = 3.4eV,
$a \equiv$ Dot Diameter; = 4nm,
$b \equiv$ Barrier Width = 1nm
$mW \equiv$ Electron Effective Mass in the Well = 0.19
$mB \equiv$ Electron Effective Mass in the Barrier = 0.3
$q \equiv$ Fundamental Charge = $1.60218 * 10^{-19}$ C
$\hbar \equiv$ Reduced Planck's Constant = $1.05458 * 10^{-34}$ Js
$mo \equiv$ Rest Mass of Electron = $9.1095 * 10^{-31}$ kg

4.3.1.1. Simulation Variable: k*a

The electron energy, the electron momentum, the wave amplitude parameter of the barrier, and the wave amplitude parameter of the well were simulated using the simulation variable for the horizontal axis. The simulation variable is defined as follows;

$k \equiv$ Wave Number

$a \equiv$ Quantum Dot Diameter

$$k * a = -3 * \pi + 6 * \pi * \frac{i}{10{,}000} \qquad 0 \le i \le 10{,}000 \qquad -3 * \pi \le k * a \le 3 * \pi \qquad (4.11)$$

The VisSim program for the simulation horizontal variable is shown in Figure 4.28.

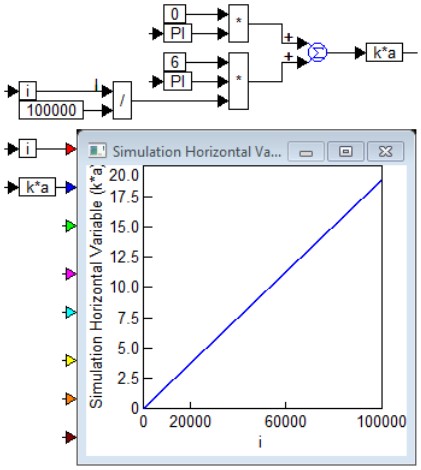


Figure 4.28. Simulation Variable: k*a

4.3.1.2. Total Energy of Electron: E

The total energy of the electron, E is expressed as follows;

$$E \equiv \text{Total Energy of the Electron} = \frac{\hbar^2 * (k * a)^2}{2 * a^2 * mW * mo * q} \tag{4.7}$$

$$x = -3 * \pi + \frac{6 * i * \pi}{1000}$$

$$\hbar \equiv \text{Reduced Planck Constant} = 1.05457 * 10^{-34}\ J * s/\text{radian}$$

$$a \equiv \text{Quantum Dot Diameter} = 4 * 10^{-9}\ m$$

$$mW \equiv \text{Electron Effective Mass in Well} = 0.19$$

$$mo \equiv \text{Rest Mass of Electron} = 9.1095 * 10^{-31}\ \text{kg}$$

$$q \equiv \text{Fundamental Charge} = 1.60218 * 10^{-19}\ C$$

The simulation for the total energy of the electron, E is shown in Figure 29.

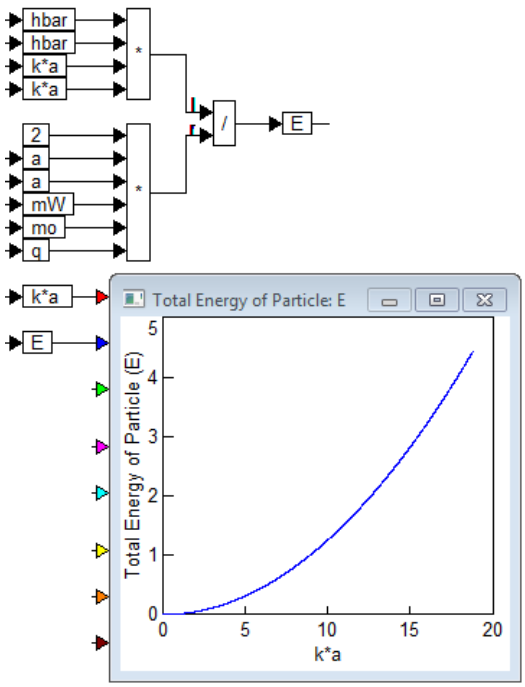
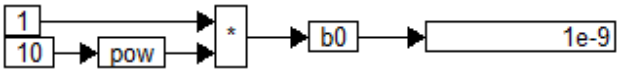


Figure 29. Total Energy of the Electron (E)

4.3.1.3. Electron Momentum: P

Define the Barrier Width: b=1nm



The value of P_0 (b=1nm) is expressed as follows;

$$P_0 = \left(\alpha - \frac{\beta^2}{\alpha}\right) * \left(\frac{a}{2}\right) * \sinh(\alpha * b_0) \qquad (4.8)$$

$$\alpha = \frac{\sqrt{2 * mB * mo * q * (V_0 - E)}}{\hbar} \qquad \beta = \frac{\sqrt{2 * mW * mo * E * q}}{\hbar}$$

$$a \equiv \text{Quantum Dot Diameter} = 4 * 10^{-9}\,\text{m}$$

$$b_0 \equiv \text{Barrier Width} = 1\,\text{nm} = 1 * 10^{-9}\,\text{m}$$

The VisSim program for the particle momentum, p is shown in Figure 4.30.

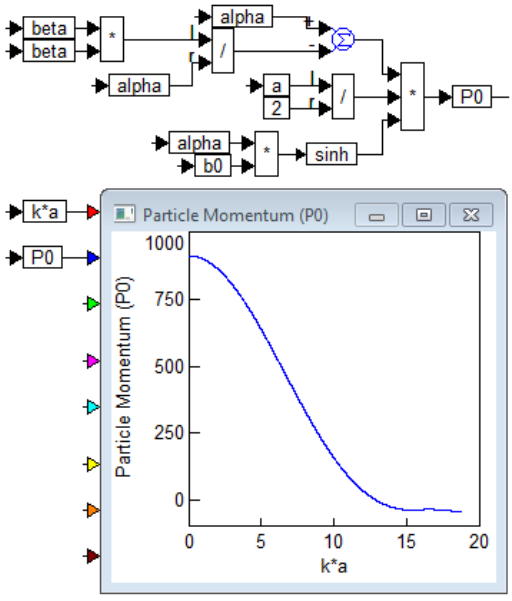


Figure 4.30. Particle Momentum (P_0)

4.3.1.4. Wave Amplitude Parameter of the Barrier: α

The value of α is expressed as follows;

$$\alpha = \frac{\sqrt{2 * mB * mo * q * (V_0 - E)}}{\hbar} \tag{4.9}$$

$$E \equiv \text{Total Energy of Electron} = \frac{(\hbar)^2 * (k * a)^2}{2 * a^2 * mW * mo * q}$$

$$\hbar \equiv \text{Planck Constant}/2\pi = 1.05458 * 10^{-34}\ J * s/\text{radian}$$

$$a \equiv \text{Quantum Dot Diameter} = 4 * 10^{-9}\ m$$

$$mo \equiv \text{Rest Mass of Electron} = 9.1095 * 10^{-31}\ kg$$

$$mB \equiv \text{Electron Effective Mass in Barrier} = 0.3$$

$$mW \equiv \text{Electron Effective Mass in Well} = 0.19$$

$$q \equiv \text{Fundamental Charge} = 1.60218 * 10^{-19}\ C$$

$$V_0 \equiv \text{Well Depth} = 3.4eV$$

The VisSim program for the wave amplitude parameter of the Barrier (α) is shown in Figure 4.31.

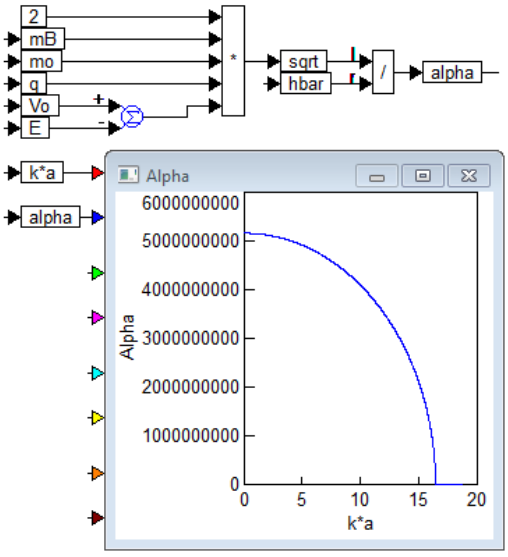


Figure 4.31. Wave Amplitude Parameter of the Barrier (α

4.3.1.5. Wave Amplitude Parameter of the Well: β

The value of β is expressed as follows;

$$\beta = \frac{\sqrt{2 * mW * mo * E * q}}{\hbar} \tag{4.10}$$

$$E \equiv \text{Total Energy of Electron} = \frac{(\hbar)^2 * (k * a)^2}{2 * a^2 * mW * mo * q}$$

$$\hbar \equiv \text{Reduced Planck Constant} = 1.05458 * 10^{-34}\ J * s/\text{radian}$$

$$a \equiv \text{Quantum Dot Diameter} = 4 * 10^{-9}\ m$$

$$mo \equiv \text{Rest Mass of Electron} = 9.1095 * 10^{-31}\ kg$$

$$mB \equiv \text{Electron Effective Mass in Barrier} = 0.3$$

$$mW \equiv \text{Electron Effective Mass in Well} = 0.19$$

$$q \equiv \text{Fundamental Charge} = 1.60218 * 10^{-19}\ C$$

The VisSim program for the wave amplitude parameter of the well α is shown in Figure 4.32.

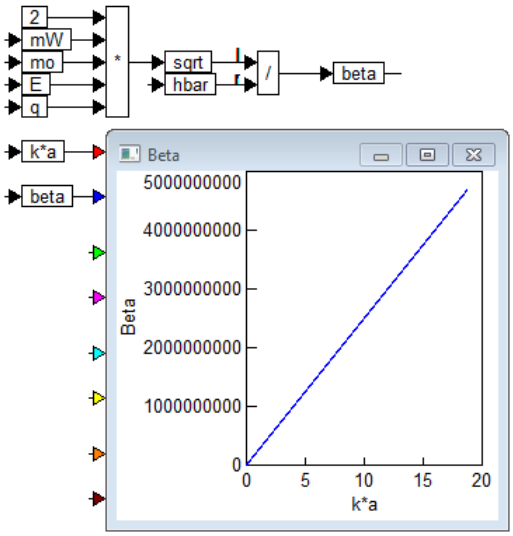


Figure 4.32. Wave Amplitude Parameter of the Well (β)

4.3.1.6. Left Hand Side: LHS

Five variables were applied for the left hand side (LHS);

$$LHS = P * \frac{\sin(\beta * a)}{\beta * a} + \cosh(\alpha * b) * \cos(\beta * a) \tag{4.11}$$

$$E = \frac{(\hbar)^2 * (k * a)^2}{2 * a^2 * mW * mo * q}$$

$$P = \left(\alpha - \frac{\beta^2}{\alpha}\right) * \left(\frac{a}{2}\right) * \sinh(\alpha * b)$$

$$\alpha = \frac{\sqrt{2 * mB * mo * q * (V_0 - E)}}{\hbar}$$

$$\beta = \frac{\sqrt{2 * mW * mo * E * q}}{\hbar}$$

The quantum dot diameter and the barrier width are determined as follows;

Quantum Dot Diameter; $a=4*10^{-9}m$

Barrier Width; $b=1*10^{-9}$ m

The VisSim program for the left hand side, LHS0 is shown in Figure 4.33.

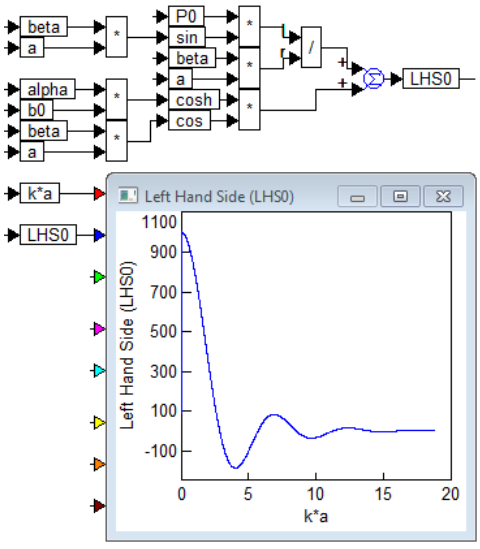


Figure 4.33. Left Hand Side: LHS

4.3.1.7. Allowable Energy Bands: E_0

The allowable energy bands (E_0) is expressed as follows;

$$\text{If } -1 \le \text{LHS}_0 \le 1$$

$$E_0 = E$$

The VisSim program for the allowable energy bands (E_0) is shown in Figure 4.34.

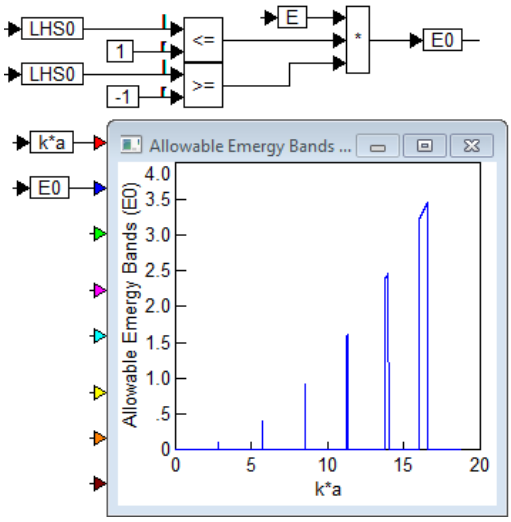


Figure 4.34. Allowable Energy Bands: E_0

4.3.1.8. Saving Data

Finally, the values of k*a and E_0 are saved in a data file.

The VisSim program for the saving data is shown in Figure 4.35.

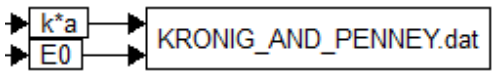


Figure 4.35. Saving Data

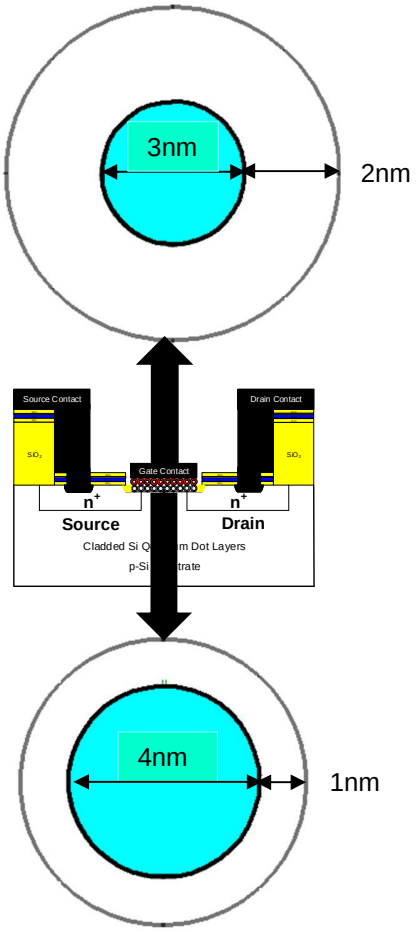
4.3.2. Simulation Results

4.3.2.1. Kronig and Penney Model

In order to determine the energy levels of mini-bands, the Kronig and Penney model was used. As seen in Equation 5, the right hand side (RHS) is the cosine function. Therefore, if the value of the left hand side (LHS) is more than -1 and less than 1, the equation is valid and there is a mini-band. This is the assumption of this simulation.

4.3.2.2. Combinational Level

In QDC FET, the silicon quantum dots were dry oxidized. So the core diameter and the barrier width were different according to the location of the silicon quantum dot. At the bottom surface, the core diameter was approximately 4nm, and the barrier width was approximately 1nm. When the silicon quantum dot was dry oxidized, the barrier width expanded, and the core diameter shrank. Therefore, at the top surface, the core diameter was approximately 3nm, and the barrier width was approximately 2nm. The barrier width was assumed to increase proportionally from the bottom surface to the top surface, and the core diameter was assumed to decrease proportionally from bottom surface to the top surface. The quantum dot layers were divided into eleven combinational levels from the bottom surface to the top surface, and the relationship between the combinational levels, the core diameters, and the barrier widths are shown in Table 4.5.



Barrier Width = 2nm

Core Diameter = 3nm

Barrier Width = 1nm

Core Diameter = 4nm

Figure 4.36. Core Diameter and Barrier Width of the Silicon Quantum Dot

Combination Number	1	2	3	4	5	6	6	8	9	10	11
Core	4.0	3.9	3.8	3.7	3.6	3.5	3.4	3.3	3.2	3.1	3.0
Barrier	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9	2.0
Total	6.0	6.1	6.2	6.3	6.4	6.5	6.6	6.7	6.8	6.9	7.0

Table 4.5. Core Diameter and Barrier Width Combinations of Silicon Quantum Dots

4.3.2.3. Simulation Results

The left hand side of the equation (LHS) is plotted using the eleven different combinational levels according to Table 4.4, and shown in Figure 4.37. This plot must be bounded between +1 and -1 to determine the allowable energy values to give the conditions for which Schrodinger's equation will have a solution. The intersections between LHS and the +1, -1 axis for Mini-band 1, 2, and 3 are shown in Figure 4.38. The intersections between LHS and the +1, -1 axis for Mini-band 4, 5, and 6 are shown in Figure 4.39.

4.3.2.4. Energy levels

From the intersection points of Figure 4.38 and Figure 4.39, the range of k*a was determined, and these values were transferred to Figure 4.40 "Relationship between Electron Energy (V) and k*a (radian)" to determine the energy levels of each mini-band. Finally, the electron energies (V) for mini-bands and core-barrier combinations are shown in Figure 4.41.

4.3.2.5. Conclusion

The left column of Figure 4.41 shows the total energy levels of the mini-bands, and there are only four mini-bands are observable. Therefore, the results clearly showed that there were only four mini-bands if the silicon quantum dots were dry oxidized. All mini-bands were combined together above the fourth mini-bands,

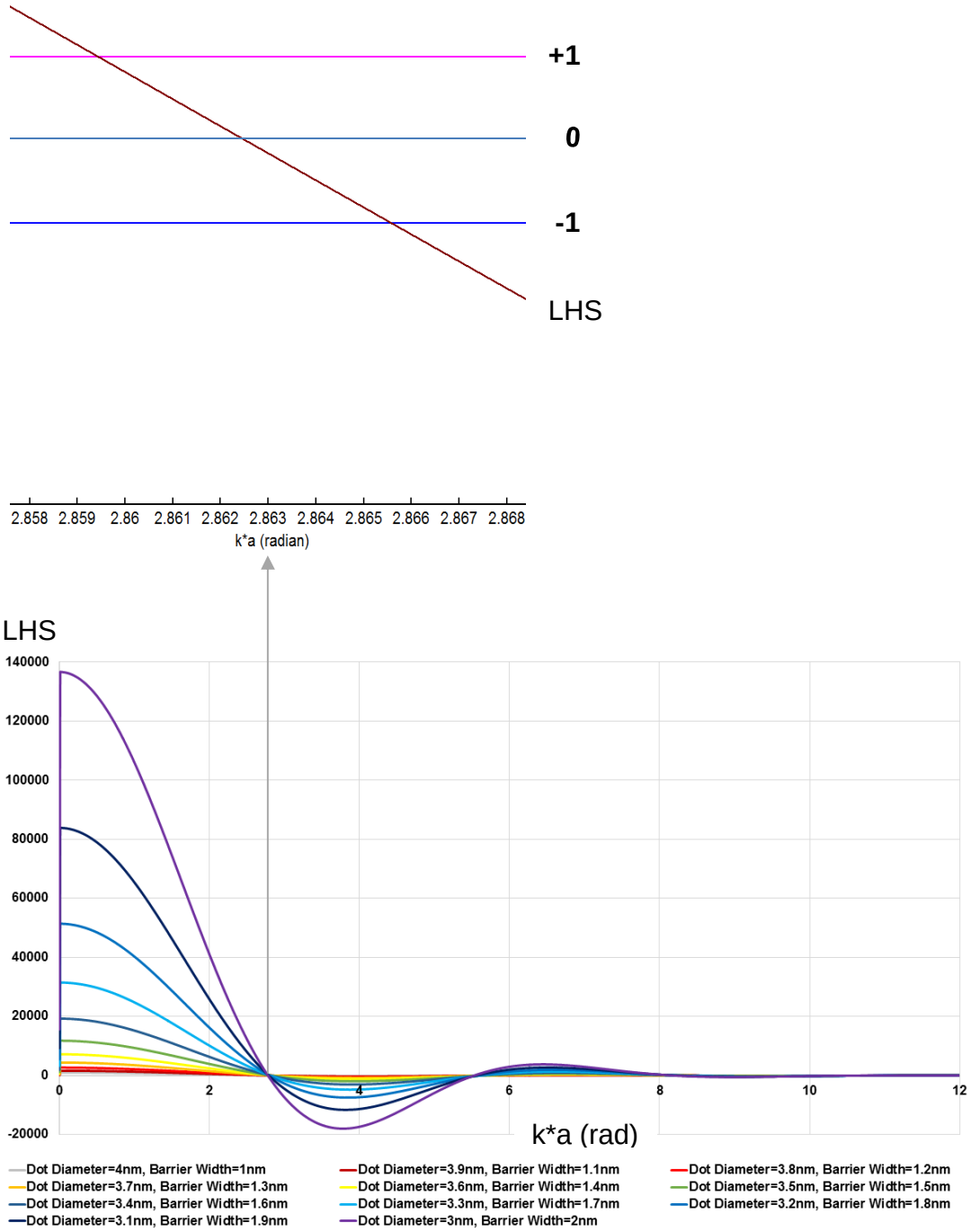


Figure 4.37. Simulation of left hand side (LHS) of the Equation

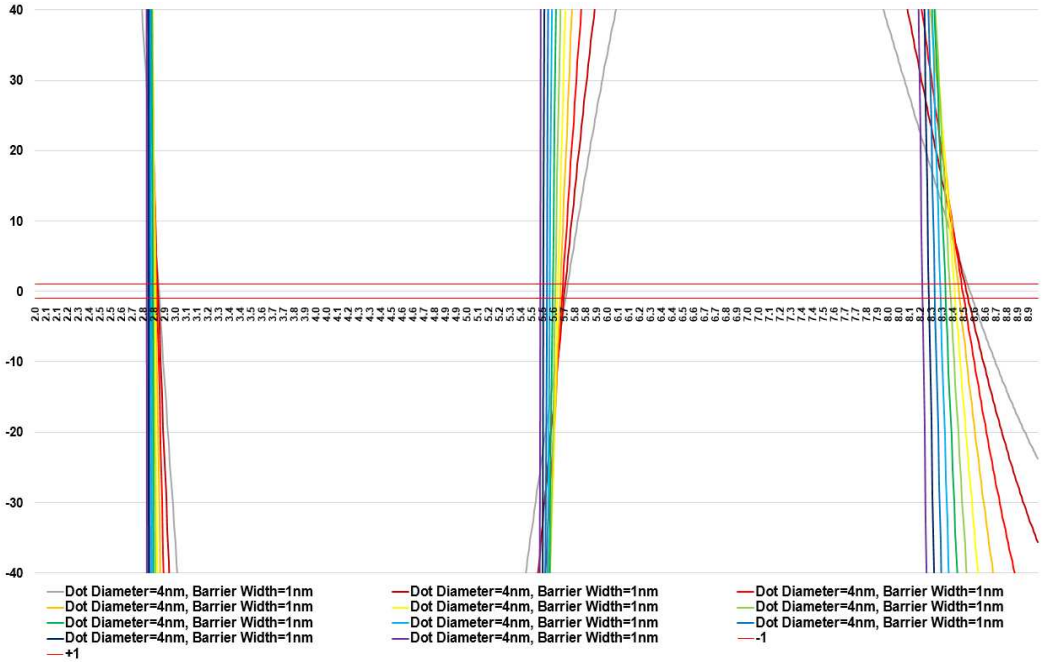


Figure 4.38. Simulation of left hand side (LHS) of the Equation

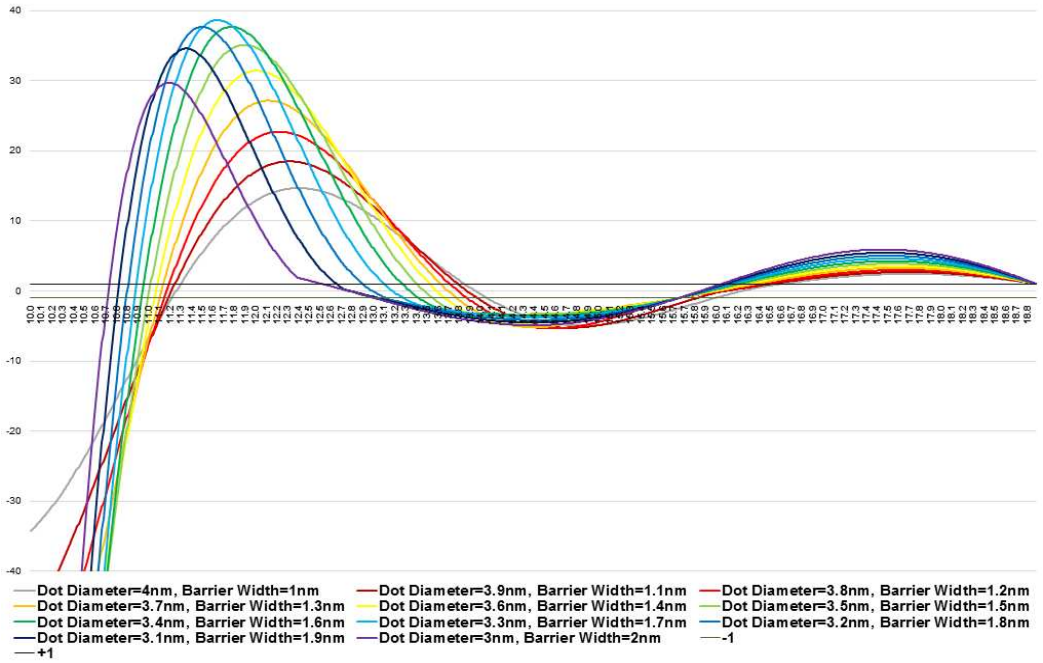


Figure 4.39. Simulation of left hand side (LHS) of the Equation

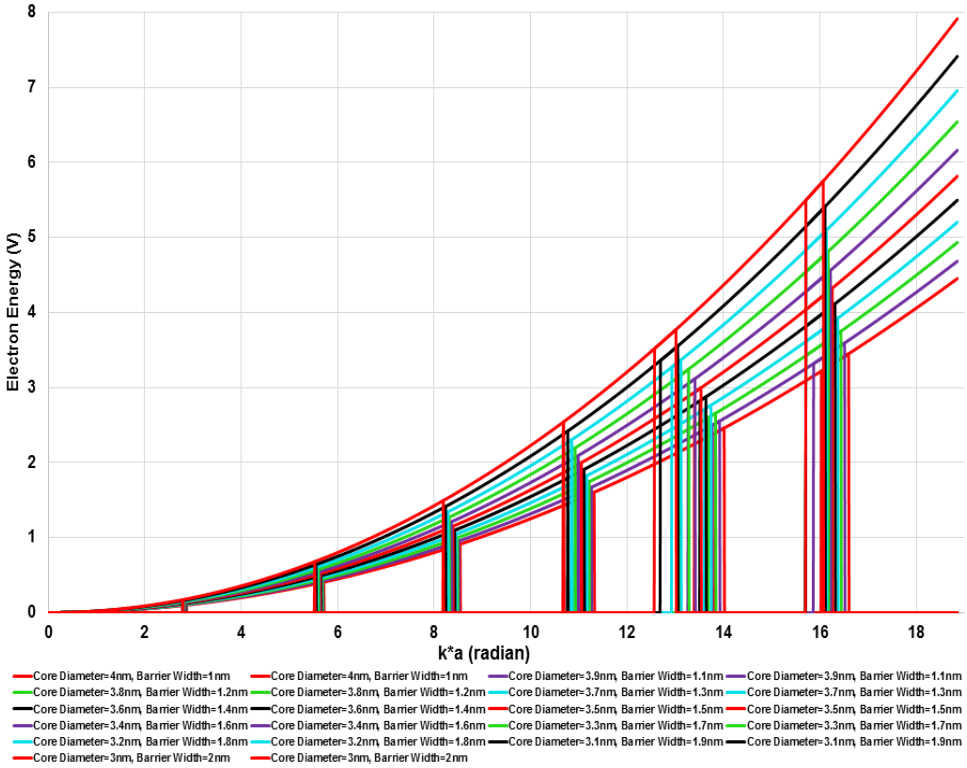


Figure 4.40. Relationship between Electron Energy (V) and k*a (radian)

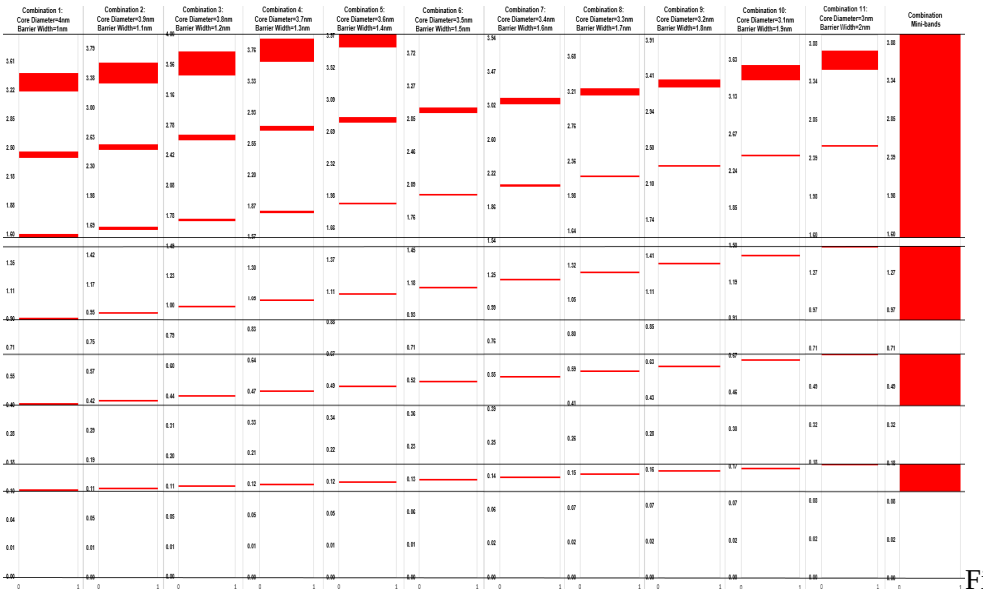


Figure 4.41. Electron Energies (V) for Mini-bands and Core-barrier Combinations

4.3. References

[1] F. Jain, M. Lingalugari, J. Kondo, P, Mirdha, E. Suarez, J. Chandy, and E. Heller "Quantum Dot Channel (QDC) FETs with Wraparound II-VI Gate Insulators: Numerical Simulations," *J. Electronic Materials*, 45, 11, pp. 5663-5670, 2016.

[2] F. Jain, P.-Y. Chan, E. Suarez, M. Lingalugari, J. Kondo, P. Gogna, B. Miller, J. Chandy, and E. Heller, "Four-State Sub-12-nm FETs Employing Lattice-Matched II-VI Barrier Layers." *Journal of Electronic Materials*, Vol. 42, No. 11, p. 3199-3201, 2013.

[3] F. Jain, S. Karmakar, P.-Y. Chan, E. Suarez, M. Gogna, J. Chandy, and E. Heller "Quantum Dot Channel (QDC) Field-Effect Transistors (FETs) Using II-VI Barrier Layers." *Journal of Electronic Materials*, Vol. 41, No. 10, 2780-2781, 2012.

[4] J. Chandy and F. Jain, *Proc. to International Symposium on Multiple Valued Logic*, Dallas, Texas, pp. 186, 2008.

[5] C. Weisbuch and B. Vinter, *Quantum Semiconductor Structures Fundamentals and Applications*, San Diego, California: Academic Press, p. 28, 1991.

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CHAPTER 5

Experimental I-V Characteristics of

QDC-FETs and Nonvolatile Memories

5.1. Quantum Dot Channel Quantum Dot Gate Field Effect Transistor

5.1.1. Device Numbering System

The device numbers of a sample are shown in Figure 5.2. The location of a device is specified using the following notation; Row Number + Colum Number + Device Number. Because this figure is the microscopic view, the gate terminal is shown at the upper part of each section. From the past research, it has been known that the right side middle four devices; R4, R5, R6 and R7 are considered as most successful devices. Therefore, these four devices were tested in this sample.

5.1.2. Test Results

Sample 9 was the first sample where one of the devices showed the characteristics of the Quantum Dot Field Effect Transistor (QDC-FET). There were 32 sections in this sample, and four devices; R4, R5, R6 and R7 were tested in each section. Therefore, the total number of tested devices was 128. Figure 5.1 shows the microscopic view of Sample 9, and the gate terminal is shown at the upper part of each section. There are three different symbols in Figure 5.1. The star mark stands for the QDC-FET, the circular mark stands for the conventional FET, and triangular mark also stands for the conventional FET. But significant noise components were mixed into the characteristics. The QDG-QDC FET was found at the device location of "R5C1r4", and is shown in Figure 5.1. The enlarged view of the device is shown in Figure 5.3. The gate length, the gate width and the gate area of all devices are shown in Table 2.4. Because Figure 5.1 is the microscopic view where the gate terminal is shown at the upper part of each section, Table 2.4 is applied reversely. Therefore, the gate length, the gate width and gate area of the QDG-QDC FET are 60μm, 60μm and 3600μm^2. For the rest of 127 devices, twenty-five

devices showed the conventional FET characteristics, eight devices also showed the conventional FET characteristics, but significant noise components were mixed into the results, and 94 devices did not show any significant characteristics. The locations of these devices are shown in Figure 5.1.

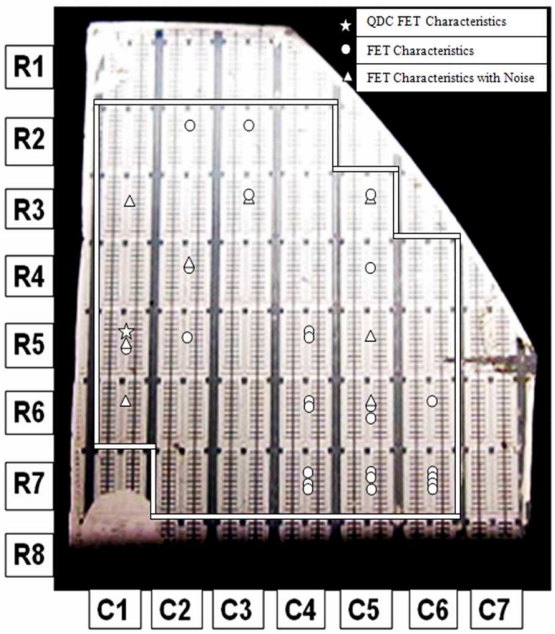


Figure 5.1. Microscopic View of Sample 9

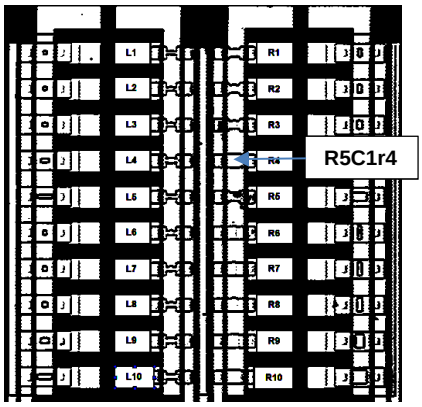


Figure 5.2. Device Numbers

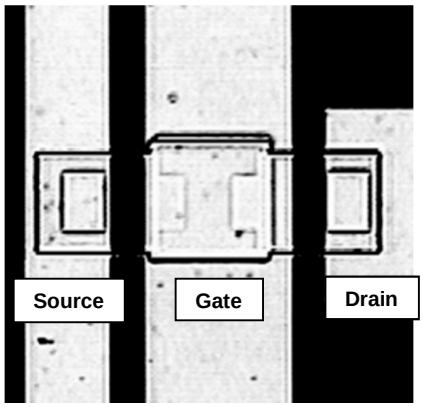


Figure 5.3. Fabricated QDG-QDC FET (R5C1r4)

5.1.3. I_D-V_G Characteristics

Figure 5.4 shows the I_D-V_G characteristics of the fabricated QDG-QDC FET, and the V_D voltages of 0.5 volts and 1.5 volts were used. When the V_D voltage was equal to 0.5 volts, one I_D current peak was observed at the V_G voltage of 0.20 volts. This I_D current peak is labeled as '1A'. When the V_D voltage was equal to 1.5 volts, three I_D current peaks were observed at the V_G voltages of -0.45, -0.20 and 0.55 volts (the upper left inset shows the enlarged view of the first and second I_D current peaks). These three peaks are labeled as '1B', '2B' and '3B'. Because the first I_D current peak is minor, characteristics of this QDG-QDC FET are still considered as the four state (OFF, 'I_1', 'I_2', ON) as the first QDG-QDC FET, and the state numbers are also indicated in Figure 5.4. The second and third I_D current peaks of the V_D voltage equal to 1.5 volts differentiate the first, second and third states, and the current saturation state is considered as the fourth state. Four I_D current peaks are individually shown in Figure 5.6. The I_D current peak information, which includes the peak label, V_D voltage, I_D peak current and corresponding V_G voltage, is shown in Table 5.1. As seen in Figure 5.4 and Table 5.1, the I_D current peaks occurred at different V_G voltages for the V_D voltages of 0.5 volts and 1.5 volts.

5.1.4. I_D-V_D Characteristics

The I_D-V_D characteristics of the QDG-QDC FET are shown in from Figure 5.5. Seven different V_G voltages were used to measure the I_D-V_D characteristics. These V_G voltages are 0.5, 0.7, 0.9, 1.1, 1.3, 1.5 and 1.7 volts. The I_D current line of the V_G voltage of 0.5 volts corresponds to the second state. Other I_D current lines correspond to the third and fourth states.

5.1.5. Conclusion

One of the most distinctive characteristics of this QDG-QDC FET is the number of I_D current peaks. Three I_D current peaks were observed at the V_G voltages of -0.45, -0.2 and 0.55 volts when the V_D voltage was equal to 1.5 volts. Therefore, it was the very first time when three current peaks were observed in QDG-QDC FETs. But the characteristics of this QDG-QDC FET were still considered as the four-state (OFF, 'I_1', 'I_2', ON) because the first current peak was minor. Also, the much higher I_D current flow was obtained from this QDG-QDC FET than the first QDG-QDC FET which was fabricated in 2011. The highest I_D peak current of approximately 141μA was obtained from this QDG-QDC FET. The highest I_D peak current of approximately 23μA was obtained from the first QDG-QDC FET. Therefore, the highest I_D peak current was approximately 6 times higher than the first QDG-QDC FET.

For the I_D-V_G characteristics of QDG-QDC FET, the I_D current peaks occurred at different V_G voltages for the V_D voltages of 0.5 volts and 1.5 volts in Figure 2.40. The peak label, V_D voltage, I_D peak current and corresponding V_G voltage are shown in Table 5.1. When the V_D voltage was equal to 0.5V, the first peak occurred at the V_G voltage of 0.20V. When the V_D voltage was equal to 1.5V, the first peak occurred at the V_G voltage of -0.45V, second peak occurred at the V_G voltage of -0.20V, and the third peak occurred at the V_G voltage of 0.55V. The electron leakage at the inconsistent and imperfect gate insulator caused these I_D current peaks which occurred at different V_G voltages for two different V_D voltages. Therefore, the gate dry oxidation process of the silicon quantum dot layer must be improved to prevent the electron leakage at the gate in the future.

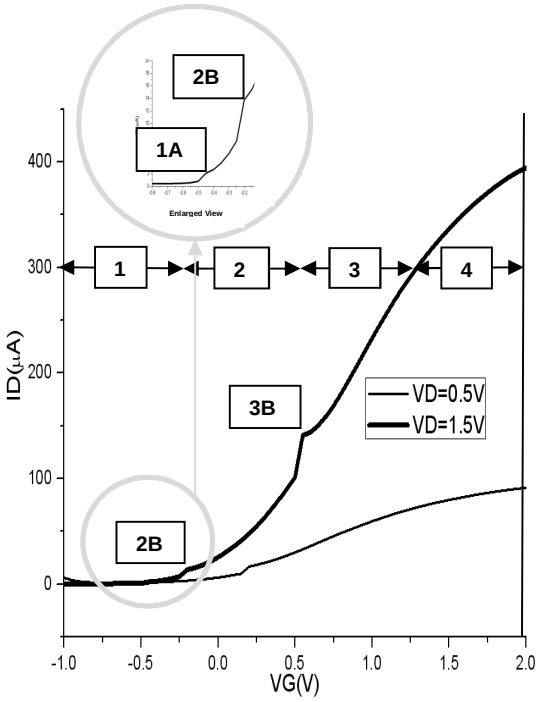


Figure 5.4. I_D-V_G Characteristics of Sample 9

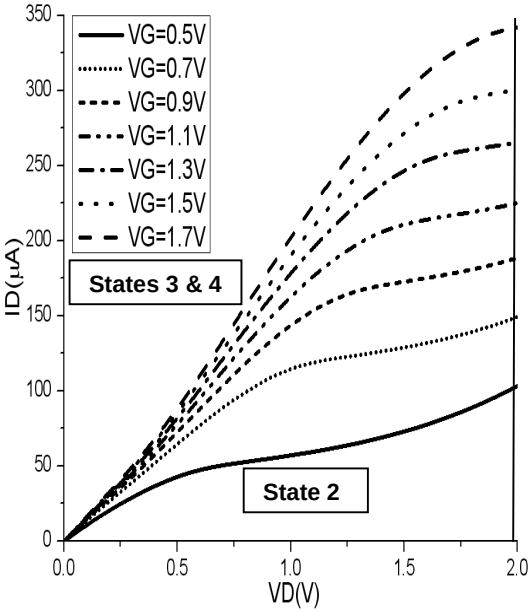


Figure 5.5. I_D-V_D Characteristics of Sample 9

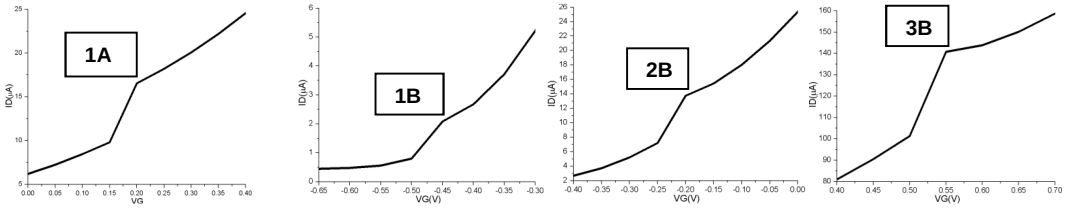


Figure 5.6. Four I_D Current Peaks of Sample 9

Peak Label	**V_D (V)**	**I_D (μA)**	**V_G (V)**
1A	0.5	16.555	0.20 V
1B	1.5	2.0835	-0.45 V
2B	1.5	13.745	-0.20 V
3B	1.5	140.80	0.55 V

Table 5.1. Peak I_D Current Information of Sample 9

5.2. QDG-QDC Nonvolatile Memory using Silicon Dots

5.2.1. Structure

The structure of the QDG-QDC Nonvolatile Memory using silicon quantum dots is shown in Figure 7.7. It consists of two layers of silicon oxide (SiOx)-cladded Si quantum dots in the channel region and the floating gate region. An oxidized SiOx-Si upper quantum dot layer forms the gate dielectric which has a thicker SiOx cladding layer with a narrower Si core [4]. A 75Å Si_3N_4 layer forms the control dielectric. The memory device has a channel width of 60μm and the length of 60μm, and the W/L ratio of 26/25.

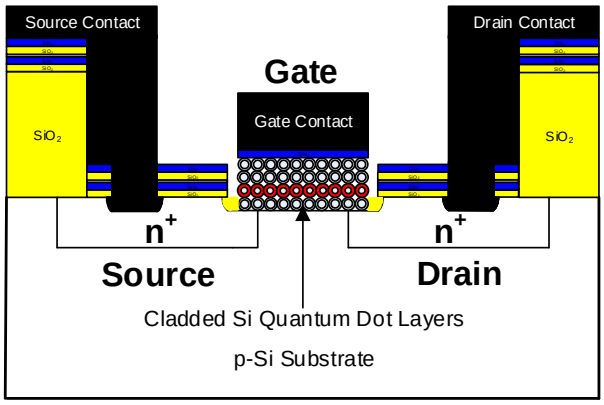


Figure 5.7. Structure of QDG-QDC Nonvolatile Memory using Silicon Quantum Dots

5.2.2. Fabrication

The fabrication procedures started with a p-type silicon wafer with a masking SiO_2 layer. Phosphorus diffusion was performed for approximately 10 min at 1000°C to form the source and drain regions. This was followed by deposition of the silicon nitride layer for the chemical and thermal protections. The gate region was oxidized to form the silicon dioxide layer which was etched to create a recessed region between the source and the drain. This was

followed by self-assembly of two layers of cladded silicon quantum dots in the recessed region for the transport channel. After self-assembly, the two layers of cladded silicon quantum dots were annealed, and the top quantum dot layer was partially oxidized in oxygen ambient to obtain the gate insulator. This was followed by self-assembly of two layers of cladded silicon quantum dots for the floating gate, and a 75Å silicon nitride layer was deposited for the control dielectric. Finally, the gate metal aluminum was deposited for approximately 2000Å, and divided for source, drain and gate contacts.

5.2.3. I_D-V_G and I_D-V_D Characteristics

Figure 5.8 shows the I_D–V_G characteristics before and after the 'Write' pulse. The gate pulse was 40V for 10 ms, and drain pulse was 30 V for 50 ms [4]. The measured threshold voltage shift ΔV_{TH} was approximately 1.8V at 50μA before and after the 'Write' cycle when V_D was equal to 2V. Figure 5.9 shows the I_D–V_D characteristics before and after the 'Write' pulse. The gate pulse was 40V for 10 ms, and drain pulse was 30 V for 50 ms. The V_G voltages are 0V, 1V, 2V, 3V, and 4V. Each V_G voltage shows clear shift before and after the pulse.

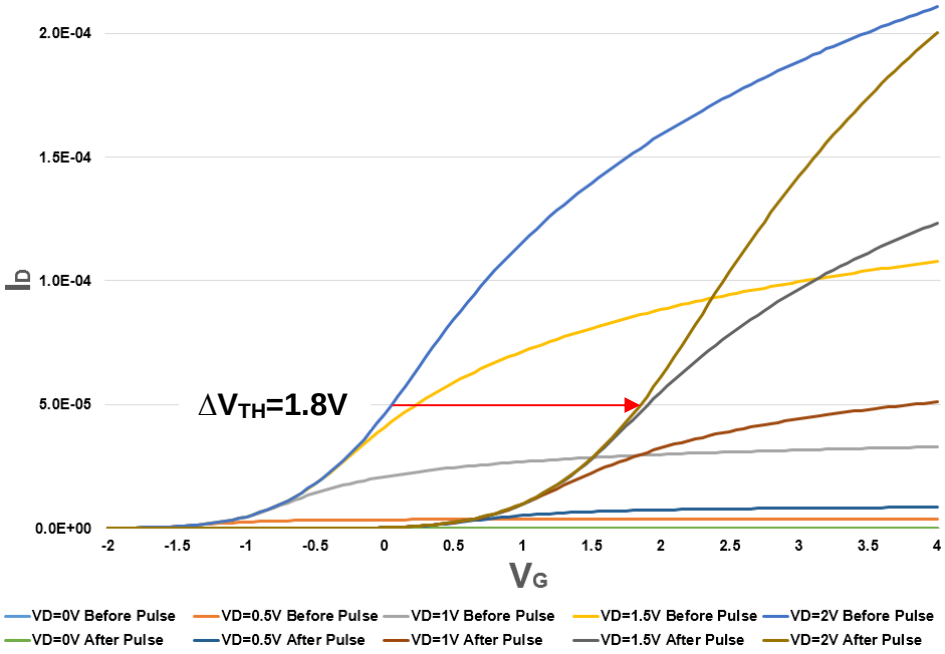


Figure 5.8. I_D-V_G Characteristics of the QDG-QDC NVM using Silicon Quantum Dots

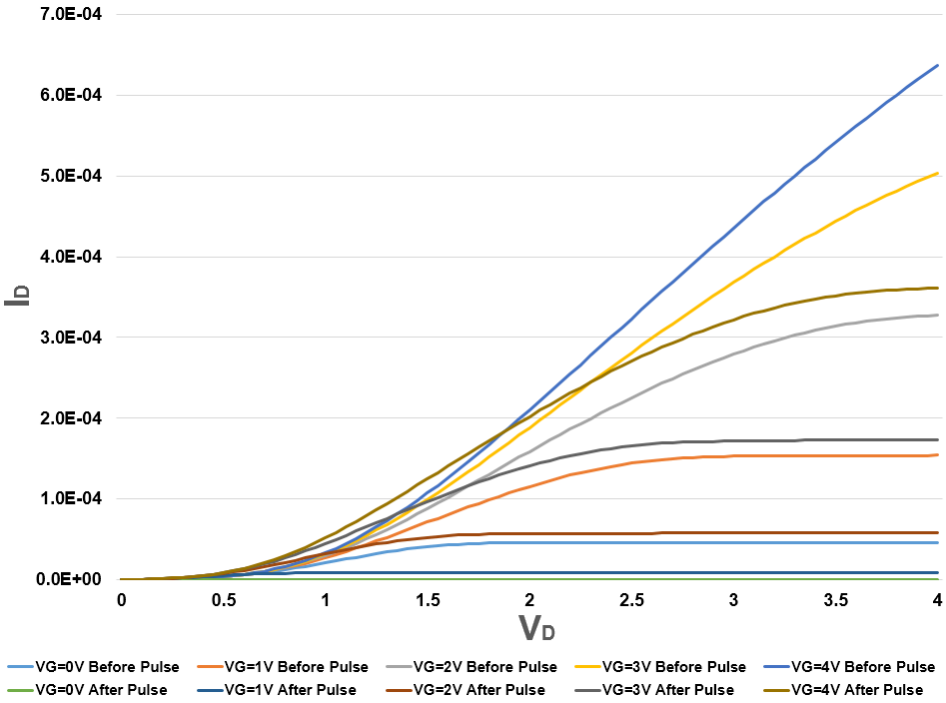


Figure 5.9. I_D-V_D Characteristics of the QDG-QDC NVM using Silicon Quantum Dots

5.3. Quantum Dot Channel Quantum Dot Gate Nonvolatile Memory using Germanium Quantum Dots

5.3.1. Structure

The structure of Quantum Dot Channel Quantum Dot Gate (QDG-QDC) Nonvolatile Memory (NVM) is shown in Figure 5.10. The nonvolatile memory has the gate size of 60µm x 60µm, and the W/L ratio of 26/25. Figure 5.11 shows the gate structure of QDG-QDC NVM. The gate dielectric consists of 26Å $HfAlO_2$, and the control dielectric consists of 53Å $HfAlO_2$. The transport channel and the floating gate consist of GeO_x-cladded Ge quantum dots.

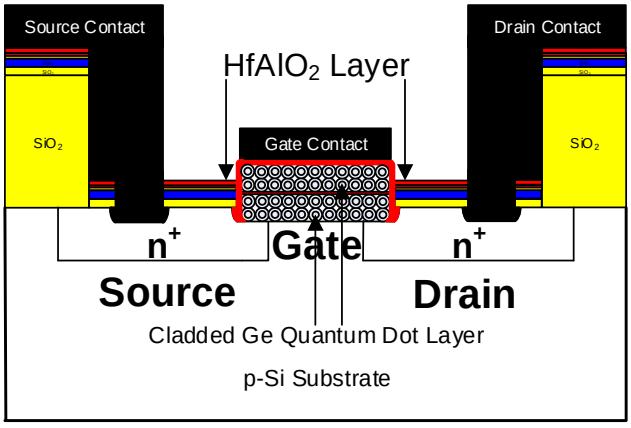


Figure 5.10. Structure of QDG-QDC NVM using Germanium Quantum Dots

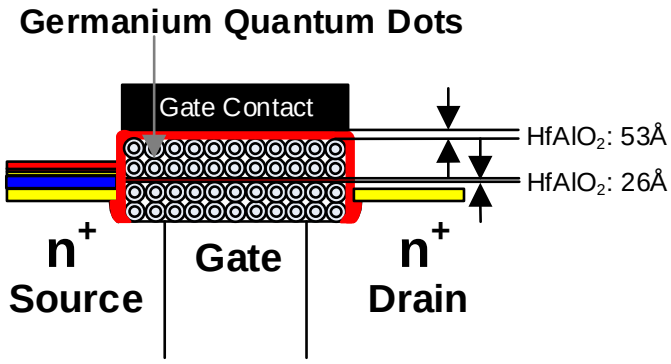
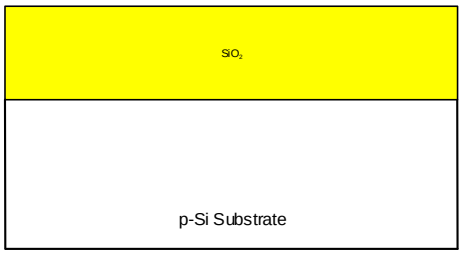


Figure 5.11. Gate Structure of QDG-QDC NVM using Germanium Quantum Dots

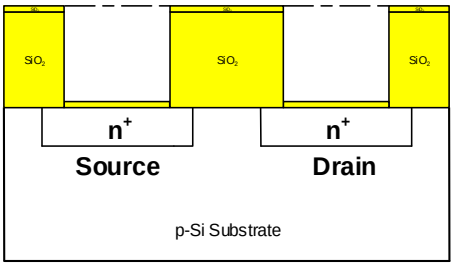
5.3.2. Fabrication

The fabrication of the nonvolatile memory was involved in the following twelve major steps;

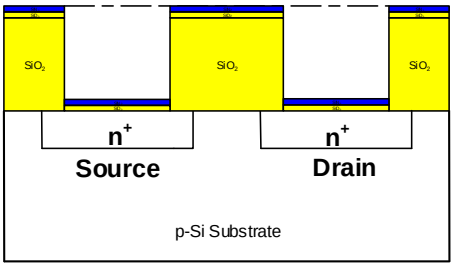
1. 1250Å Wet Oxidation on P-Type Silicon Substrate



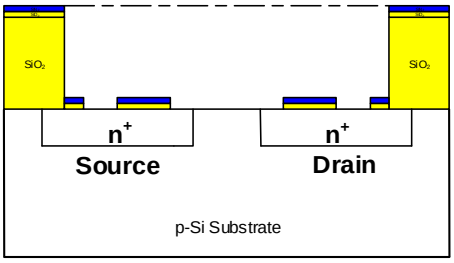
2. Source and Drain Fabrication using Mask 3, and Phosphorus Diffusion



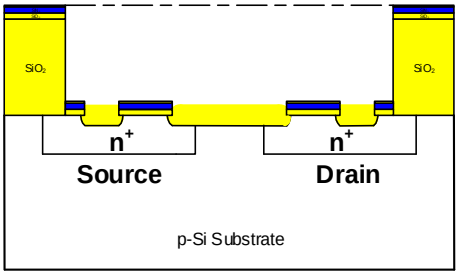
3. 75Å Silicon Nitride Deposition



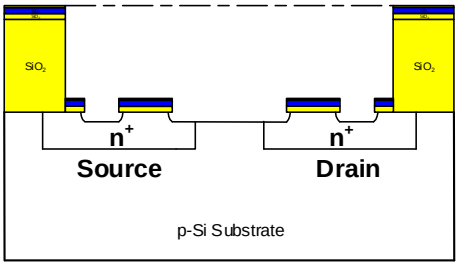
4. Mask 4: Gate Opening, Part 1 (Refer to Appendix 5.A: BOE Time Estimate)



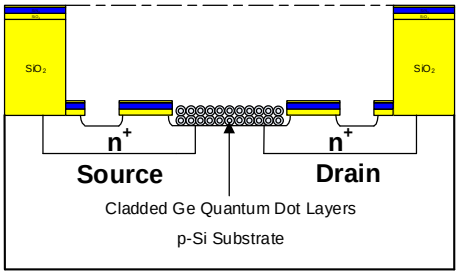
5. 250Å Dry Oxidation



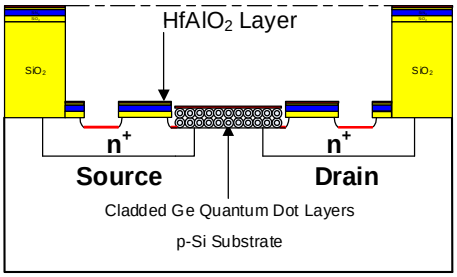
6. Mask 4: Gate Opening, Part 2



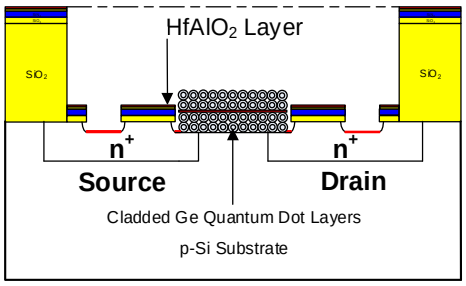
7. Germanium Quantum Dot Deposition:
   Self-Assembly and Annealing at 350ºC for 10 minutes



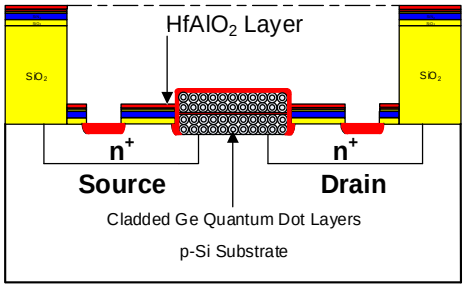
8. Aluminum Oxide and Hafnium Oxide Deposition



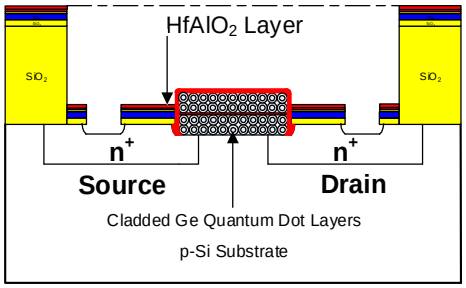
9. Self-Assembly and Annealing at 350°C for 10 minutes



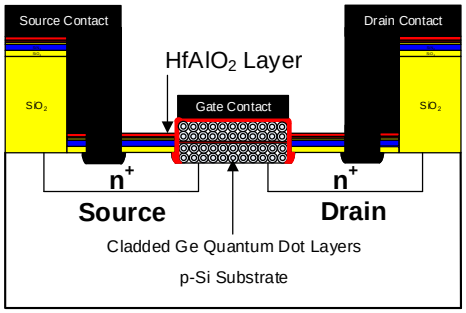
10. Aluminum Oxide and Hafnium Oxide Deposition



11. Mask 5: Open Source and Drain Contacts (Refer to Appendix 5.B BOE Time Estimate)



12. Metallization and Mask 6: Interconnect



QDG-QDC NVM using Germanium Quantum Dots

The $HfAlO_2$ nanolaminate high-k dielectric combinational layers were deposited using the Savannah Atomic Layer Deposition (ALD) system. The program was executed for twelve cycles to deposit the 26Å gate dielectric in Step 8, and for thirty-four cycles to deposit the 53Å control dielectric in Step 10. Please refer to Section 2.1.5 of this thesis for more information.

5.3.3. I_D-V_G and I_D-V_D characteristics

The measured I_D-V_G and I_D-V_D characteristics of the fabricated floating gate nonvolatile memory are shown in Figure 5.12 and Figure 5.13. The drain pulse of 4V for 400µs and the gate pulse of 15V for 100µs were applied simultaneously. In Figure 5.12, the labels B4, B5 and B6 correspond the drain voltages of 4, 5, and 6V before the pulse, and the labels A4, A5 and A6 correspond the drain voltages of 4, 5, and 6V after the pulse. In Figure 5.13, the labels B4, B5 and B6 correspond the gate voltages of 4, 5, and 6V before the pulse, and the labels A4, A5 and A6 correspond the gate voltages of 4, 5, and 6V after the pulse. The maximum threshold voltage shift ΔV_{TH} in I_D-V_G characteristics was approximately 0.9V at the drain current of 246µA. The maximum threshold voltage shift ΔV_{TH} in I_D-V_D characteristics was approximately 0.8V at the drain current of 390µA. The maximum current flow in I_D-V_G characteristics was 522µA before the pulse, and 246µA after the pulse. The maximum current flow in I_D-V_D characteristics was 704µA before the pulse, and 390µA after the pulse. Therefore, it is concluded that the QDC-FET nonvolatile memory with $HfAlO_2$ nanolaminate high-k dielectric combinational layers at the gate dielectric and the control dielectric provides both the significantly higher I_D current flow and the significantly higher threshold voltage shifts which improve the threshold voltage variation, and show the potential for fabricating multi-bit nonvolatile memories.

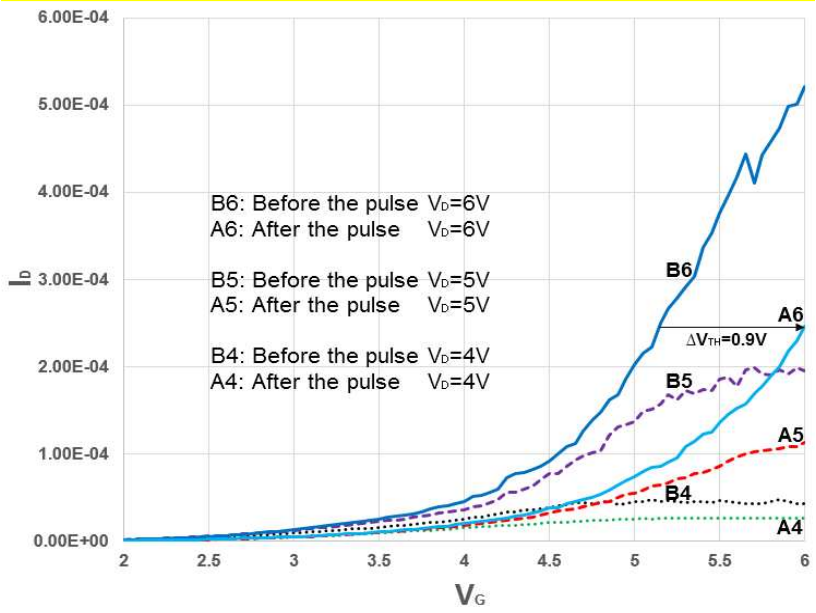


Figure 5.12. I_D-V_G characteristics of QDG-QDC NVM using Germanium Quantum Dots

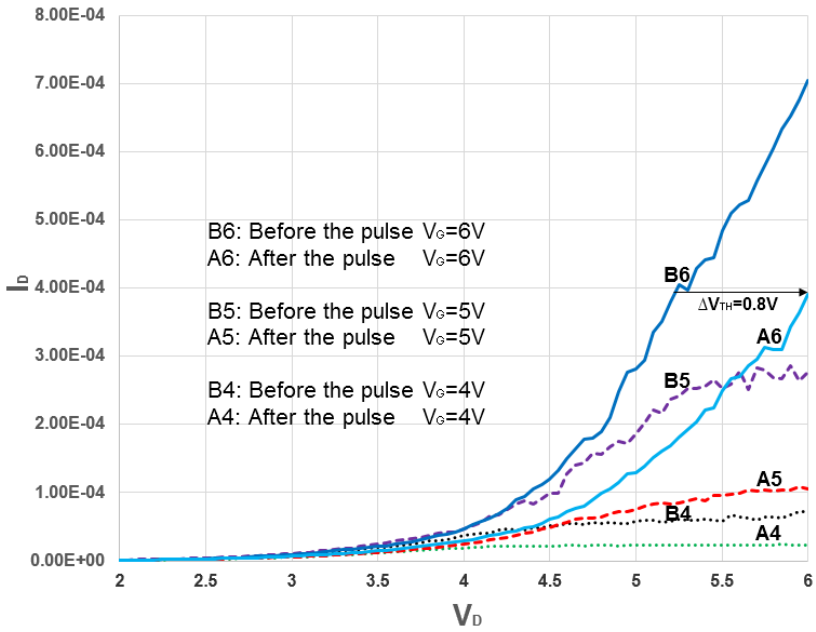


Figure 5.13. I_D-V_D characteristics of QDG-QDC NVM using Germanium Quantum Dots

5.4. Quantum Dot Gate Nonvolatile Memory using Silicon Quantum Dots

5.4.1. Structure

The structure of Quantum Dot Gate (QDG) Nonvolatile Memory (NVM) is shown in Figure 5.14. The nonvolatile memory has the gate size of 10µm x 5µm, and the W/L ratio of 10/5 [X]. The gate dielectric consists of 20Å silicon dioxide, and the control dielectric consists of 75Å silicon nitride, and the floating gate consist of SiO_x-cladded Si quantum dots [X]. The major advantage of this structure is the electrical insulation provided by the SiOx cladding layer [X]. It reduces lateral dot-to-dot charge conduction in the floating gate layer, and allows improved dot uniformity and higher density resulting in higher charge storage [X].

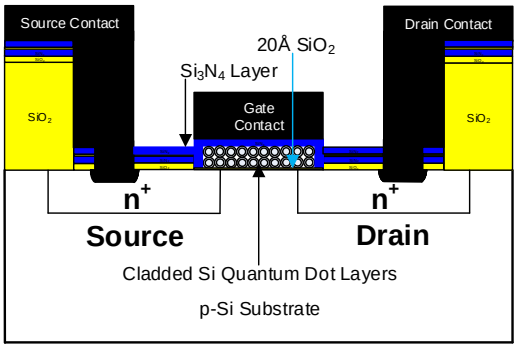


Figure 5.14. Structure of QDG NVM using Silicon Quantum Dots

5.4.2. I_D-V_G and I_D-V_D Characteristics

The I_D-V_G and I_D-V_D characteristics of the fabricated floating gate nonvolatile memory are shown in Figure 5.15 and Figure 5.16 [X]. The drain pulse of 10V for 1µs, 2µs, and 10µs, the gate pulse of 6V for 1µs, 2µs, and 10µs were applied simultaneously [X]. The I_D-V_G characteristics show the maximum threshold voltage shift ΔV_{TH} of approximately 0.7V at the drain current of approximately 100µA [X]. The I_D-V_D characteristics show the significant current reduction after the drain and gate pulses [X].

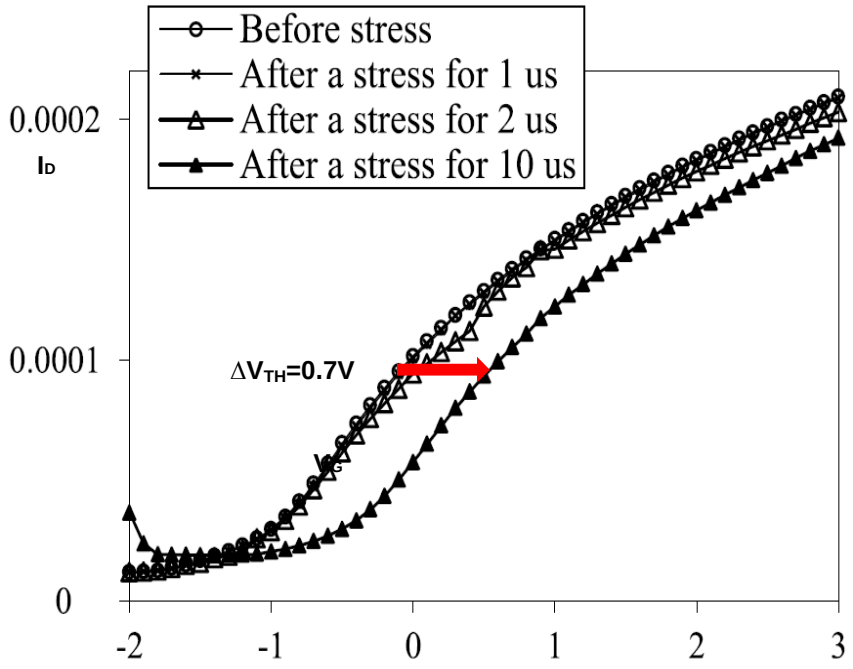


Figure 5.15. I_D-V_G Characteristics of the QDG NVM using Silicon Quantum Dots

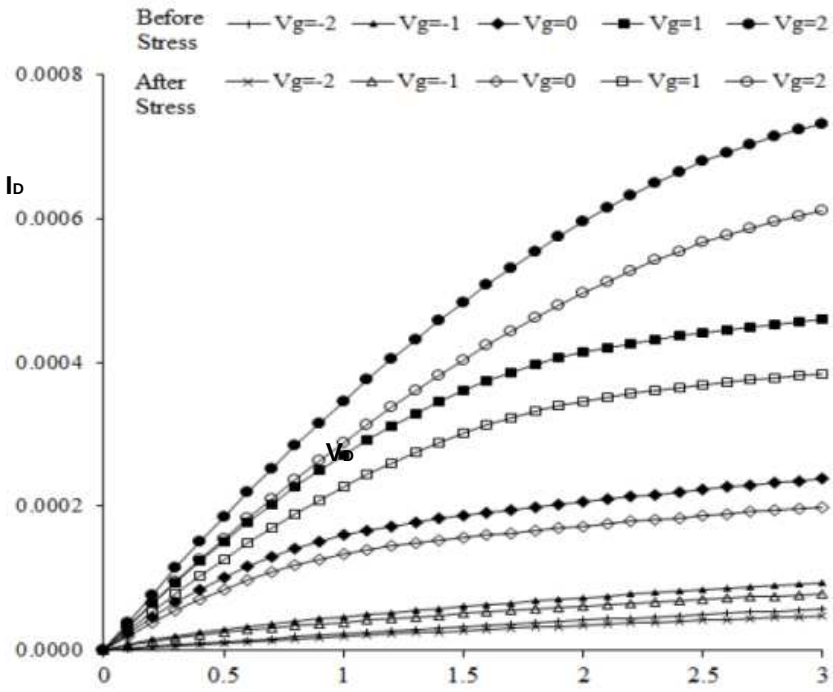


Figure 5.16. I_D-V_D Characteristics of the QDG NVM using Silicon Quantum Dots

5.5. Quantum Dot Channel Field Effect Trannsistor using Ge Quantum Dots

5.5.1. Structure

The structure of QDC FET is shown in Figure 5.17. The QDC FET consists of two layers of cladded Germanium quantum dots in the channel regions. Here, GeOx cladded forms the thin-barrier (~1nm) over Ge quantum dots (3nm in diameter). An array of these cladded dots behaves as a quantum dot superlattice (QDSL) [2]. This superlattice has energy mini-bands that are very narrow and separated with larger energy than in conventional quantum well/wire superlattices [2]. The Kronig-Penney model was used to determine the energy mini-band locations and widths [2]. The measured QDC-FET device has the gate length and the gate width of 60μm, and the gate width and the gate length ratio (W/L ratio) of 26/25.

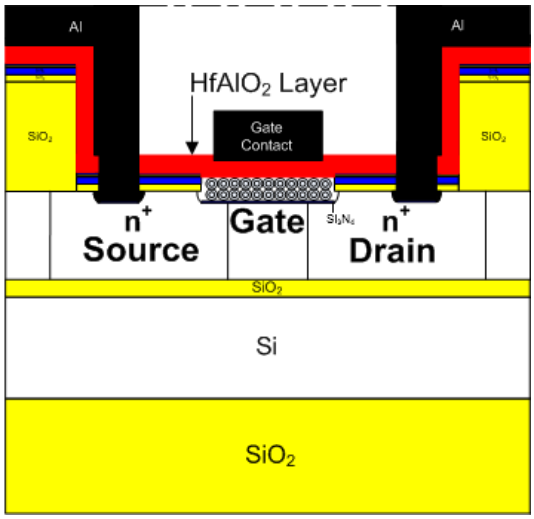


Figure 5.17. Structure of QDC FET

Fig. 5.18 shows that this FET has the following materials for the gate; aluminum gate contact, $HfAlO_2$, GeO_x-cladded Ge quantum dots, silicon nitride. In order to enhance the current flow in the transport channel, a silicon nitride layer was deposited on the substrate. Two layers of GeO_x-cladded Ge quantum dots were self-assembled for the transport channel at the recessed region between the n^+ source and the n^+ drain. Electrons flow from the source to the drain through the transport channel. Eighty seven cycles of $HfAlO_2$ nanolaminated high-k dielectric combinational layers were deposited for the 200Å tunnel oxide in order to attain relatively large dielectric constant and band gap. The combinational layers were deposited using the Savannah Atomic Layer Deposition (ALD) system at Harvard. For more information about the Savannah Atomic Layer Deposition (ALD) system, please refer to Section 2.1.5 of this thesis.

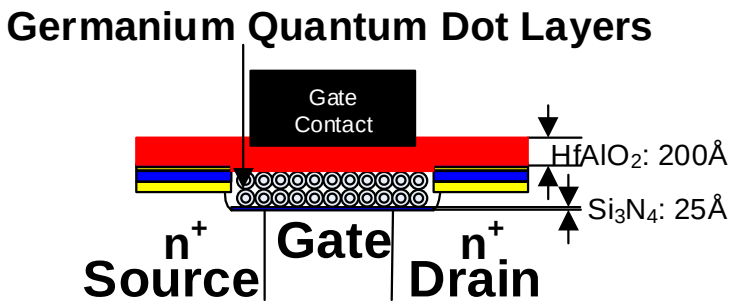
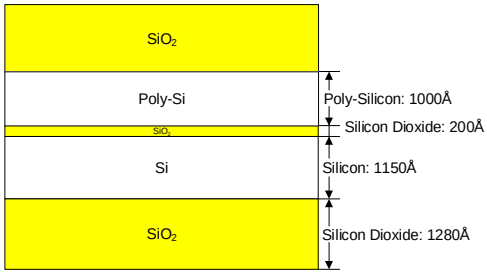


Figure 5.18. Gate Structure of QDC FET

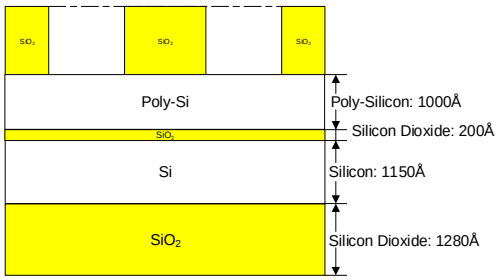
5.5.2. Fabrication Procedures

The fabrication of the field effect transistor was involved in the following twelve major steps;

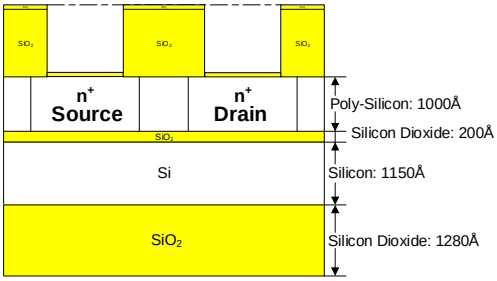
1. 1250Å PECVD Deposition on the Polysilicon Substrate



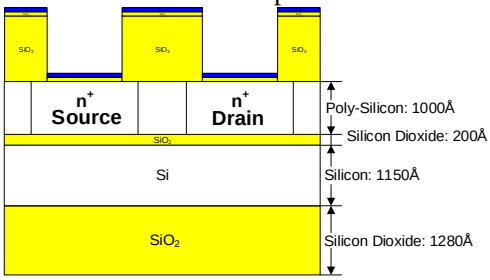
2. Source and Drain Fabrication using Mask 3



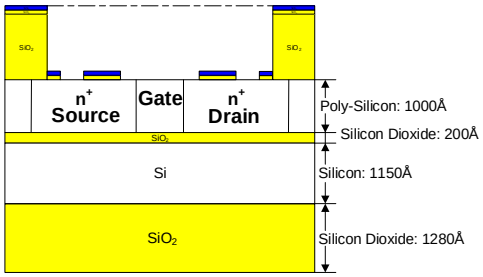
3. Phosphorus Diffusion



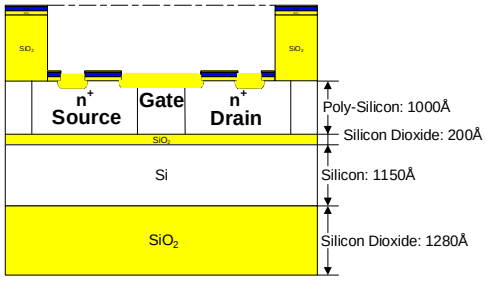
4. 75Å Silicon Nitride Deposition



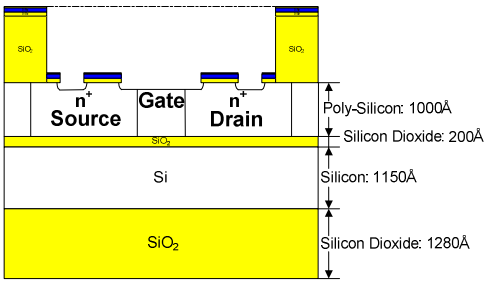
5. Mask 4: Gate Opening, Part 1



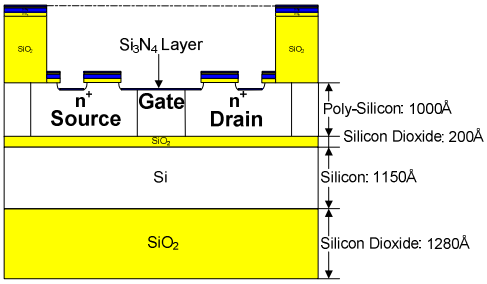
6. 250Å Dry Oxidation



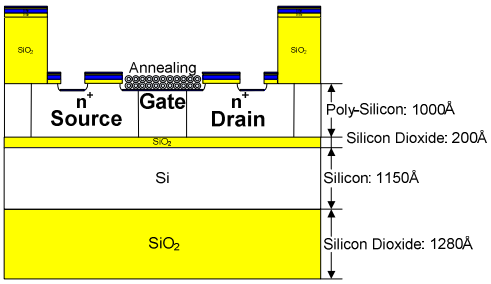
7. Mask 4: Gate Opening, Part 2



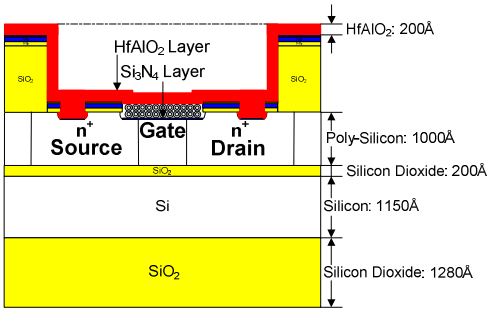
8. 20Å Silicon Nitride Deposition



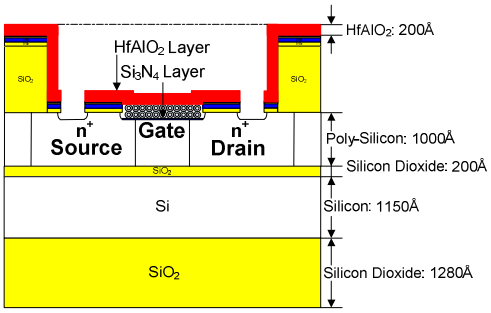
9. Self-Assembly of Germanium Quantum Dots and Annealing at 350ºC for 10 minutes



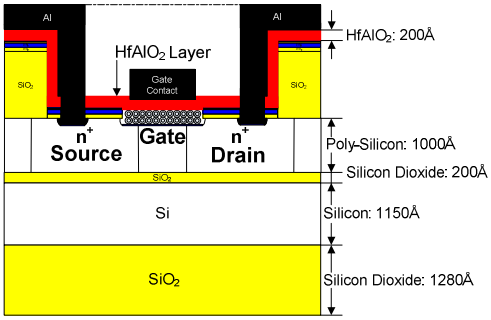
10. Hafnium Oxide/Aluminum Oxide Combinational Layer Deposition for the Tunnel Oxide



11. Mask 5: Open Source and Drain Contacts



12. Metallization and Mask 6: Interconnect



QDC FET using Germanium Quantum Dots with Silicon Nitride Insulator

5.5.3. I_D-V_G Characteritics

The fabricated QDC FET was tested for multi-state characteristics. Figure 5.19 shows the I_D-V_G characteristics of QDC FET, and V_G was changed from -3 to 13 volts, and V_G was changed from 0 to 15 volts. When V_D was greater than 3 volt, I_D peaks was observed at numerous locations. The distinct three-state characteristic (low-intermediate-high) were observed when V_D was equal to 12, 13 and 14 volts. When V_D was equal to 12V, the maximum I_D peak was 9.17μA at V_G equal to 9.5V. When V_D was equal to 13V, the maximum I_D peak was 9.01μA at V_G equal to 9.0V. When V_D was equal to 14V, the maximum I_D peak was 9.98μA at V_G equal to 8.0V.

5.5.4. I_D-V_D Characteritics

Figure 5.20 shows the I_D-V_D characteristics which was generated from I_D-V_G characteristics. V_D was changed from 0 to 15 volts, and V_G was changed from -3 to 13 volts. These I_D-V_D characteristics represented three distinct groupings. The I_D currents of V_G less than 8.5 volts formed the first group, the I_D currents of V_G equal to 8.5, 9, 9.5, 10, 10.5 volts formed the second group, and the I_D currents of V_G equal to 11, 11.5, 12, 12.5, 13 volts formed the third group. In the past, distinct groupings were also observed in quantum dot gat quantum dot channel field effect transistor (QDG-QDC FET). But these groups were completely separated. In the QDC FET, some groups were actually overlapping each other, and show completely different I_D-V_D characteristics from QDG-QDC FET.

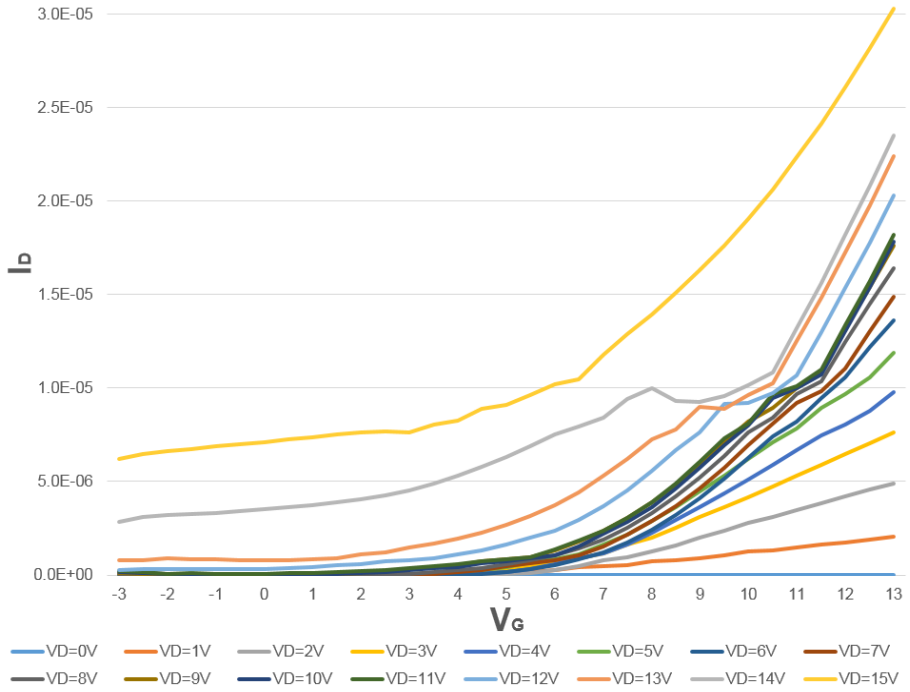


Figure 5.19. I_D-V_G Characteristics of the QDC FET using Germanium Quantum Dot

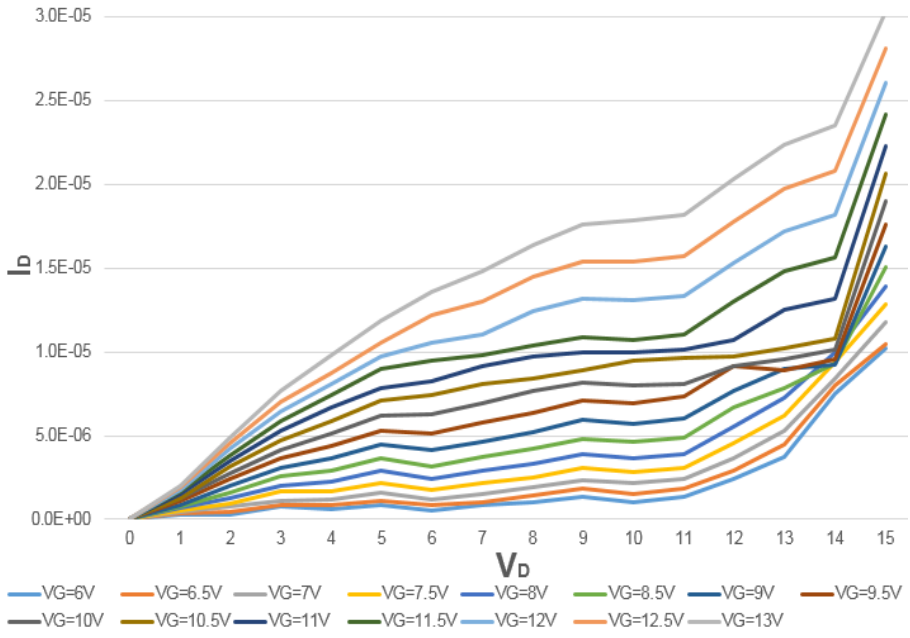


Figure 5.20. I_D-V_D Characteristics of the QDC FET using Germanium Quantum Dots

5.6. Conventional Field Effect Transistor

5.6.1. Structure

The structures of conventional FETs are shown on Figure 5.21. These figures show the FETs which have 200Å and 300Å $HfAlO_2$ nanolaminate high-k dielectric combinational layers for the tunnel oxides. The measured QDC-FET device has the gate length and the gate width of 60μm, and the gate width and the gate length ratio (W/L ratio) of 26/25. The devices with 25Å, 50Å, 100Å and 150Å $HfAlO_2$ nanolaminate high-k dielectric combinational layers were also tested. But electrons penetrated through the tunnel oxides, and the experiments were unsuccessful. Also, the device with 400Å $HfAlO_2$ nanolaminate high-k dielectric combinational layers was tested. But the results were very similar to the device with 300Å $HfAlO_2$ nanolaminate high-k dielectric combinational layers.

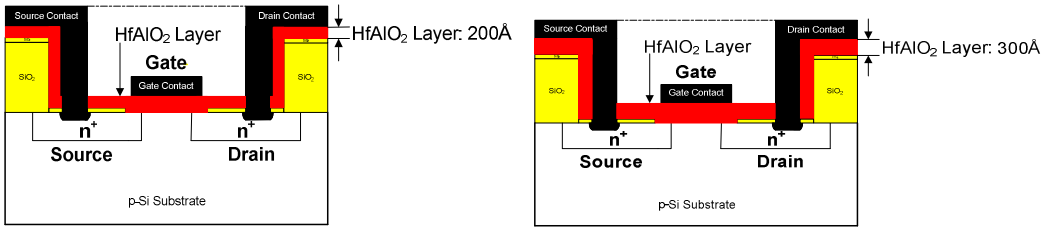


Figure 5.21. Cross-section of the conventional FET with 200Å and 300Å tunnel oxide

5.6.2. I_D-V_G and I_D-V_D characteristics

I_D-V_G characteristics for the 200Å tunnel oxide device are shown in Figure 5.22, and I_D-V_D characteristics for the 200Å tunnel oxide device are shown in Figure 5.23. I_D-V_G characteristics for the 300Å tunnel oxide device are shown in Figure 5.24, and I_D-V_D characteristics for the 300Å tunnel oxide device are shown in Figure 5.25.

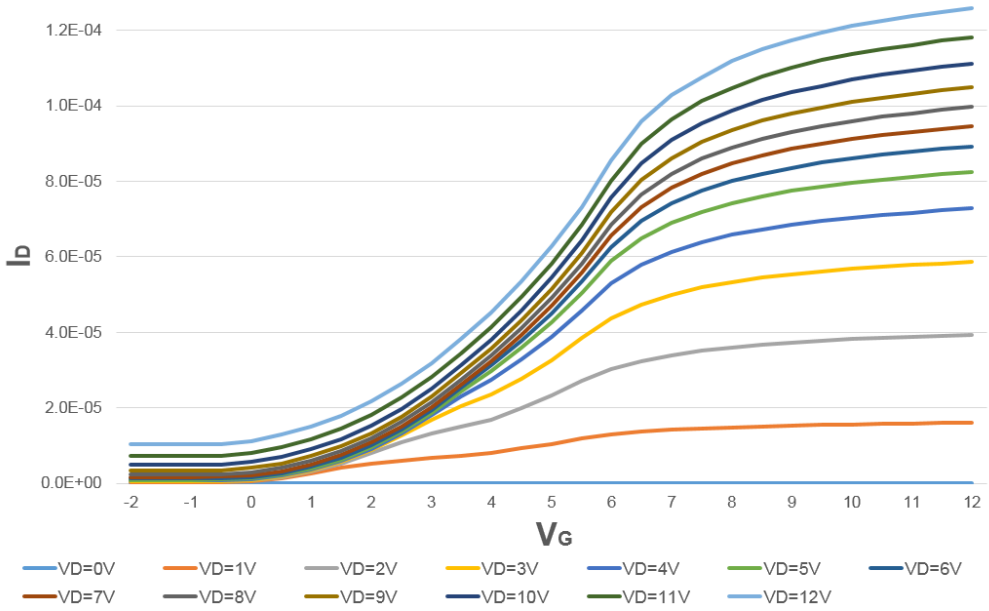


Figure 5.22. I_D-V_G characteristics of the Conventional FET with 200Å tunnel oxide

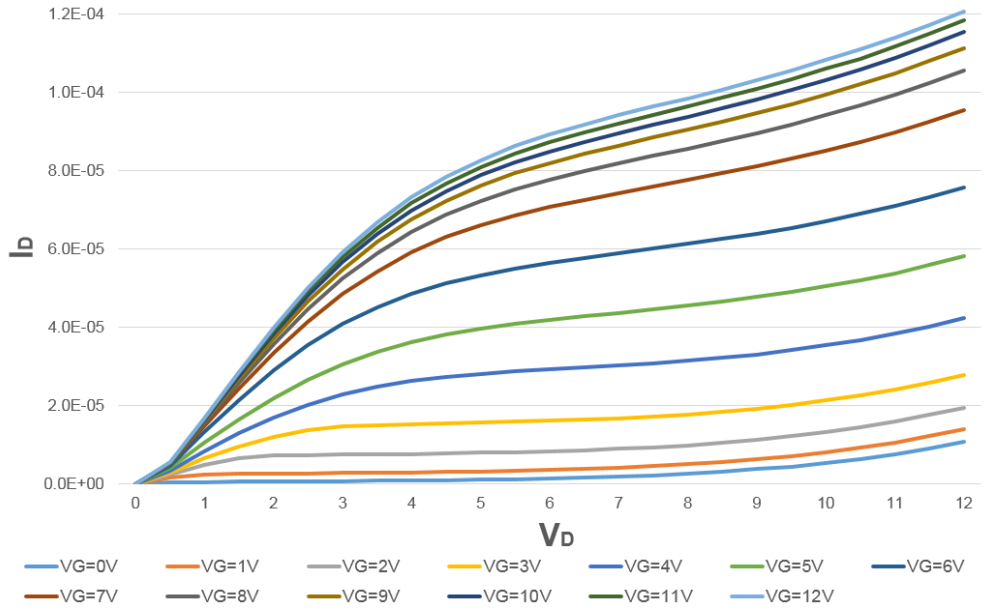


Figure 5.23: I_D-V_D characteristics of the Conventional FET with 200Å tunnel oxide

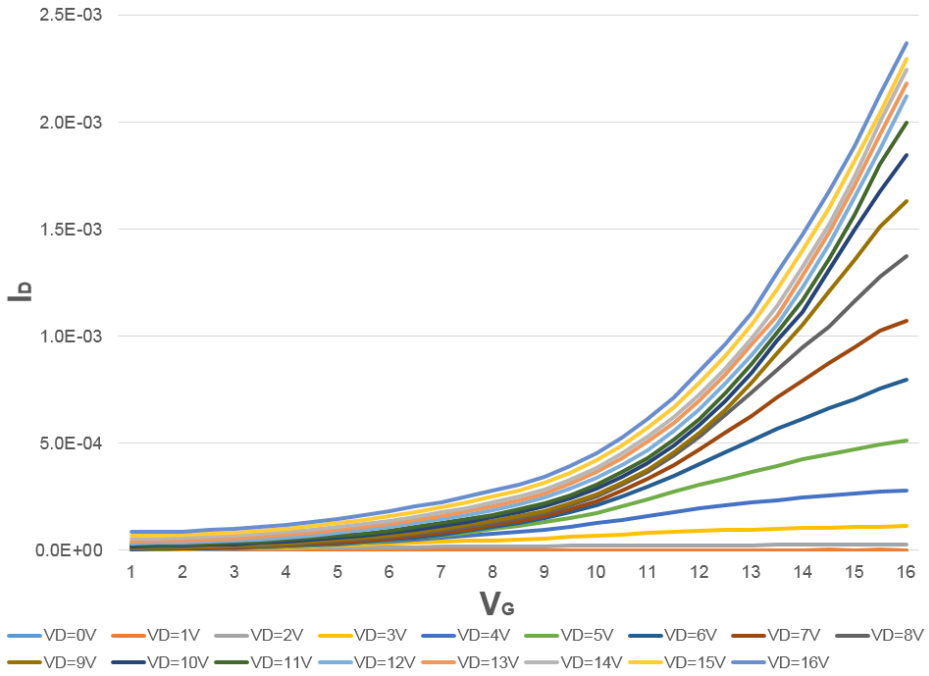


Figure 5.24. I_D-V_G characteristics of the Conventional FET with 300Å tunnel oxide

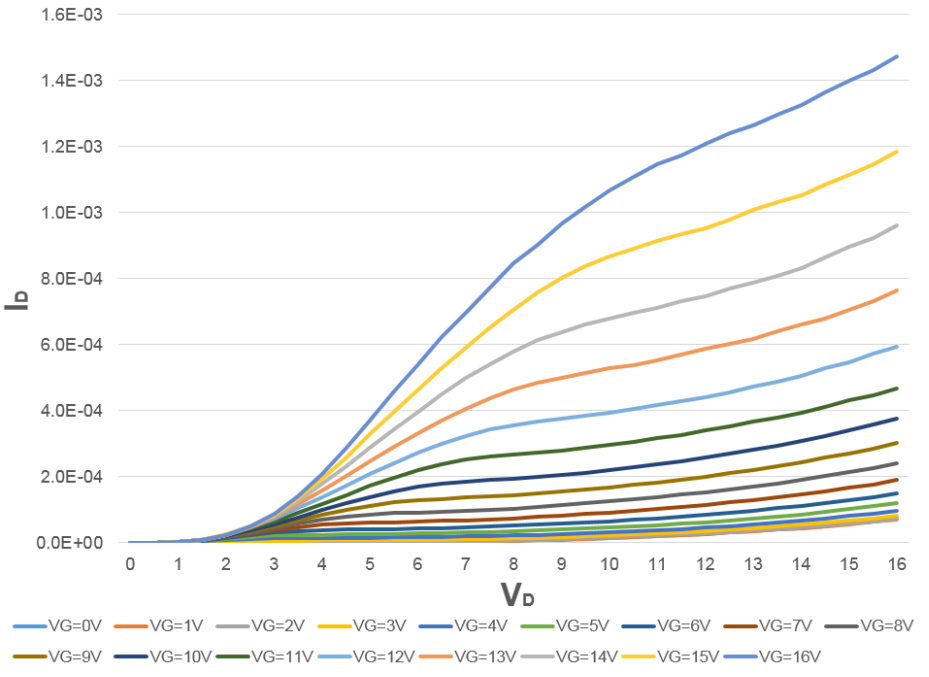


Figure 5.25. I_D-V_D characteristics of the Conventional FET with 300Å tunnel oxide

From the I_D-V_G and I_D-V_D measurement results, it was conclude that the conventional FETs with $HfAlO_2$ nanolaminate high-k dielectric combinational layers for the tunnel oxides have the following characteristics.

1. Extremely High Current Flow

   For the device with 300Å tunnel oxide, the current flow was exceeded 2mA when V_G and V_D were over 10 volts. Therefore, they are strong candidates for power transistors.

2. Unique I_D-V_G and I_D-V_D Characteristics

   It was difficult to determine the threshold voltages because no straight current line existed in the I_D-V_G characteristics. Also, the current increased almost exponentially when V_D was low in the I_D-V_D characteristics. Therefore, the traditional current equations could not be applied for these results.

The gate structures of these devices are summarized as follows;

Device Name	Ge Quantum Dots	$HfAlO_2$	Si_3N_4	Total Thickness
QDG QDC NVM	50Å*4=200Å	25Å+50Å =75Å	0	275Å
QDC FET	50Å*2=100Å	200Å	25Å	325Å
Con. FET (200Å)	200Å	0	0	200Å
Con. FET (300Å)	300Å	0	0	300Å

Table 5.2. Gate Structures of Four Devices

These devices had more than 200Å total thickness, and no electron leakage.

5.7. References

[1] F.C. Jain and F. Papadimitrakopoulos, US Patent 7,368,370 B2 (2008).

[2] F. Jain, S. Karmakar, P.-Y. Chan, E. Suarez, M. Gogna, J. Chandy, and E. Heller, "Quantum Dot Channel (QDC) Field-Effect Transistors (FETs) Using II-VI Barrier Layers." *J. Electronic Materials*, 41, 10, pp. 2781-2782 (2012).

[3] R. Shankar, R. Velampati, El-Sayed Hasaneen, E. K. Heller, and Faquir C. Jain, "Floating Gate Nonvolatile Memory Using Individually Cladded Monodispersed Quantum Dots." *IEEE Transactions on very large scale integration (VLSI) Systems*, January 19, 2017.

Chapter 6

Quantum Dot Channel (QDC) Field-Effect Transistors

Analog Behavior Model (ABM)

6.1. Introduction

This chapter describes use of analog behavior model (ABM) developed for QDC-FETs representing their multi-state characteristics. In four states n-QDC-FET, the threshold voltage changes linearly when the gate voltage increases through a range of voltages (Vg1 to Vg2, Vg3 to Vg4). The relationship is showing in equation 1 [1]

$$VT_{EFF} = VT + \Delta VTH \tag{6.1}$$

$$\Delta VT = \begin{cases} 0, & V_{GS} \le Vg1 \\ \alpha1(V_{GS} + Vg1), & Vg1 < V_{GS} \le Vg2 \\ \alpha1(Vg2 + Vg1), & Vg2 < V_{GS} \le Vg3 \\ \alpha1(Vg2 + Vg1) + \alpha2(V_{GS} + Vg3), & Vg3 < V_{GS} \le Vg4 \\ \alpha1(Vg2 + Vg1) + \alpha2(Vg4 + Vg3), & V_{GS} \ge Vg4 \end{cases}$$

Berkeley Short-channel IGFET Model (BSIM3) and Analog Behavioral Model (ABM) libraries are used to establish the n-type QDC-FET model that can address the changing in threshold voltage ΔVT. The output of ABM block represents V_G-ΔVT, the applied gate voltage of the BSIM transistor is equal to the output of ABM block, and the threshold voltage of the BSIM transistor is VT. This approach captures the behavior of the four state n-QDC-FET. The advantage of using the BSIM models is that they can scale to 45 nm and 25 nm with capturing the latest technology advances.

This model is set in hierarchical block and it ready to be used in Cadence-OrCAD CIS as shown in Figure 6.1. The I_{DS}-V_{GS} characteristic of the four states n-QDC-FET is shown in Figure 6.2 (the setting for this circuit as L=1um, W=5um, V_{DD}=3V, VT=0.5, Vg1=1*V_{DD}/3=1V, Vg2=1.5*V_{DD}/3=1.5V, Vg3=2V_{DD}/3=2V, and Vg4=2.5*V_{DD}/3=2.5V). The simulation result shows the four regions (OFF-MOD1-MOD2-ON) of the transfer characteristics.

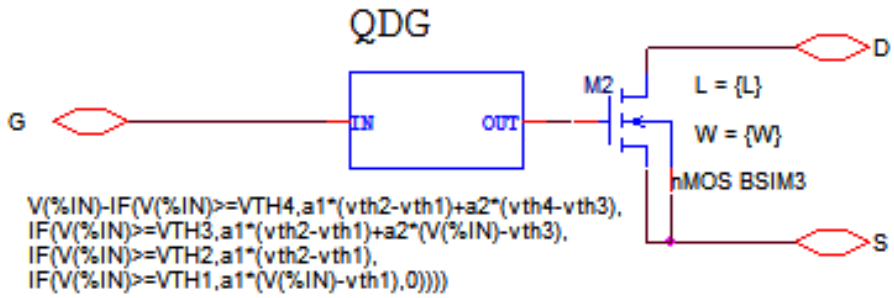


Figure 6.1. BSIM Four-State n-QDC-FET Model Circuit

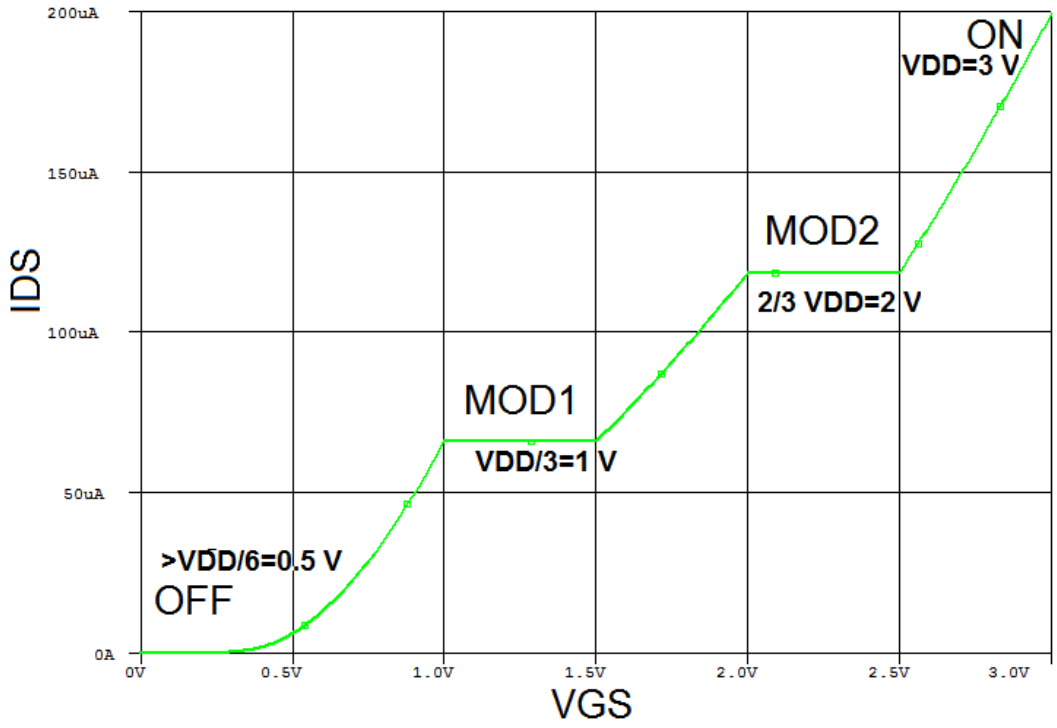


Figure 6.2. 1µm Four-State n-QDC-FET I_{DS}-V_{GS} Characteristics

6.2. Quaternary Inverter

The four state QDC-FETs are suitable for the quaternary logic application with less complex and more efficient than existing quaternary logic circuits. The quaternary inverter logic circuit and its transfer characteristics are shown in Figure 6.3 and Figure 6.4, respectively. The input single is regenerated by inverting the output of the circuit in Fig.6.3 using other four state inverter, the regenerating input signal is showing in Figure 6.4. Figure 6.5 shows the transient time simulation of the quaternary inverter logic.

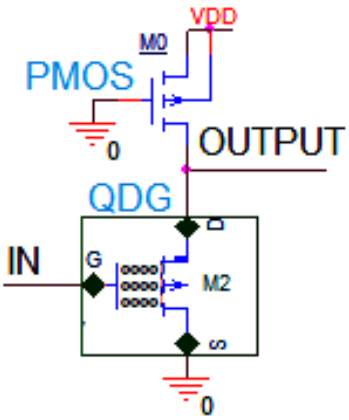


Figure 6.3. Four State n-QDC-FET Inverter Circuit.

The four state inverter comprising of p-MOS and four states n-QDC-FET (pseudo-nMOS). If Vin<VDD/3, the output of the inverter is VDD (Logic3). When VDD/3 < Vin > 2*VDD/3, the output of the inverter is 2*VDD/3 (Logic2). The inverter output is VDD/3 (Logic2) when Vin ≈ VDD/3, the output of the inverter is <VDD/3 (Logic0) if the input is >2*VDD/3.

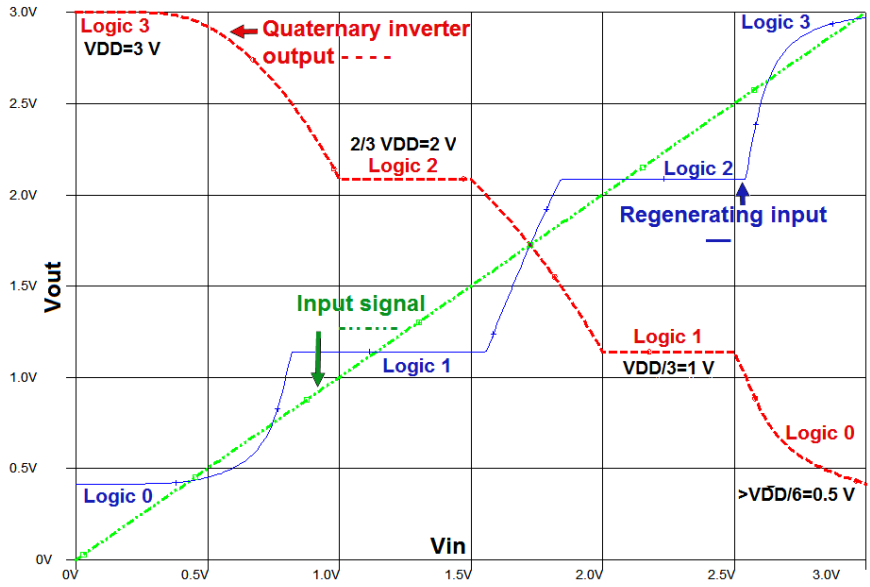


Figure 6.4. Transfer Characteristic of Four State n-QDC-FET Inverter.

Figure 6.5 shows the transient time simulation of the quaternary inverter logic.

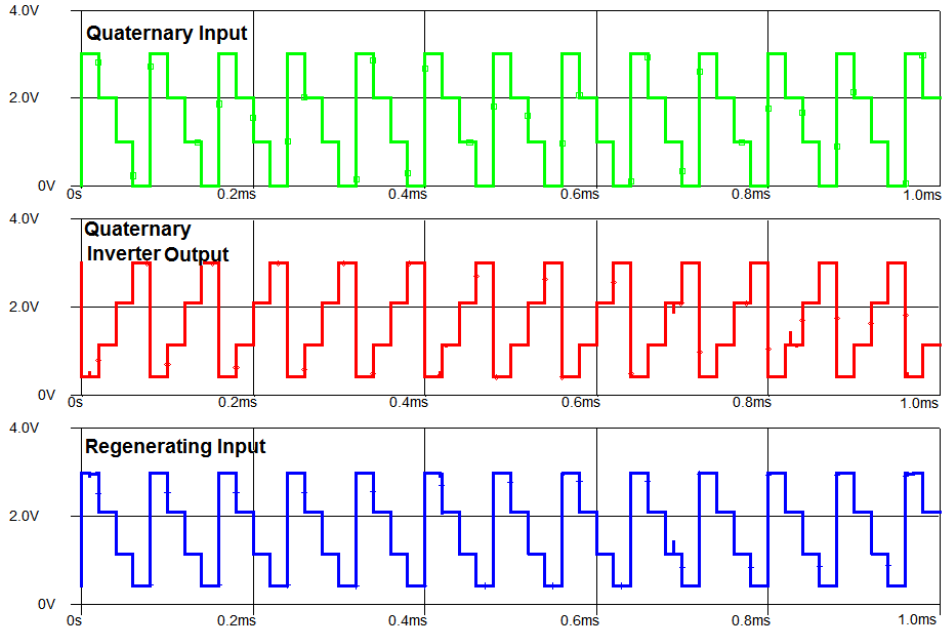


Figure 6.5. Transient Time Simulation of Quaternary Inverter Logic

6.3. 2-Bit SRAM

The conventional 1 bit SRAM consists of two conventional-coupled COMS Inverters for the memory implementation, the same circuit can be used to make 2 bit SRAM by replacing the COMS Inverter with a four state n-QDC-FET inverter as showing in Figure 6.6.

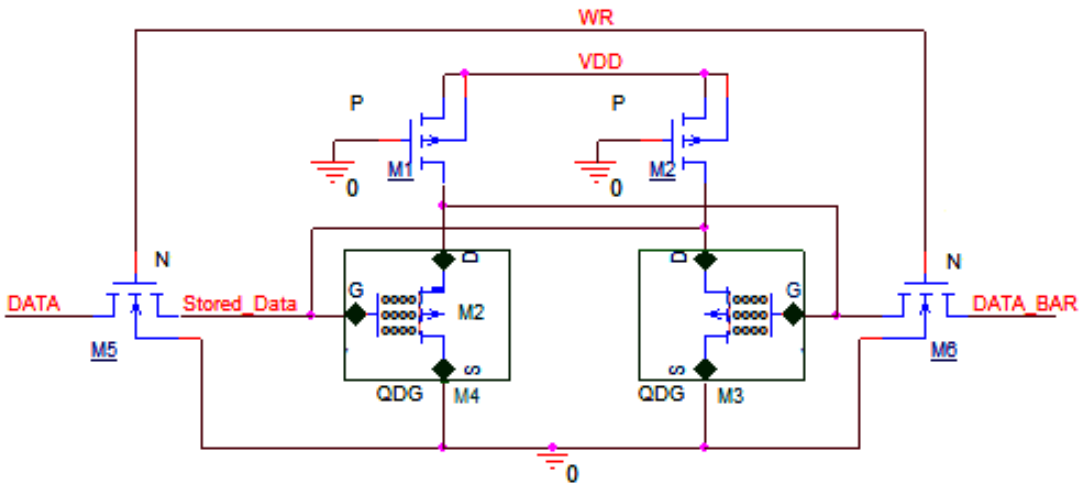


Figure 6.6. The two bit SRAM 6T cell using n-QDC-FET inverter.

Figure 6.7 shows transient simulations of the 2-bit SRAM using a 6T (transistor) cell. In case of the “Write” input signal is on (=VDD), a stored data signal flows a data input signal. When the “Write” input signal is switched off (=0), the voltage/logic stays at the storage node. The simulation result depicts the 2-bit SRAM stored the data as expected.

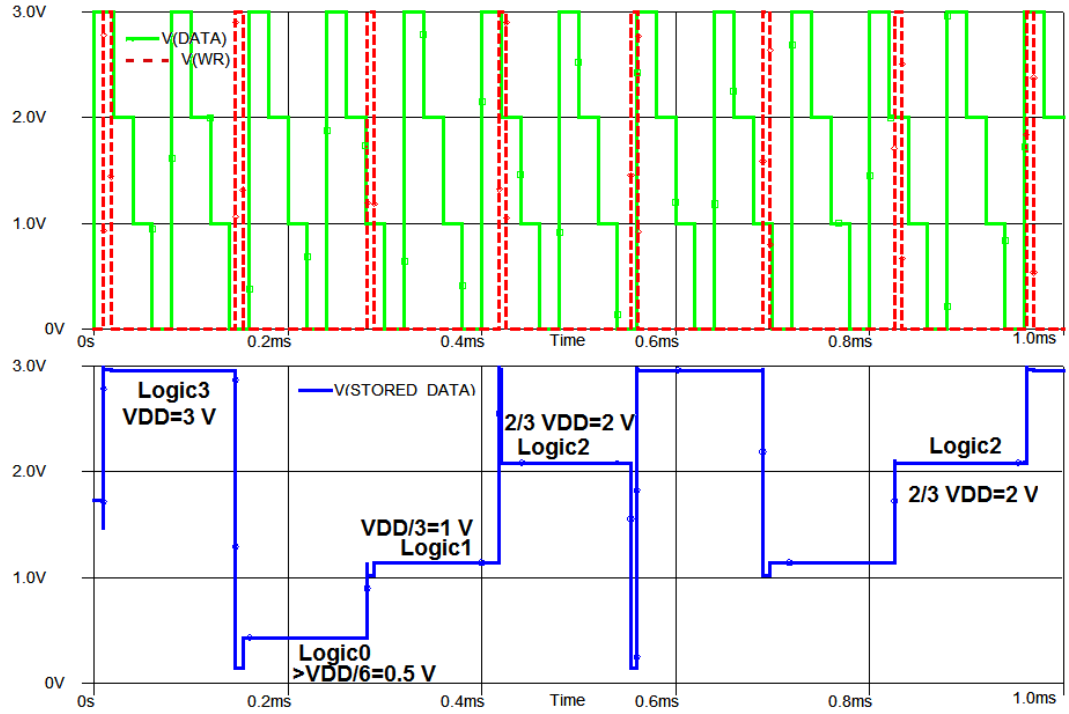


Fig. 6.7 Simulation of 2-bit SRAM

6.4 References

The information in Chapter 6 was extracted from the report e-mailed by Dr. Bander Saman on April 17, 2017.

Chapter 7

Conclusion and Future Plan

7. Conclusion and Future Plan

7.1. Conclusion

The FET comparison chart is shown in Figure 7.1 [1,2], and the NVM comparison chart is shown in Figure 7.2 [3,1,4]. The conclusion of this project is stated below;

1. Germanium QDC FETs were fabricated on poly-silicon and exhibited comparable electron mobility to silicon QDC FETs fabricated on crystal silicon. The I-V characteristics of germanium QDC FET on a poly-silicon substrate are shown at the first row of Figure 7.1. The I-V characteristics of silicon QDC FET on a crystal silicon substrate are shown at the second row of Figure 7.1 [1]. The germanium QDC FET on a poly-silicon substrate exhibits the mobility which is comparable to the silicon QDC FETs on a crystal silicon substrate.
2. Ge QDC NVM exhibited greater threshold shift and potential for multi-bit operation. The I-V characteristics of QDC NVM using germanium quantum dots is shown at the first row in Figure 7.2 [3]. The maximum threshold voltage shift ΔV_{TH} in I-V characteristics was approximately 0.9V at the drain current of 246μA [3]. Also, the I-V characteristics of QDC NVM using silicon quantum dots is shown at the second row in Figure 7.2 [1]. The maximum threshold voltage shift ΔV_{TH} in I_D-V_G characteristics was approximately 1.8V at the drain current of 50μA [1]. These greater threshold shifts exhibit potential for multi-bit operation.
3. Quantum simulations were performed, and analog behavioral models (ABM) were recently developed.

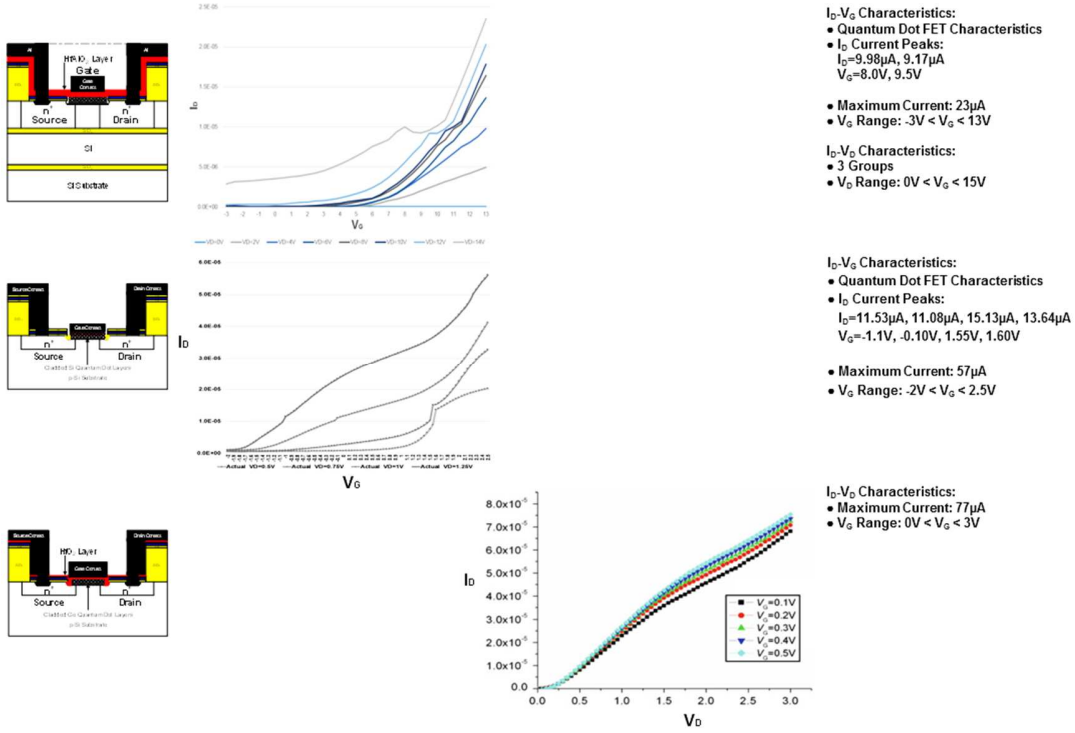


Figure 7.1. FET Comparison Chart

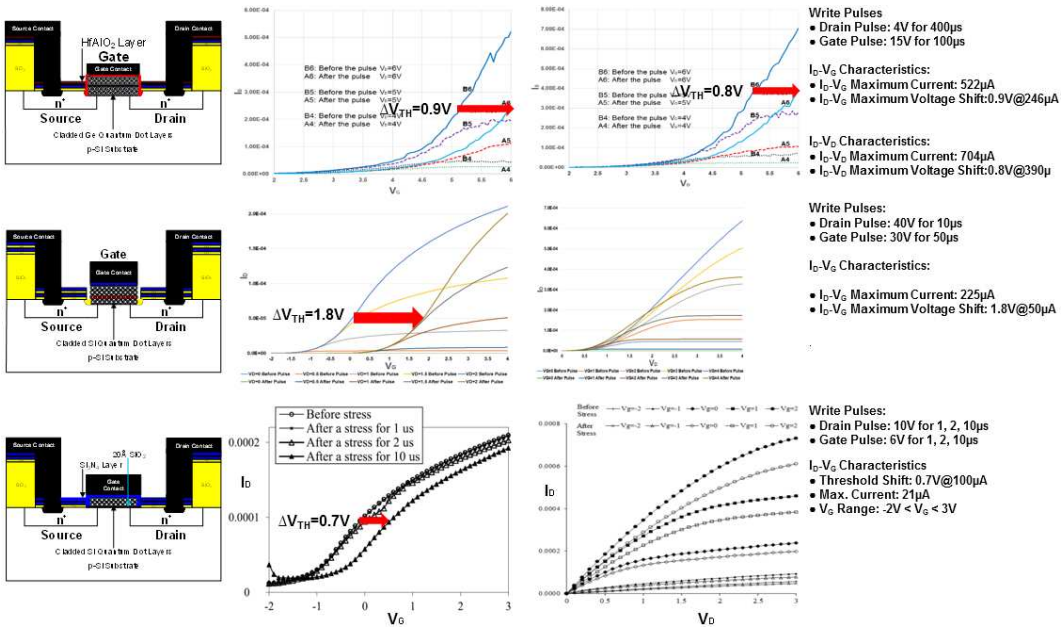


Figure 7.2. NVM Comparison Chart

7.2. Future Plan

The future plans of this project are stated as follows;

1. Development of multi-state logic circuits using QDC-FETs

   The four state inverter comprising of p-MOS and n-QDC-FET was successfully designed using the ABM model. Also, the two-bit SRAM comprising of two p-MOS, two n-MOS, and two QDC-FETs was successfully designed using the ABM model. This work will be extended to the applications other devices.

2. Multi-bit NVM memories on a poly-silicon substrate

   The germanium QDC FET on a poly-silicon substrate was successfully fabricated, and the mobility is comparable to the silicon QDC FET on a crystal silicon substrate. Therefore, the germanium QDC NVM on a poly-silicon substrate will be fabricated in order to reduce the fabrication cost.

3. Demonstration of QDC FETs and NVMs below 130 nm.

   Presently, most of the devise are fabricated using the 60µm x 60µm gate size. The device size must be significantly reduced in the future.

4. Investigate wrap-around Gate QDC FETs.

   Wrap-around Gate QDC FETs will be fabricated in order to reduce the interfacial trapped charge density, and the threshold variability ΔV_{TH} to improve the noise margins of logic gates.

7.3. References

[1] J. Kondo, M. Lingalugari, P.-Y. Chan, E. Heller, F. Jain, "Quantum Dot Channel (QDC) Field Effect Transistors (FETs) and Floating Gate Nonvolatile Memory Cells," *Journal of Electronic Materials*, Volume 44, Number 9, pp. 3188-3193, 2015.

[2] F. Jain, S. Karmakar, P.-Y. Chan, E. Suarez, M. Gogna, J. Chandy, and E. Heller "Quantum Dot Channel (QDC) Field-Effect Transistors (FETs) Using II-VI Barrier Layers." *Journal of Electronic Materials*, Vol. 41, No. 10, 2780-2781, 2012.

[3] J. Kondo, M. Lingalugari, P. Mirdha, P.-Y. Chan, E. Heller, and F. Jain, "Quantum Dot Channel (QDC) Field Effect Transistors (FETs) Configured as Floating Gate Nonvolatile Memories (NVMs)," *International Journal of High Speed Electronics and Systems*, 2017, Accepted.

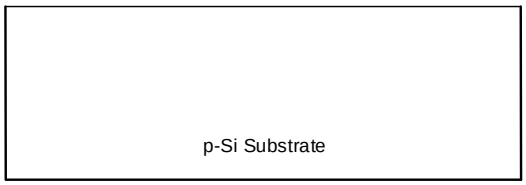
[4] R. Shankar, R. Velampati, El-Sayed Hasaneen, E. K. Heller, and Faquir C. Jain, "Floating Gate Nonvolatile Memory Using Individually Cladded Monodispersed Quantum Dots." *IEEE Transactions on very large scale integration (VLSI) Systems*, January 19, 2017.

Appendix

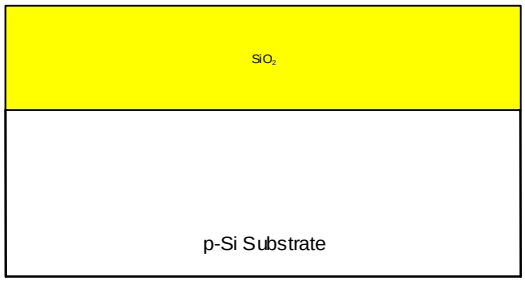
Appendix 1

Conventional FET using Crystal Silicon Substrate

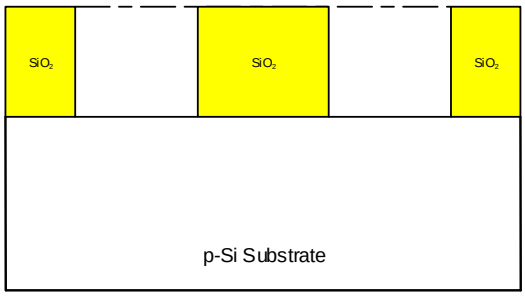
1. P-Type Silicon Substrate



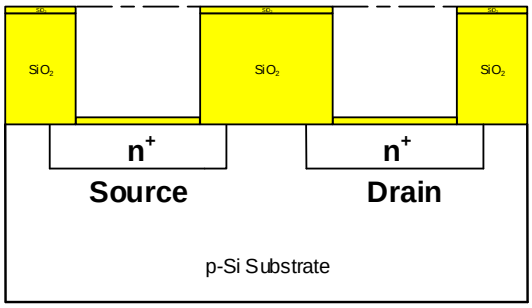
2. 1250Å Wet Oxidation on P-Type Silicon Substrate



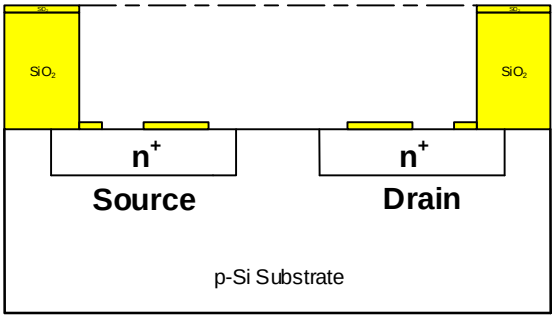
3. Source and Drain Fabrication using Mask 3



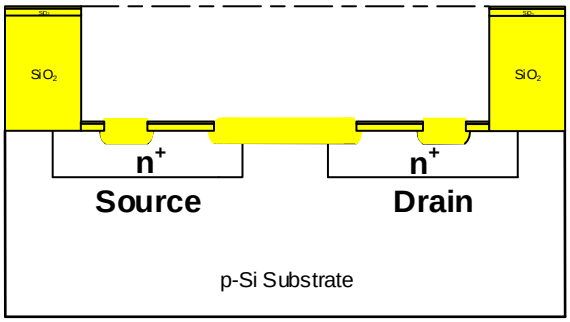
4. Phosphorus Diffusion



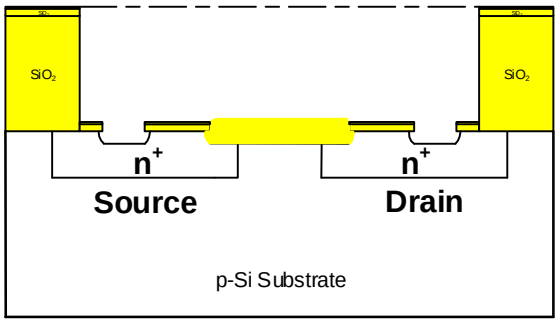
5. Mask 4: Gate Opening
   (Refer to Appendix 5.1: BOE Time Estimate for Gate Opening)



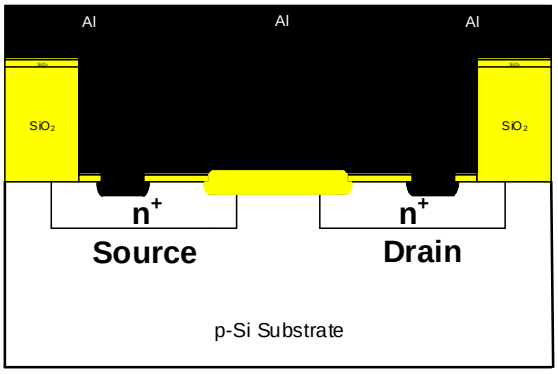
6. Dry Oxidation



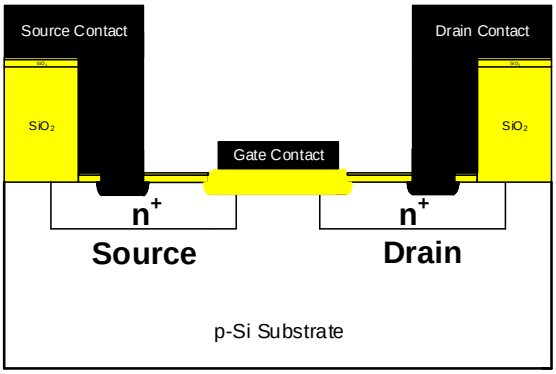
7. Mask 5: Source and Drain Contact Hole
   (Refer to Appendix 6.1: Source and Drain Contact Hole)



8. Metallization



9. Mask 6: Interconnect

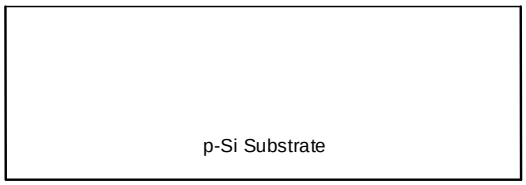


Conventional FET

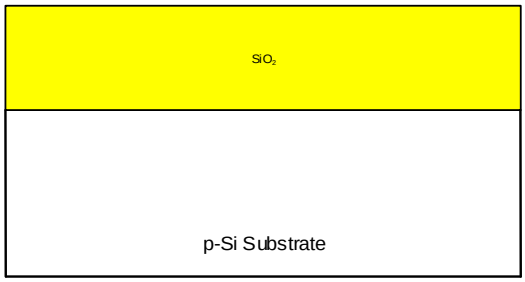
Appendix 2

Trench Fabrication for Crystal Silicon Substrate

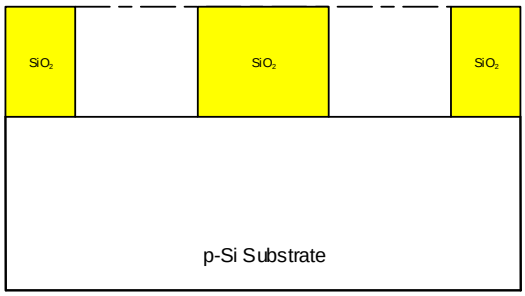
13. P-Type Silicon Substrate



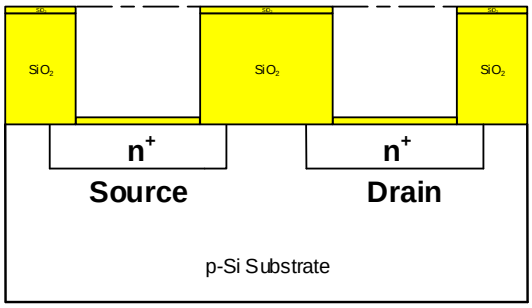
14. 1250Å Wet Oxidation on P-Type Silicon Substrate



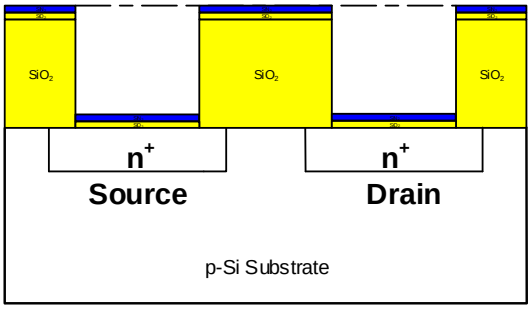
15. Source and Drain Fabrication using Mask 3



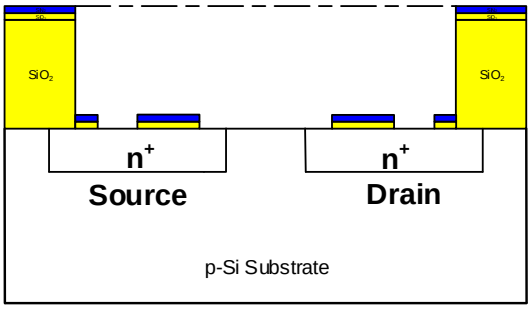
16. Phosphorus Diffusion



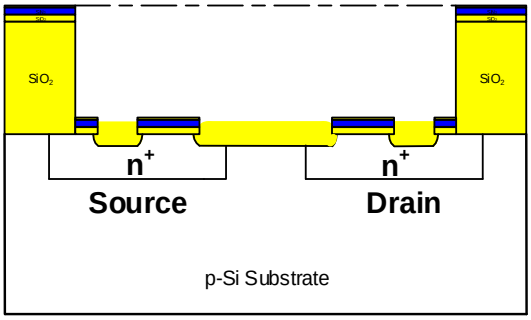
17. 75Å Silicon Nitride Deposition



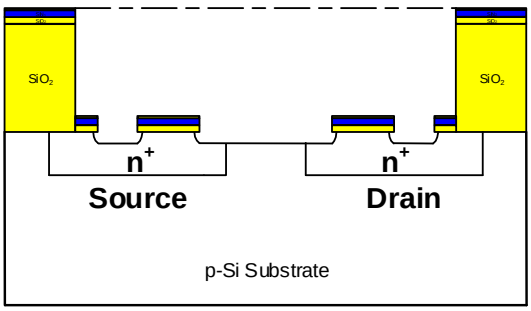
18. Mask 4: Gate Opening, Part 1 (Refer to Appendix 5.2: BOE Time Estimate)



19. 250Å Dry Oxidation



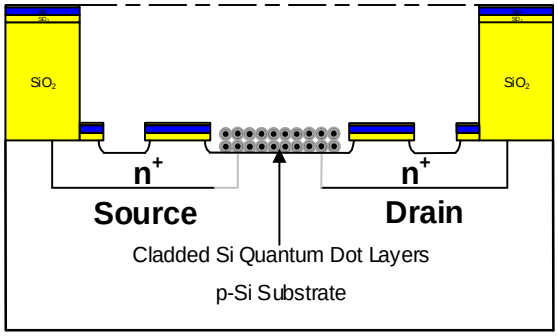
20. Mask 4: Gate Opening, Part 2



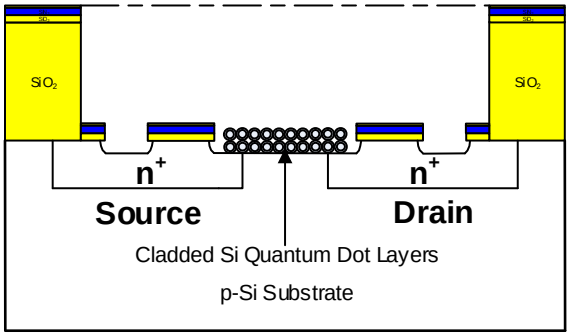
A. QDC FET using Silicon Quantum Dots

9A. Silicon Quantum Dot Deposition

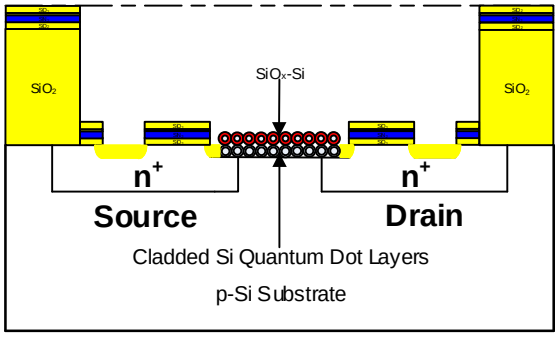
Self-Assembly of Si Quantum Dot Layers



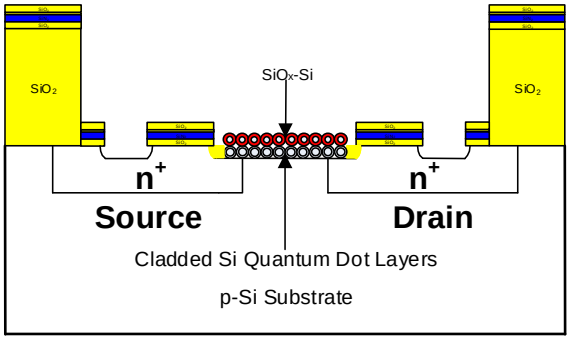
Annealing at 750ºC for 10 minutes



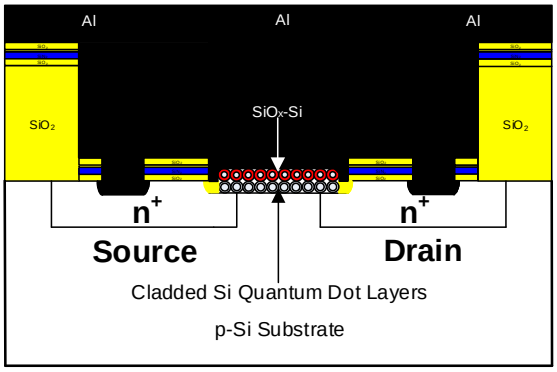
Dry Oxidation at 800ºC for 5 minute



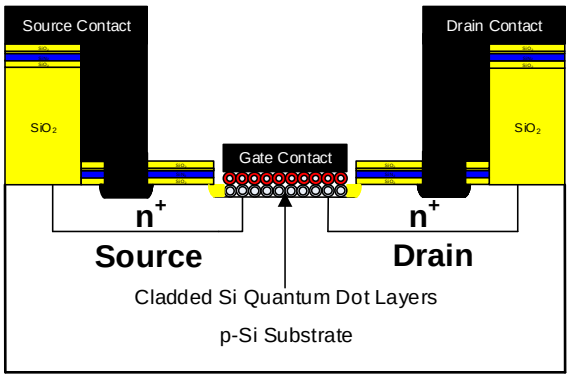
10A. Mask 5: Open Source and Drain Contacts using Mask 5
(Refer to Appendix 6.2: BOE Time Estimate for Contact Holes)



11A. Metallization



12A. Mask 6: Interconnect

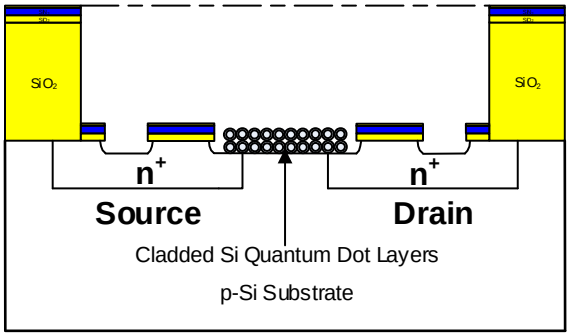


QDC FET using Silicon Quantum Dots

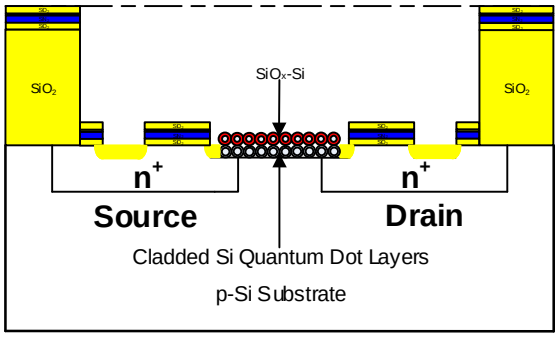
B. QDG-QDC FET using Silicon Quantum Dots

9B. Silicon Quantum Dot Deposition

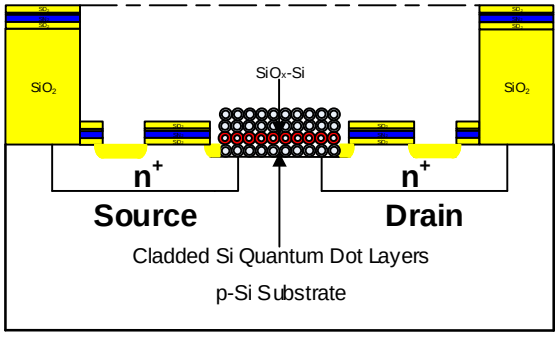
Self-Assembly and Annealing at 750ºC for 10 minutes



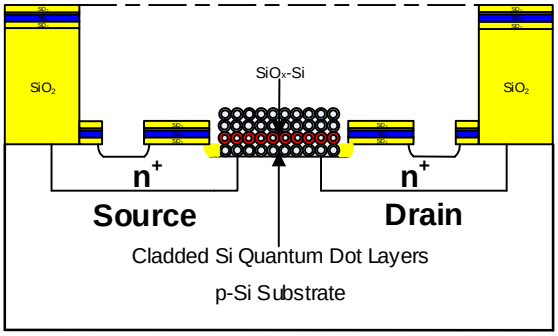
Dry Oxidation at 800ºC for 5 minute



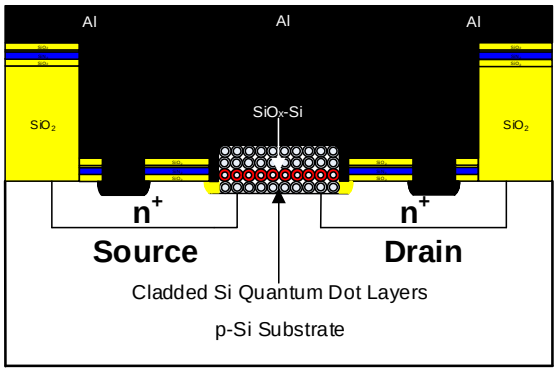
Self-Assembly and Annealing at 750ºC for 10 minutes



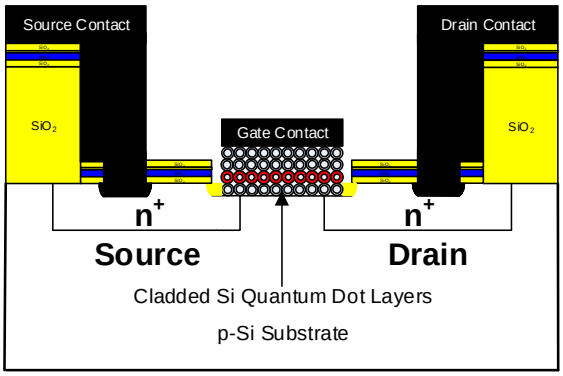
10B. Mask 5: Open Source and Drain Contacts
(Refer to Appendix 6.2: BOE Time Estimate for the Contact Holes)



11B. Metallization



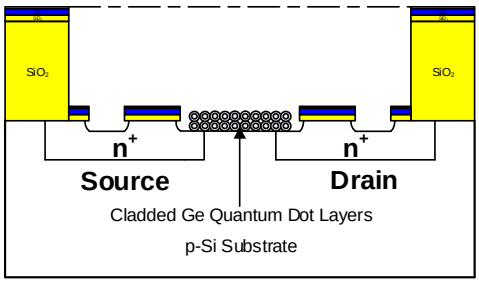
12B. Mask 6: Interconnection



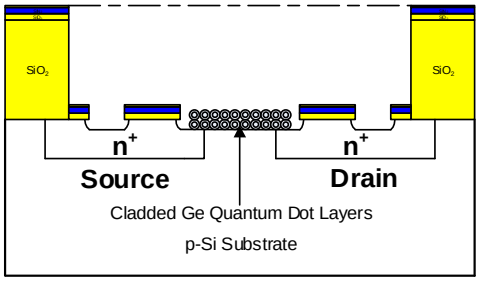
C. QDC FET using Germanium Quantum Dots

9C. Germanium Quantum Dot Deposition for QDC FET

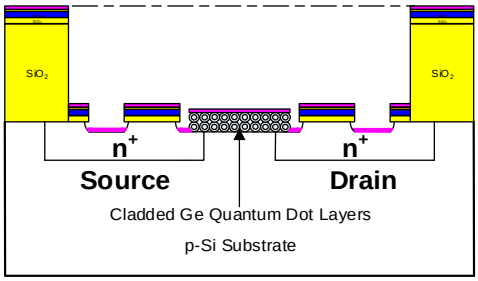
Self-Assembly



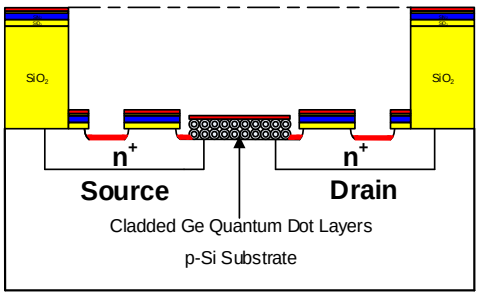
Annealing at 350ºC for 10 minutes



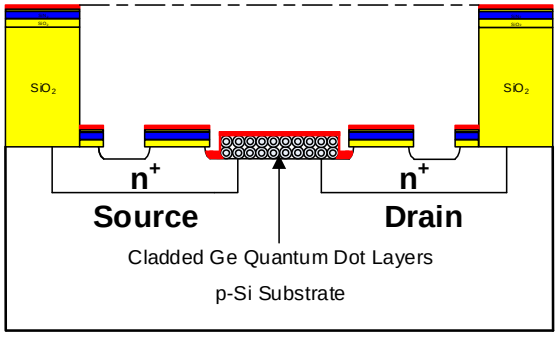
Hafnium Oxide Layer Deposition



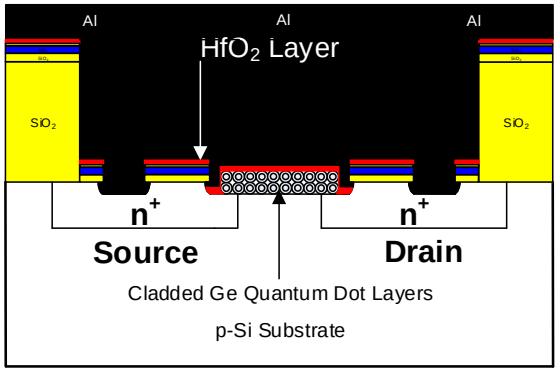
Rapid Thermal Annealing (RTA) at 520 ºC for 10 seconds



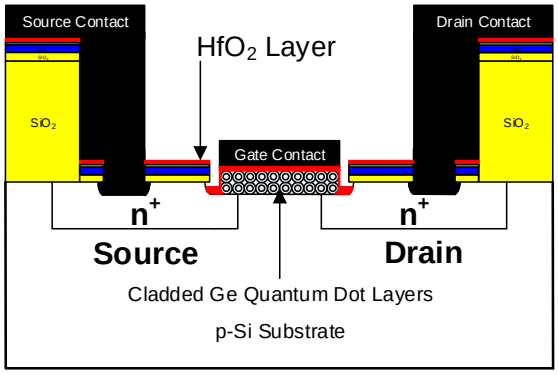
10C. Mask 5: Open Source and Drain Contacts
(Refer to Appendix 6.3: BOE Time Estimate for Contact Holes)



11C. Metallization



12C. Mask 6: Interconnect

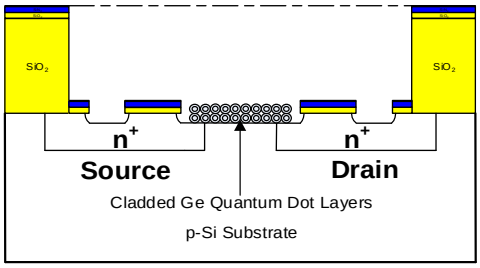


QDC FET using Germanium Quantum Dots

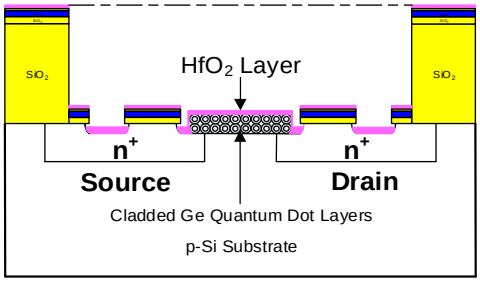
D. QDG-QDC FET using Germanium Quantum Dots

9D. Germanium Quantum Dot Deposition

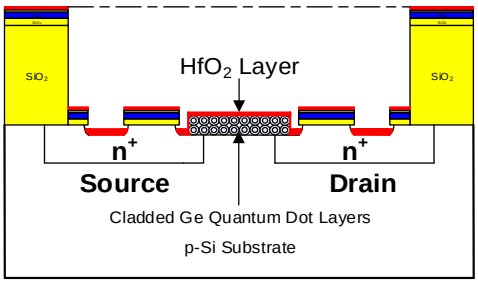
Self-Assembly and Annealing at 350ºC for 10 minutes



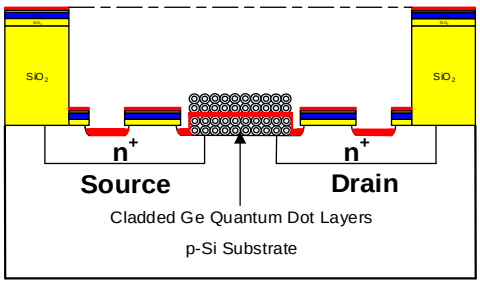
Hafnium Oxide Layer Deposition



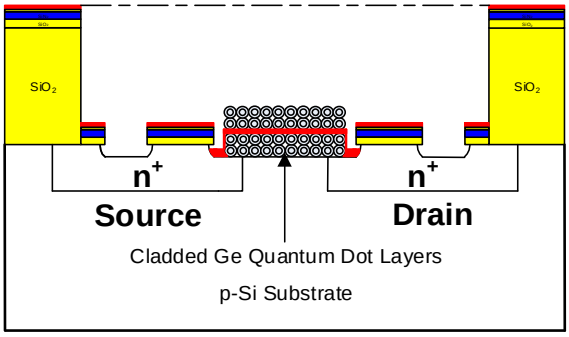
Rapid Thermal Annealing (RTA) at 520ºC for 10 seconds



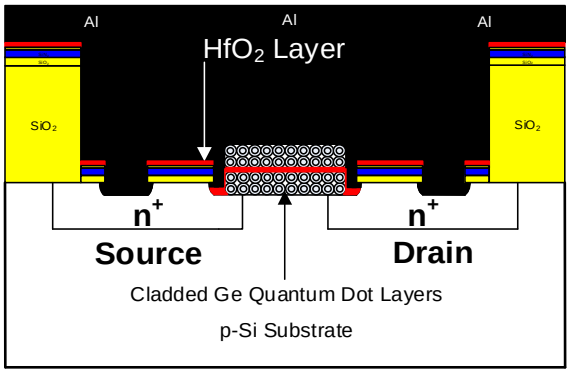
Self-Assembly and Annealing at 350˚C for 10 minutes



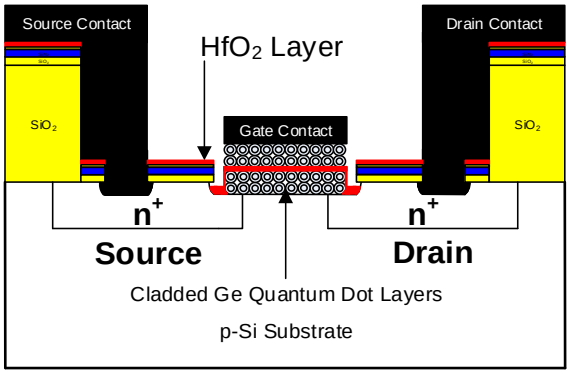
10D. Mask 5: Open Source and Drain Contacts
(Refer to Appendix 6.3: Time Estimate for Contact Holes)



11D. Metallization



12D. Mask 6: Interconnect



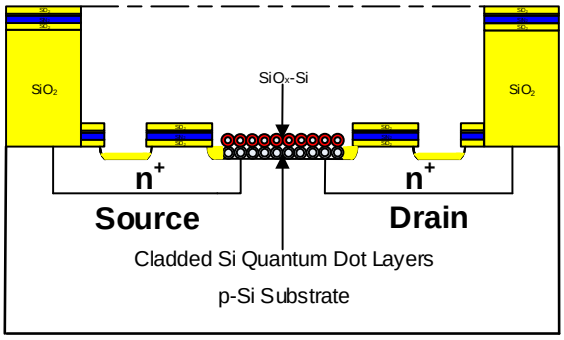
QDG-QDC FET using Germanium Quantum Dots

E. QDG-QDC NVM using Silicon Quantum Dots

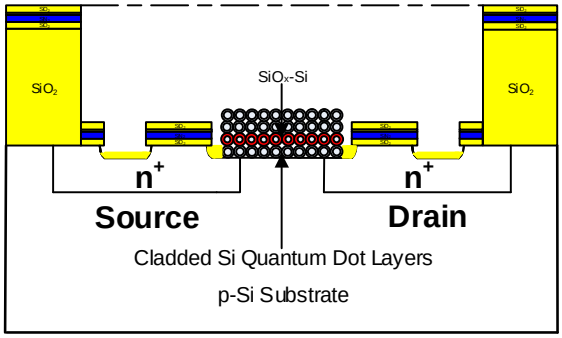
9E. Silicon Quantum Dot Deposition

Self-Assembly and Annealing at 750ºC for 10 min. &

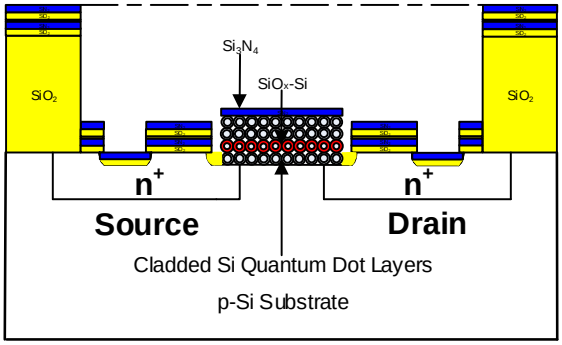
Dry Oxidation at 800ºC for 5 minutes



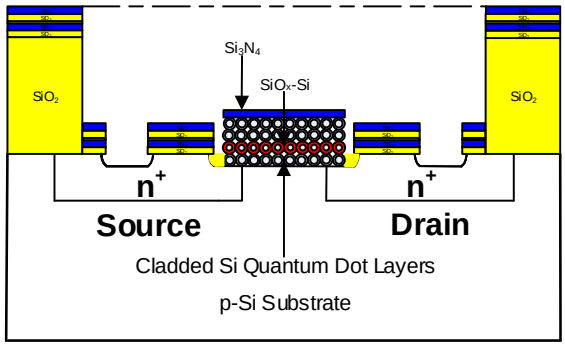
Self-Assembly and Annealing at 750ºC for 10 minute



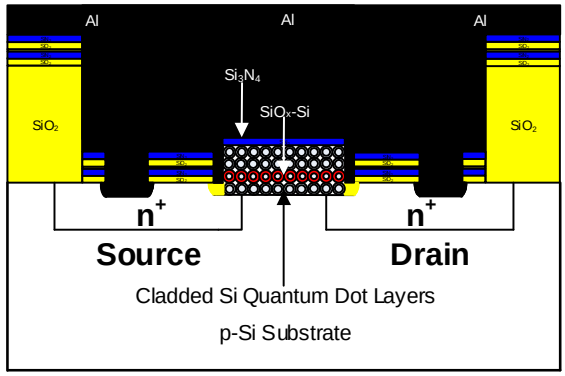
Deposit Silicon Nitride Layer for the Control Dielectric



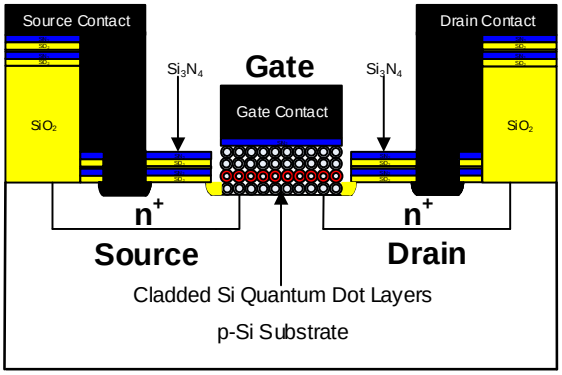
10E. Mask 5: Open Source and Drain Contacts



11E. Metallization



12E. Mask 6: Interconnection

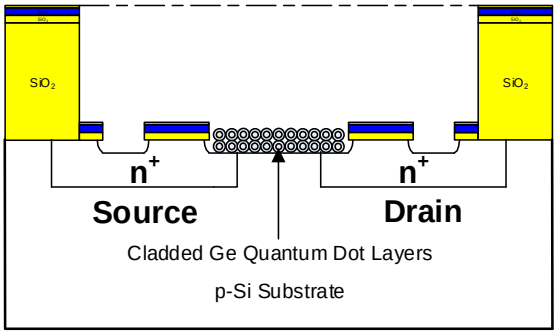


QDG-QDC NVM using Silicon Quantum Dots

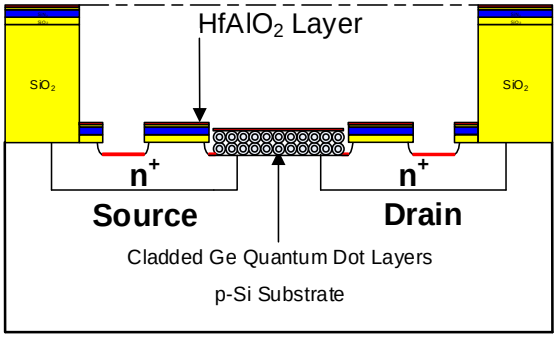
F. QDG-QDC NVM using Germanium Quantum Dots

9F. Germanium Quantum Dot Deposition

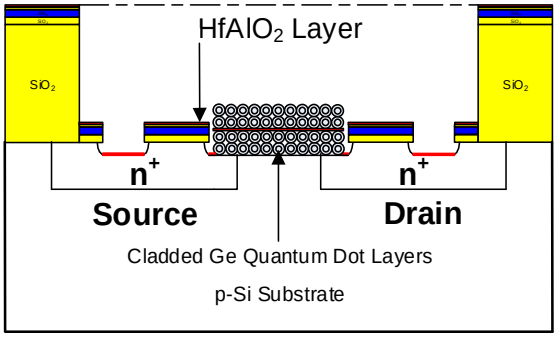
Self-Assembly and Annealing at 350ºC for 10 minutes



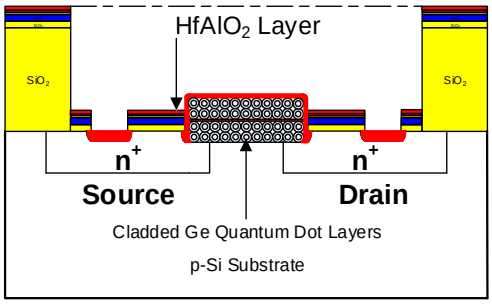
Aluminum Oxide and Hafnium Oxide Deposition



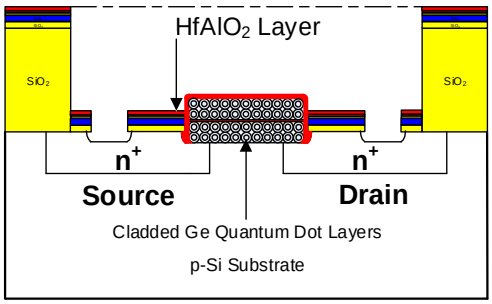
Self-Assembly and Annealing at 350°C for 10 minutes



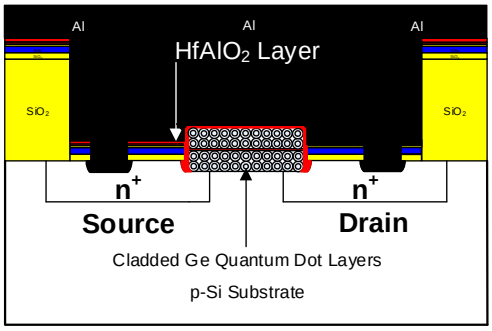
10F. Aluminum Oxide and Hafnium Oxide Deposition



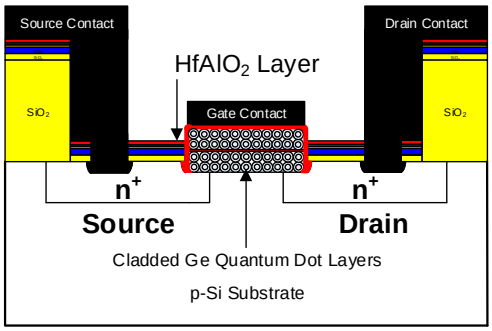
11F. Mask 5: Open Source and Drain Contacts (Refer to Appendix 6.2: BOE Time Estimate)



12F. Metallization



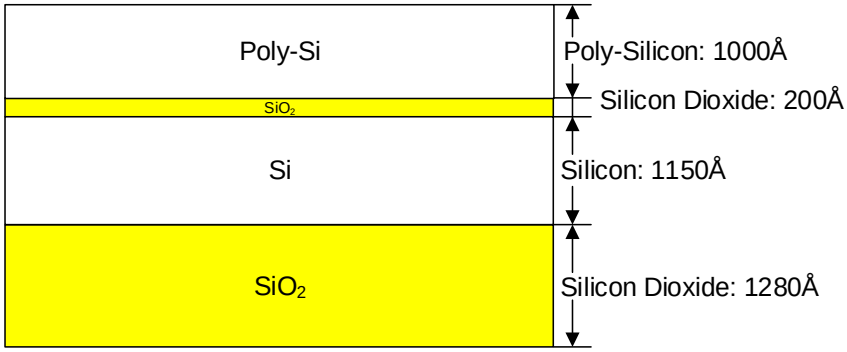
13F. Mask 6: Interconnect



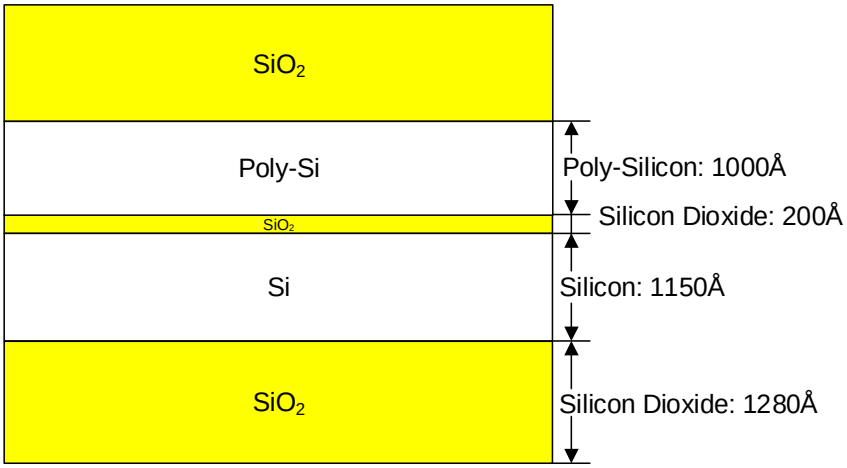
Appendix 3

Conventional FET using Polysilicon Substrate

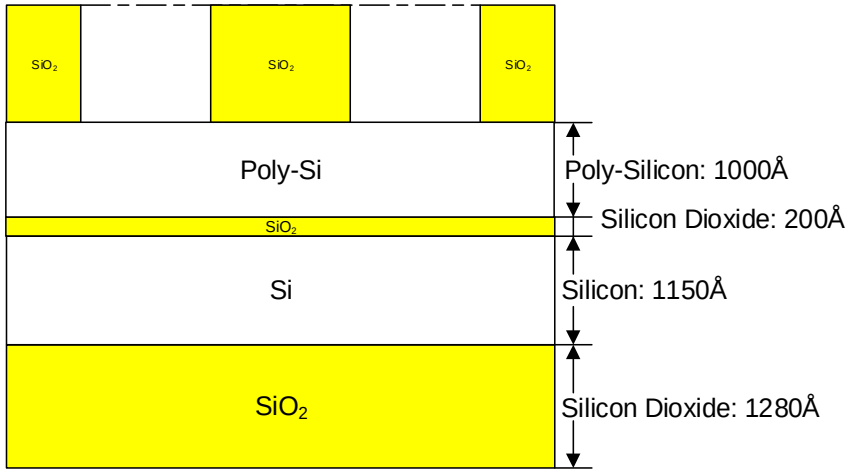
1. Poly-silicon Substrate



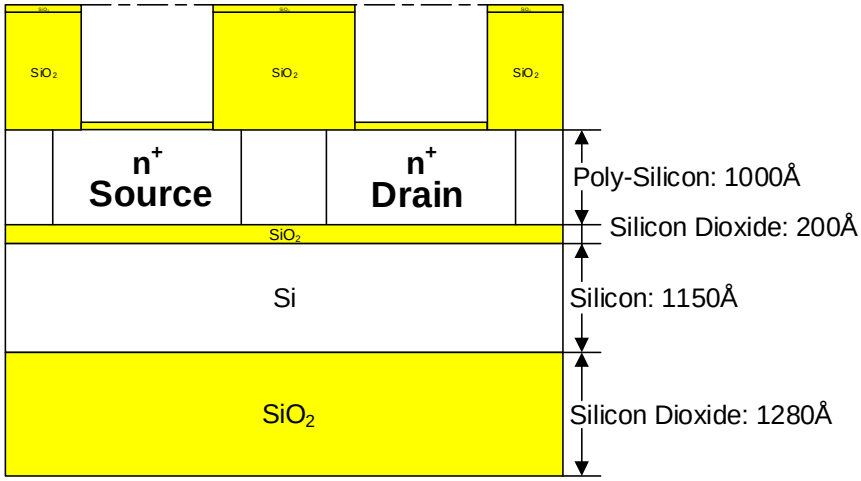
2. 1250Å PECVD Deposition on the Polysilicon Substrate



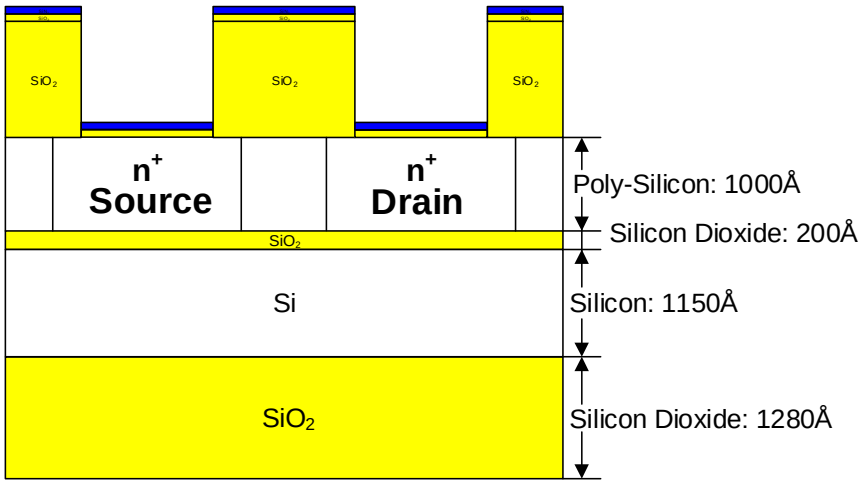
3. Source and Drain Fabrication using Mask 3



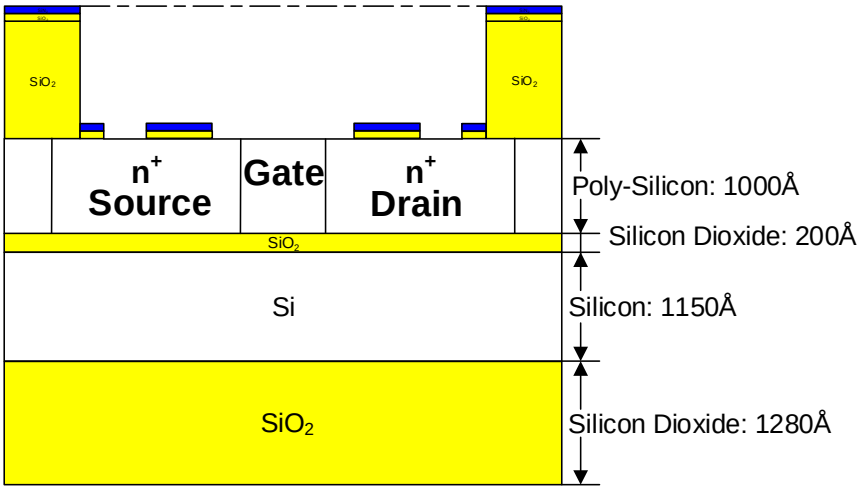
4. Phosphorus Diffusion



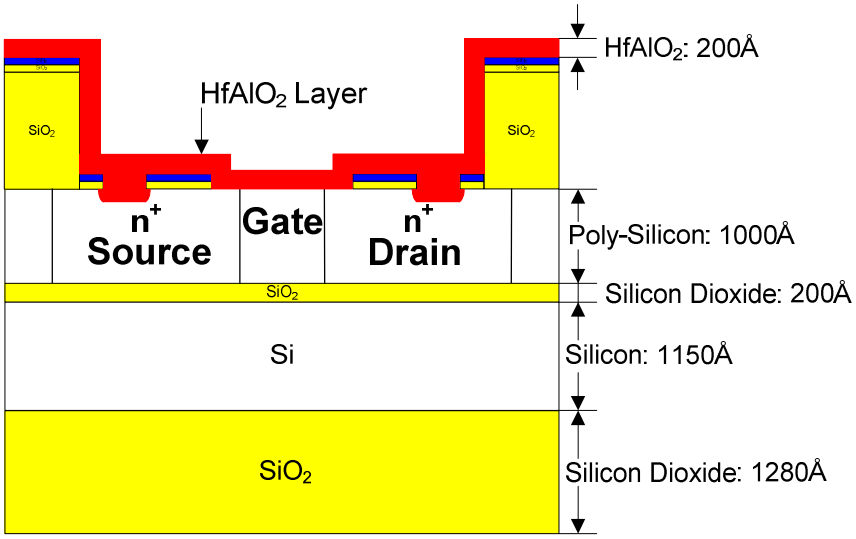
5. 75Å Silicon Nitride Deposition



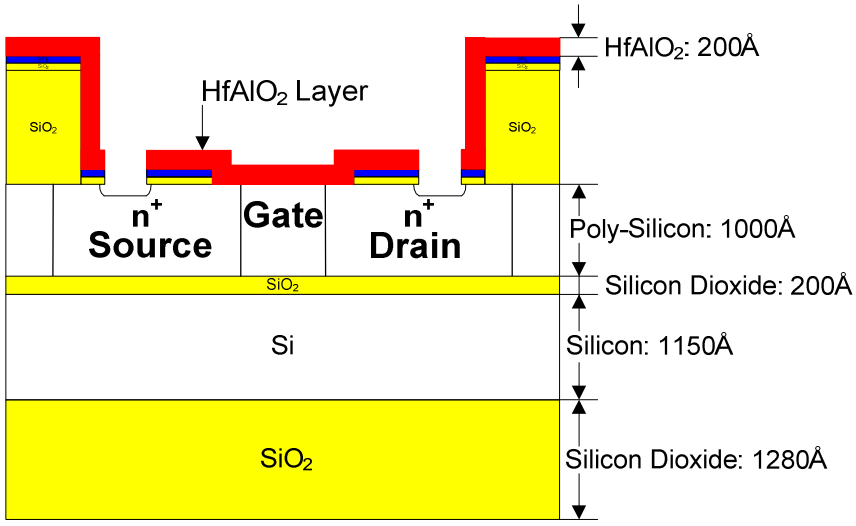
6. Mask 4: Gate Opening



7. Hafnium Oxide/Aluminum Oxide Combinational Layer Deposition for for the Tunnel Oxide

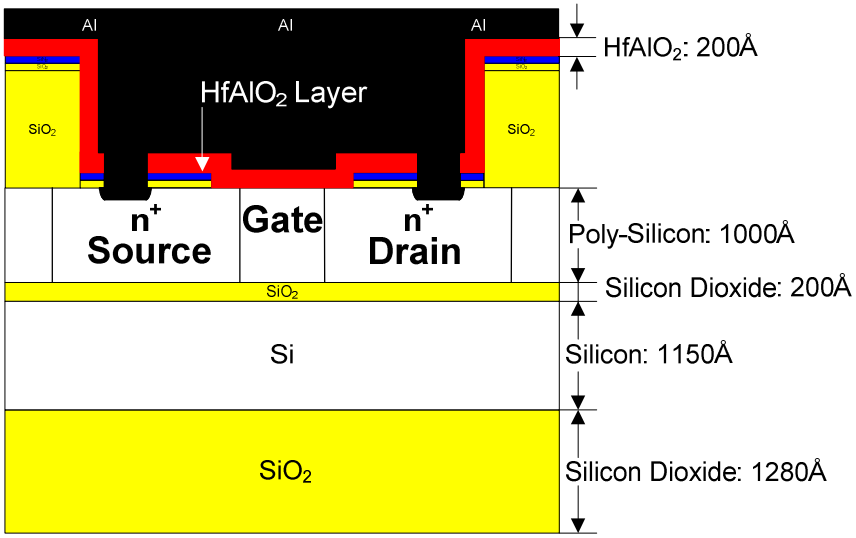


8. Mask 5: Open Source and Drain Contacts

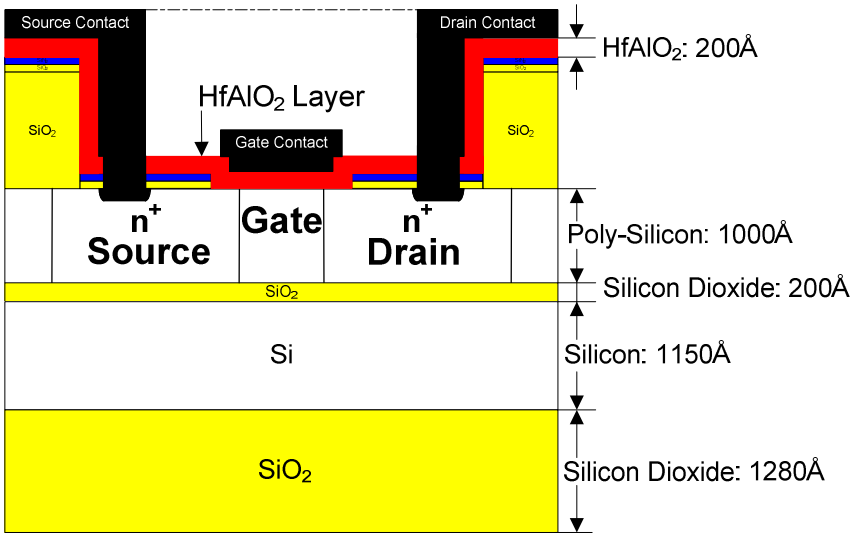


9. Metallization

Self-Assembly of Germanium Quantum Dots



10. Mask 6: Interconnect

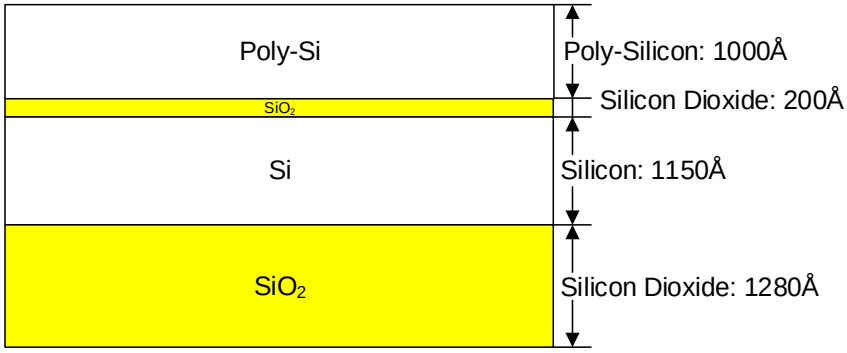


Conventional FET

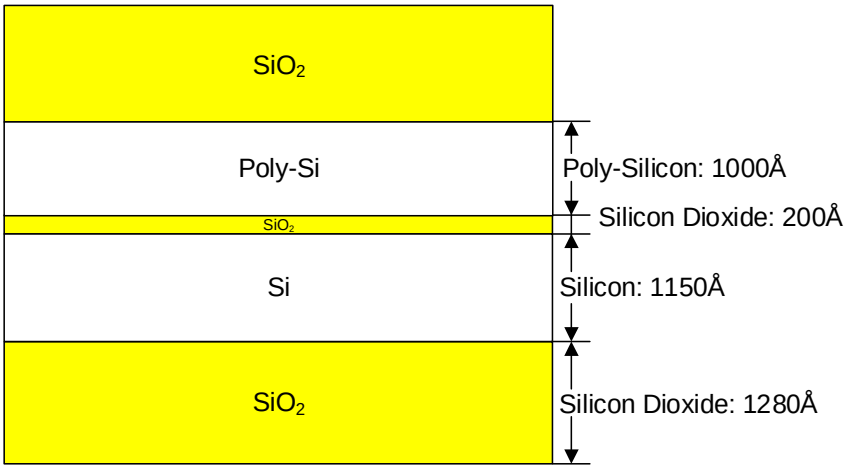
Appendix 4

Trench Fabrication for Poly-silicon Substrate

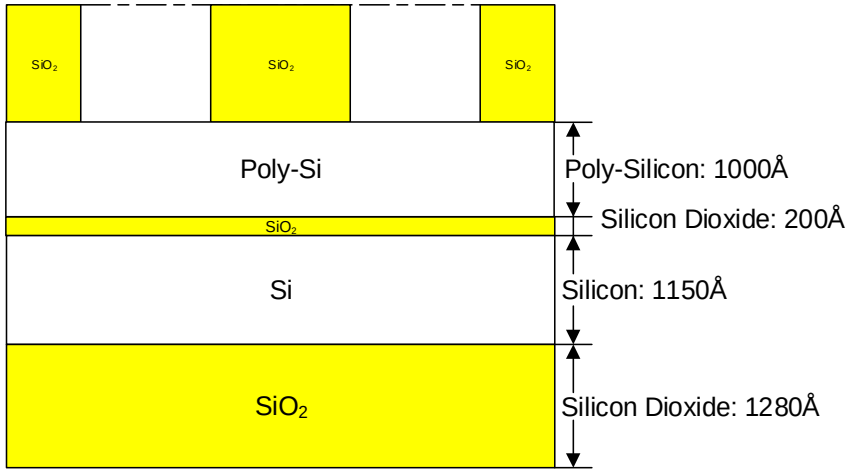
8. Poly-silicon Substrate



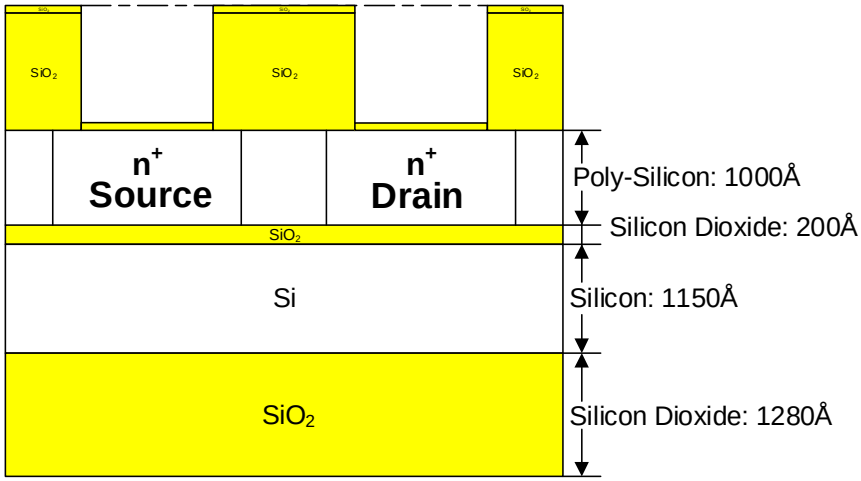
9. 1250Å PECVD Deposition on the Polysilicon Substrate



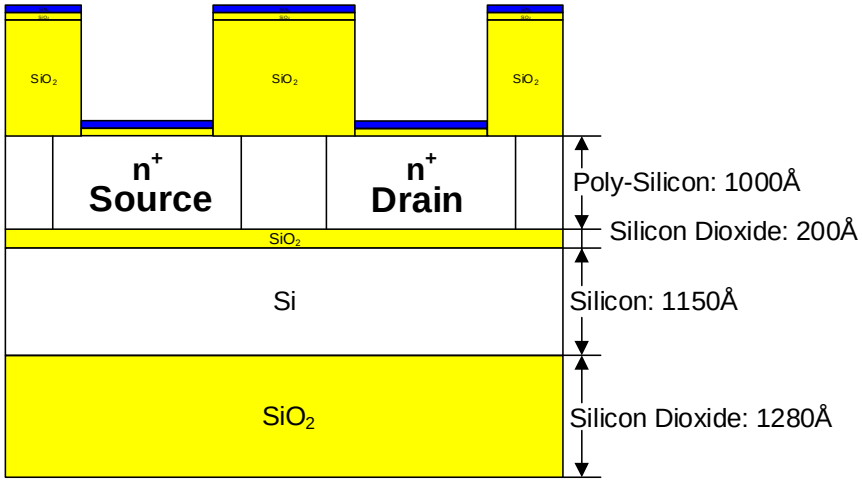
10. Source and Drain Fabrication using Mask 3



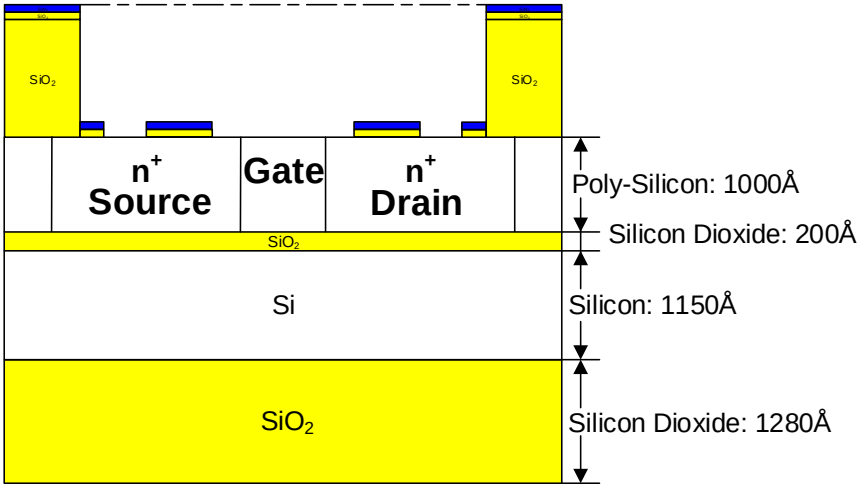
11. Phosphorus Diffusion



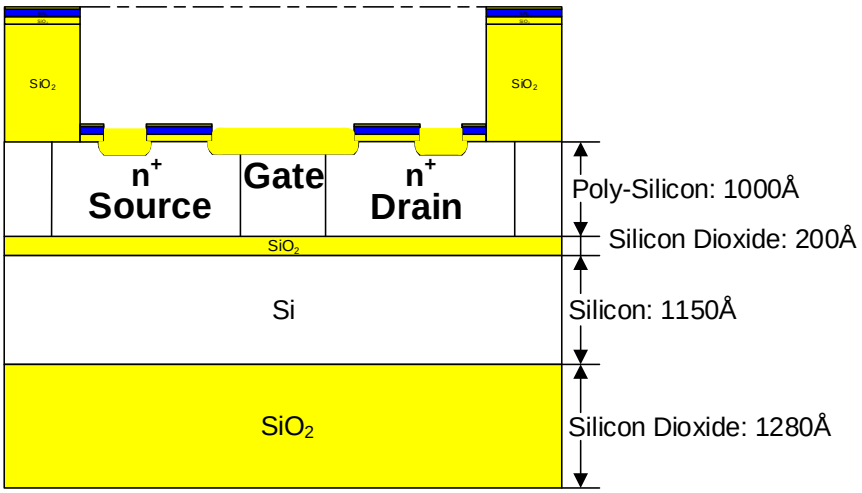
12. 75Å Silicon Nitride Deposition



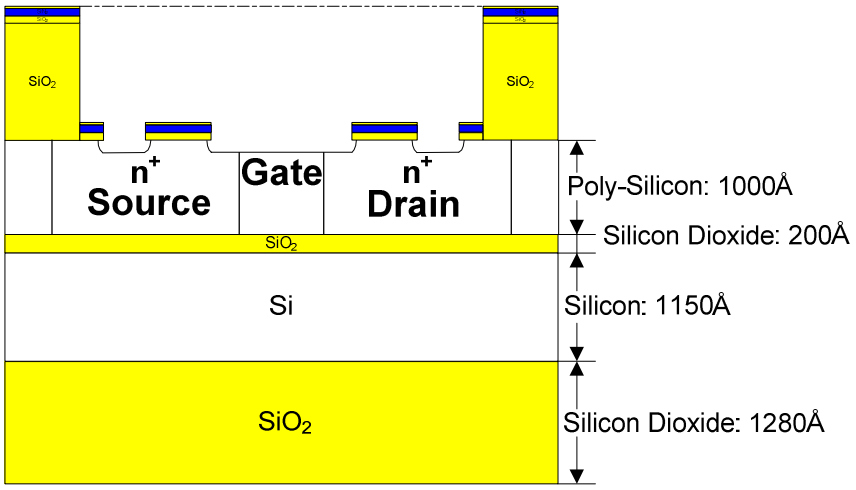
13. Mask 4: Gate Opening, Part 1



14. 250Å Dry Oxidation

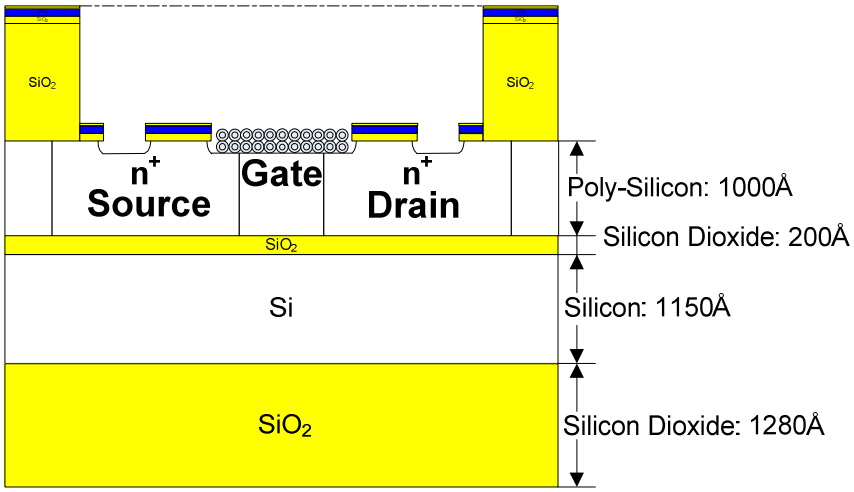


15. Mask 4: Gate Opening, Part 2

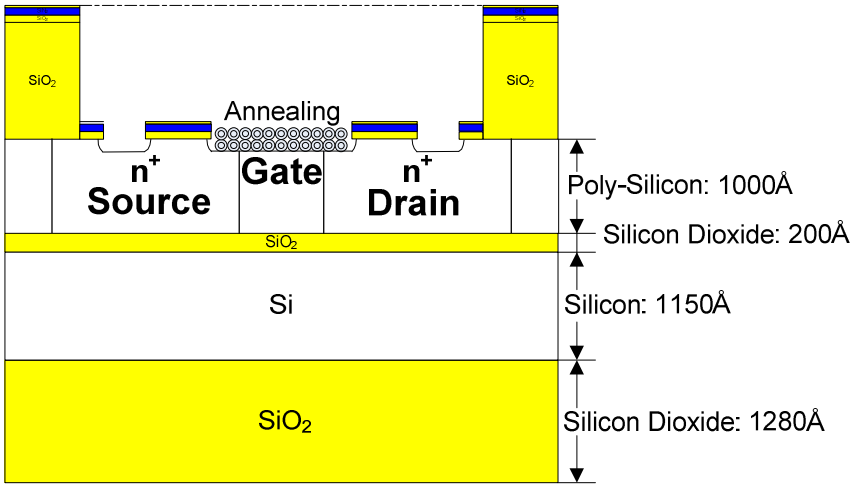


A. QDC FET using Germanium Quantum Dots

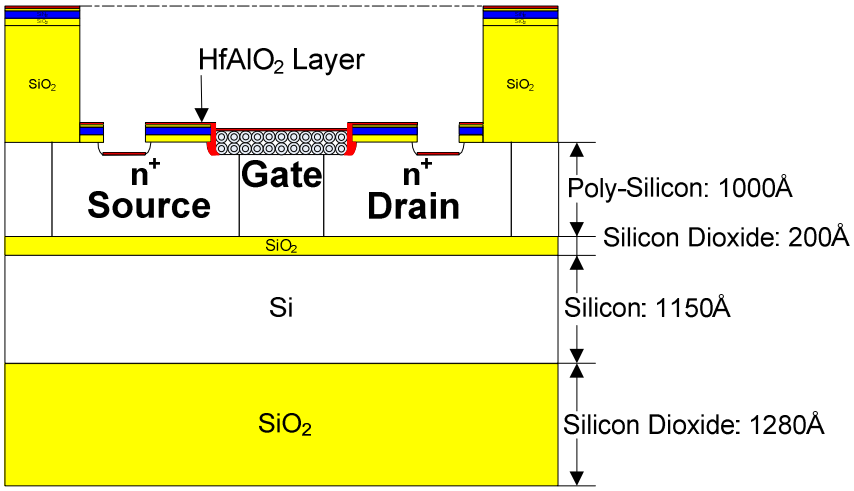
9A. Self-Assembly of Germanium Quantum Dots



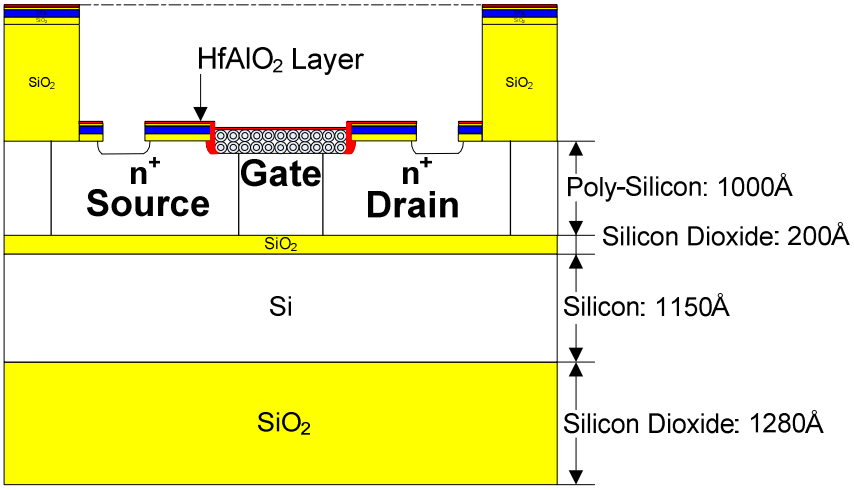
Annealing at 350ºC for 10 minutes



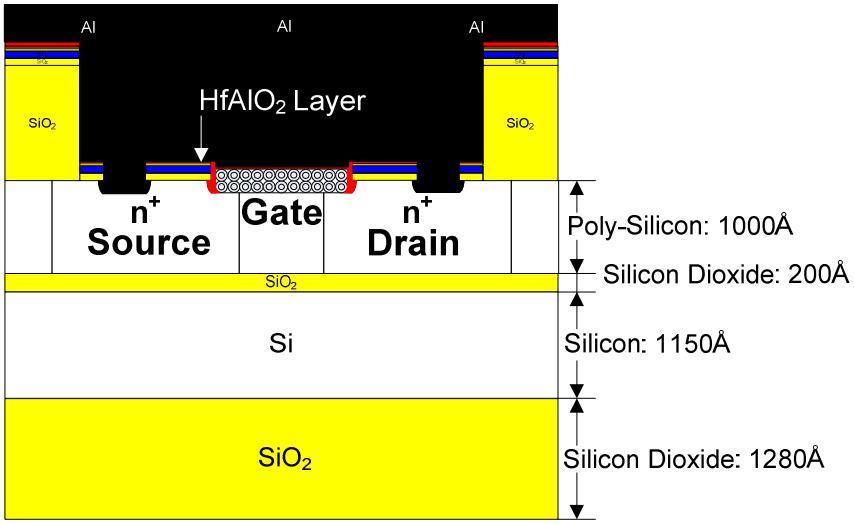
10A. Hafnium Oxide/Aluminum Oxide Combinational Layer Deposition
for the Tunnel Oxide



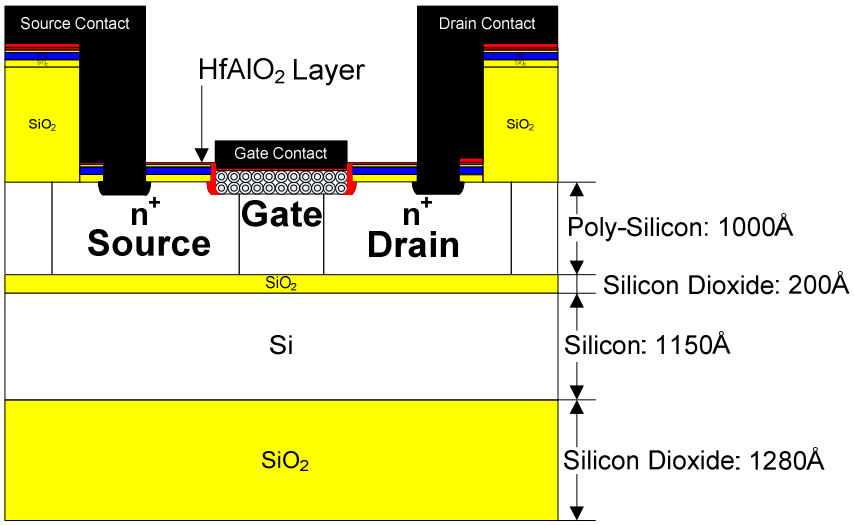
11A. Mask 5: Open Source and Drain Contacts



12A. Metallization



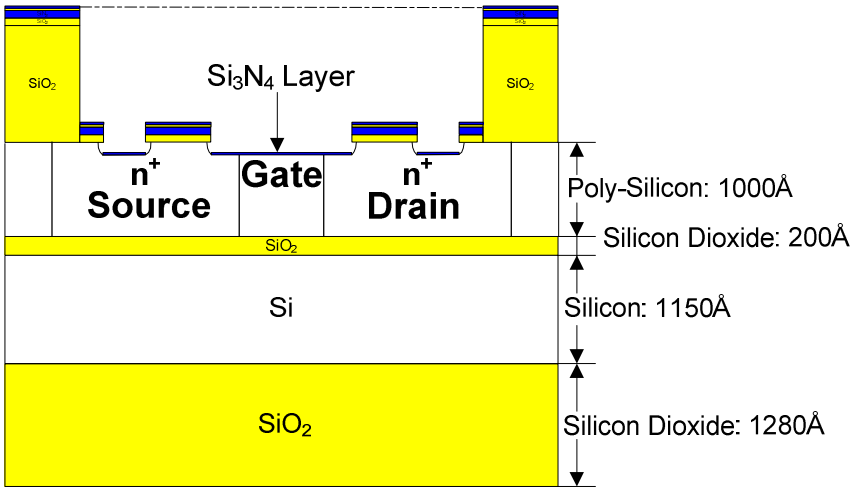
13A. Mask 6: Interconnect



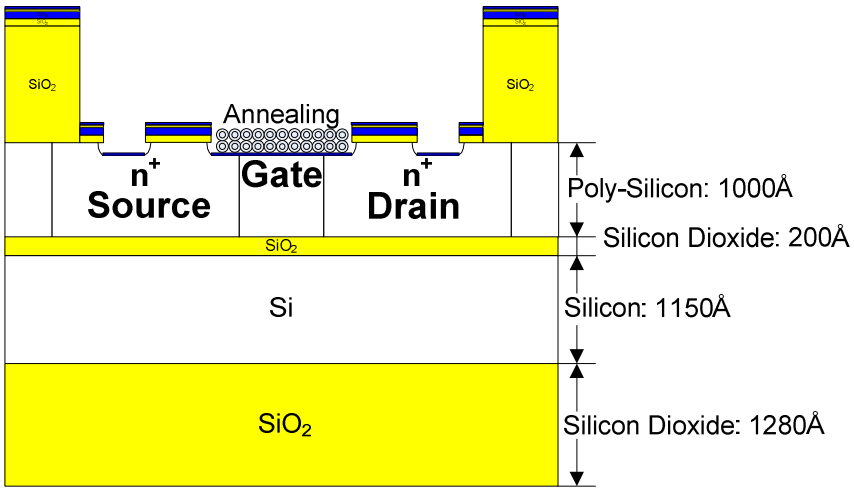
QDC FET using Germanium Quantum Dots

B. QDC FET using Germanium Quantum Dots with Silicon Nitride Insulator

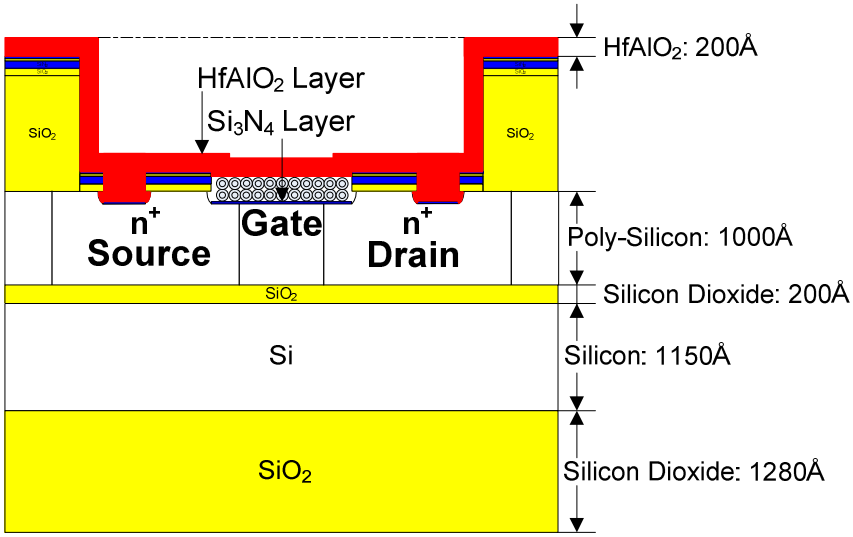
9B. 20Å Silicon Nitride Deposition



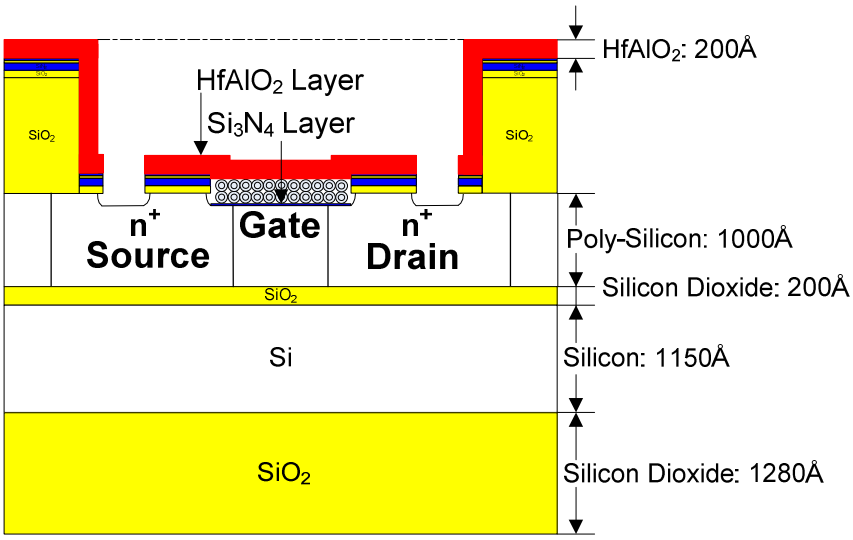
10B. Self-Assembly of Germanium Quantum Dots and Annealing at 350ºC for 10 minutes



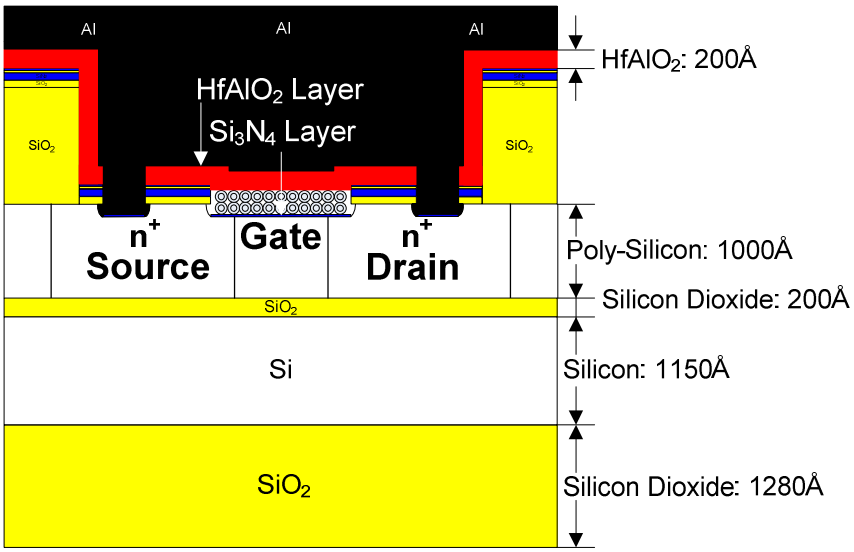
11B. Hafnium Oxide/Aluminum Oxide Combinational Layer Deposition
for the Tunnel Oxide



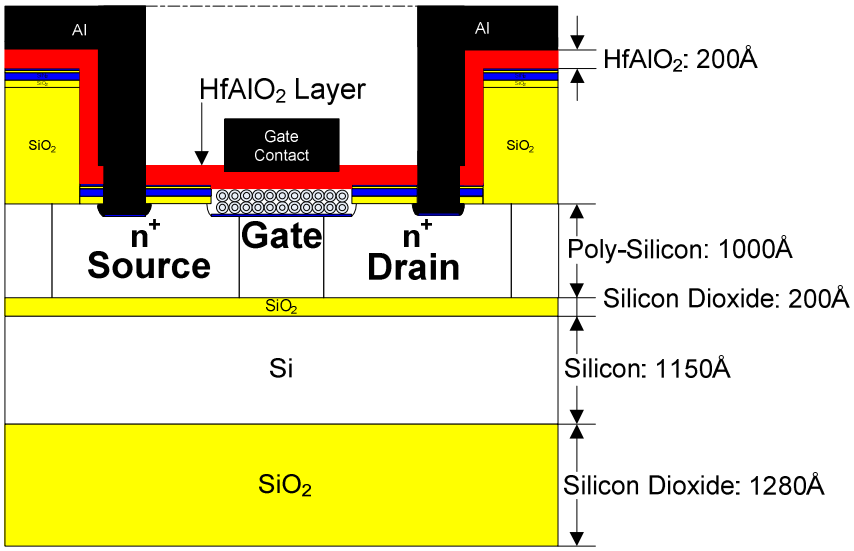
12B. Mask 5: Open Source and Drain Contacts



13B. Metallization

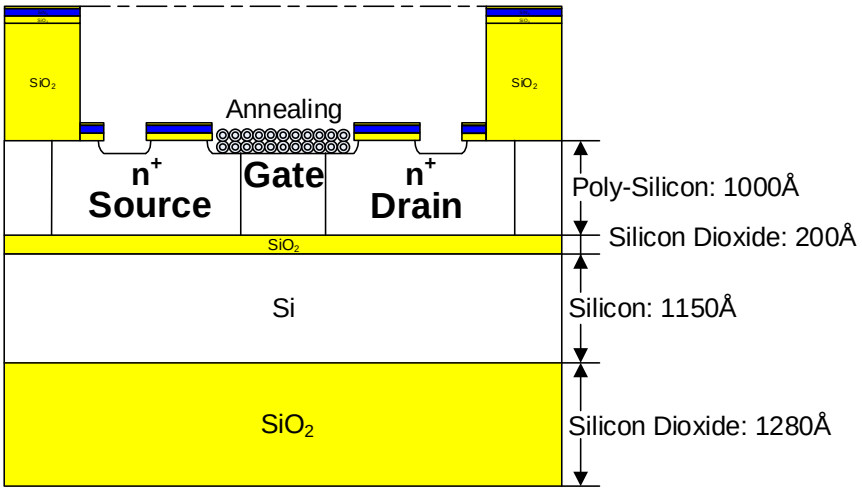


14B. Mask 6: Interconnect

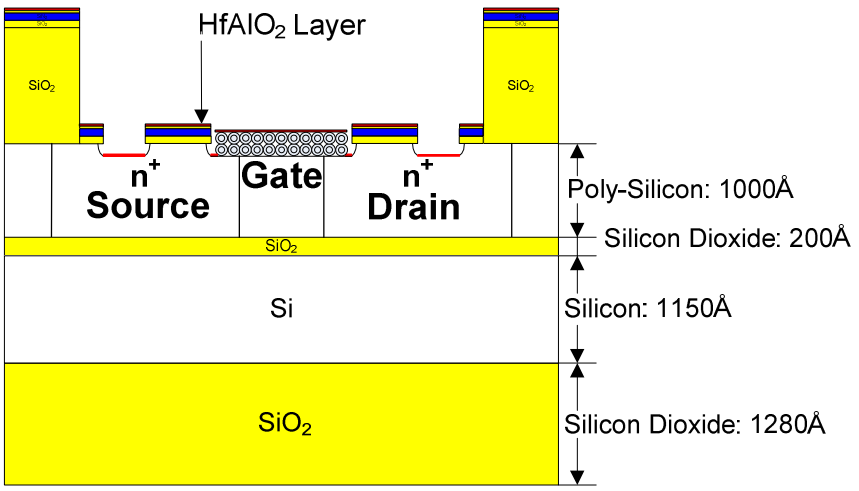


C. QDG-QDC FET using Germanium Quantum Dots

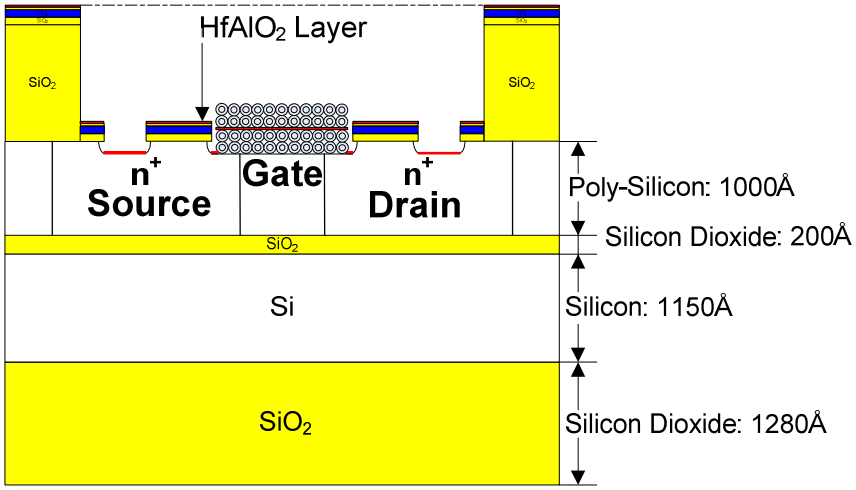
9C. Self-Assembly of Germanium Quantum Dots and Annealing at 350ºC for 10 minutes.



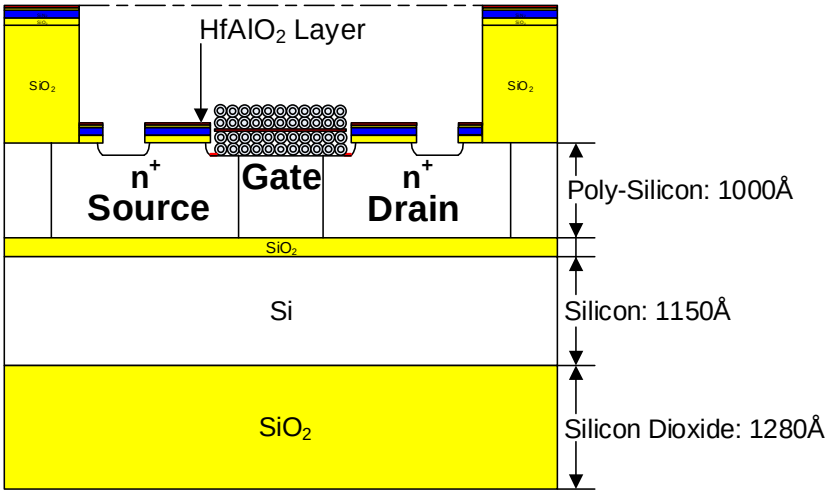
10C. Hafnium Oxide/Aluminum Oxide Combinational Layer Deposition for the Tunnel Oxide



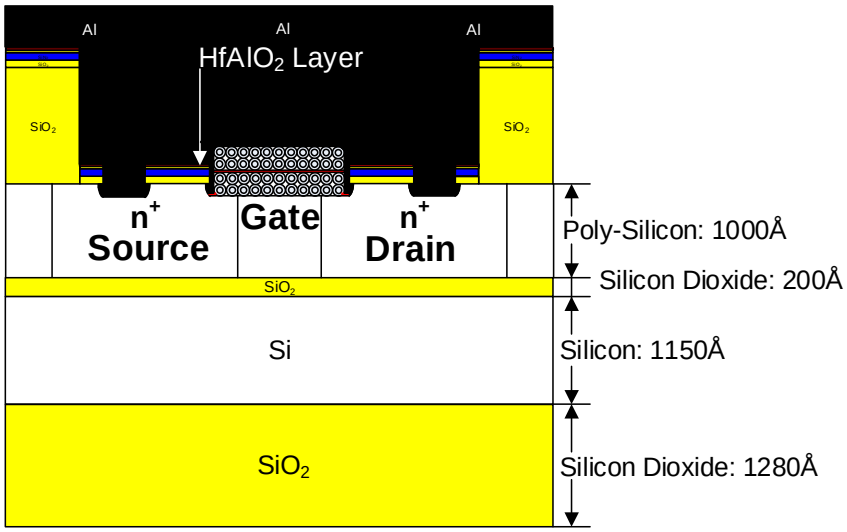
11C. Self-Assembly of Germanium Quantum Dots and Annealing at 350°C for 10 minutes



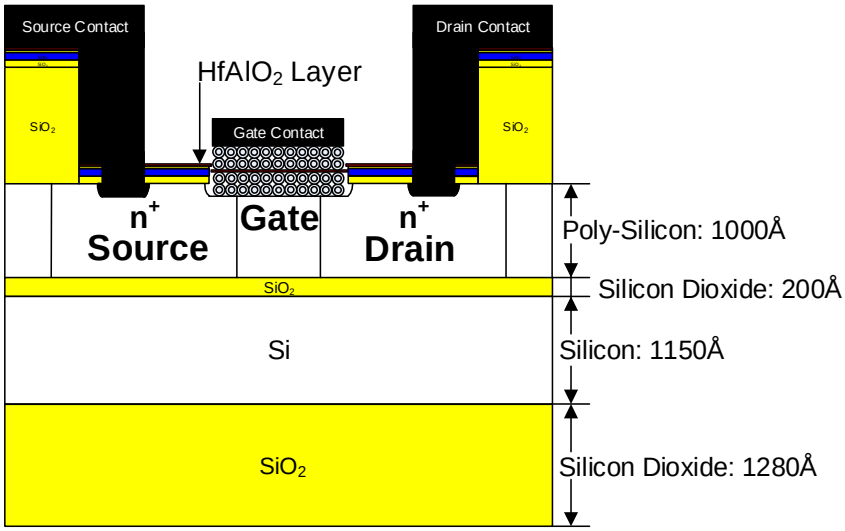
12C. Mask 5: Open Source and Drain Contacts



13C. Metallization



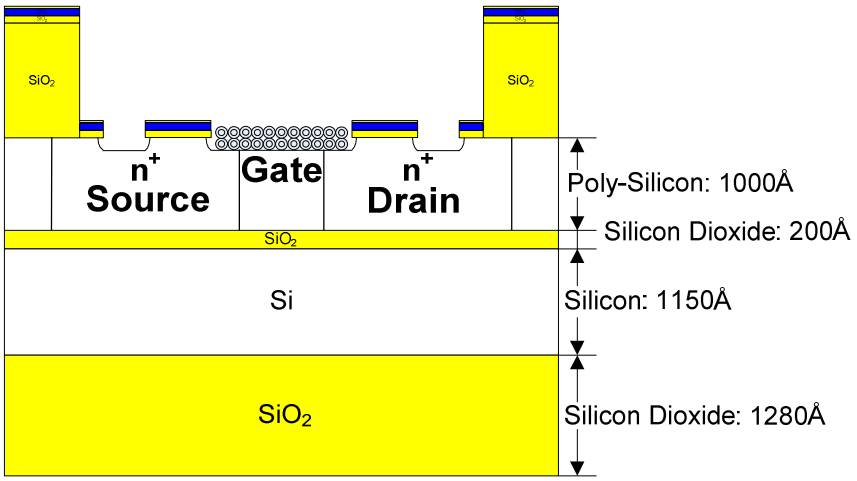
14C. Mask 6: Interconnect



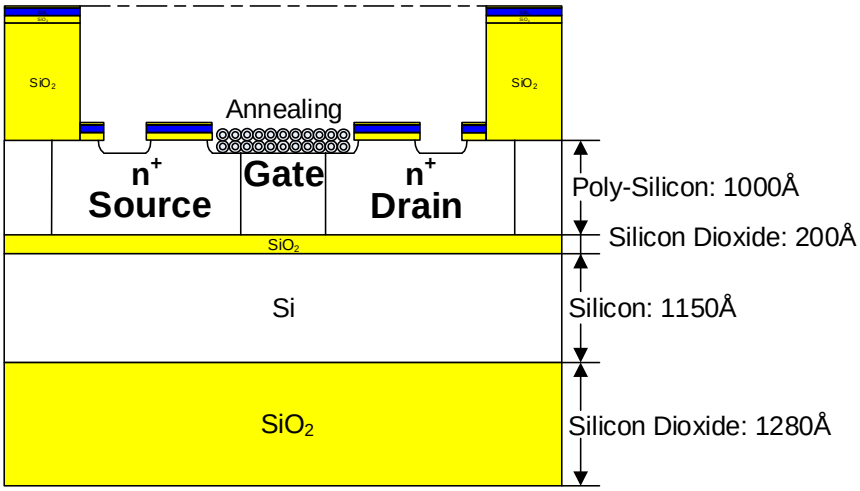
QDG-QDC FET using Germanium Quantum Dots

A. QDG-QDC Nonvolatile Memory using Germanium Quantum Dots

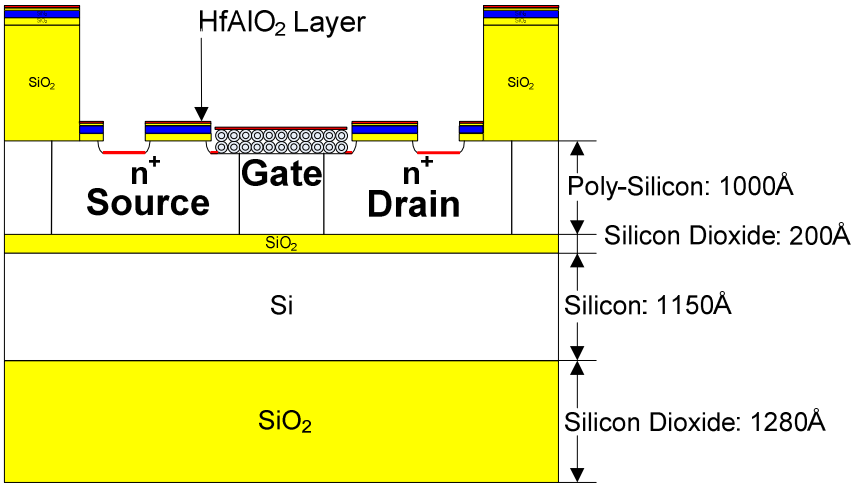
9D. Self-Assembly of Germanium Quantum Dots and Annealing at 350ºC for 10 minutes



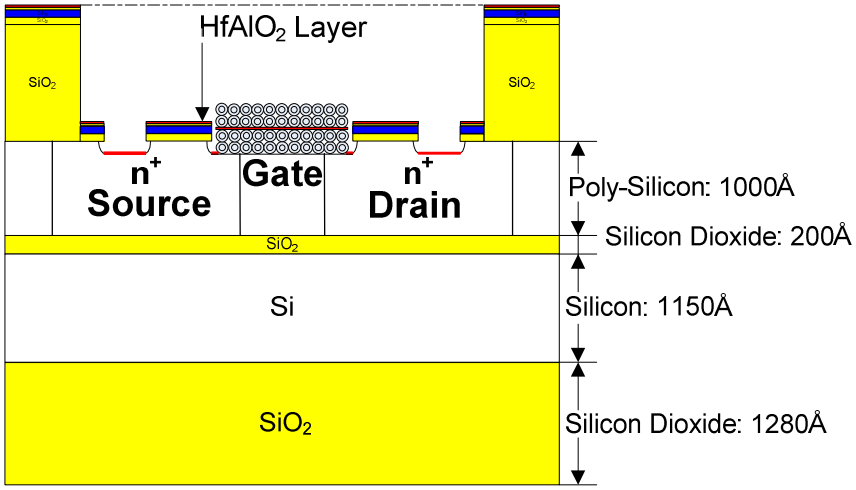
Annealing at 350ºC for 10 minutes



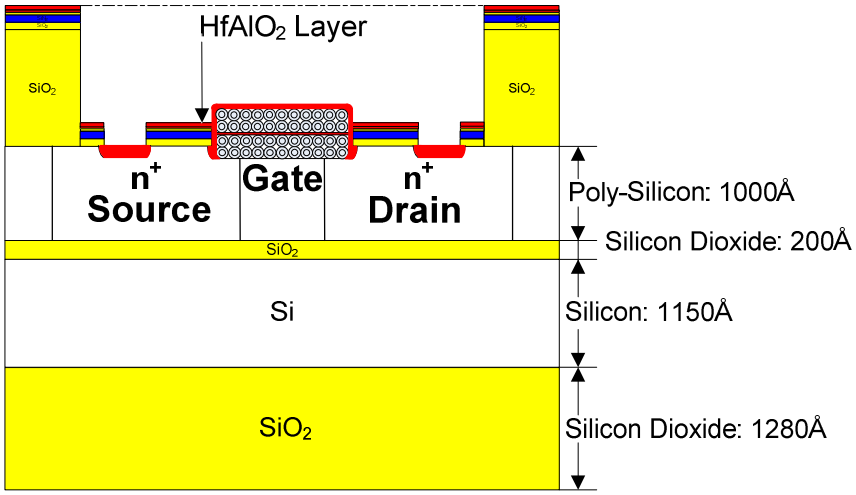
10D. Hafnium Oxide/Aluminum Oxide Combinational Layer Deposition
for the Tunnel Oxide



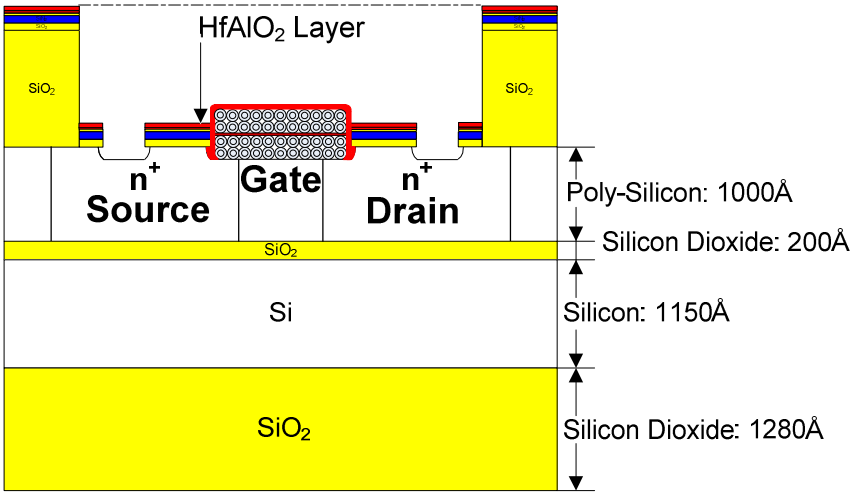
11D. Self-Assembly of Germanium Quantum Dots and Annealing at 350°C for 10 minutes



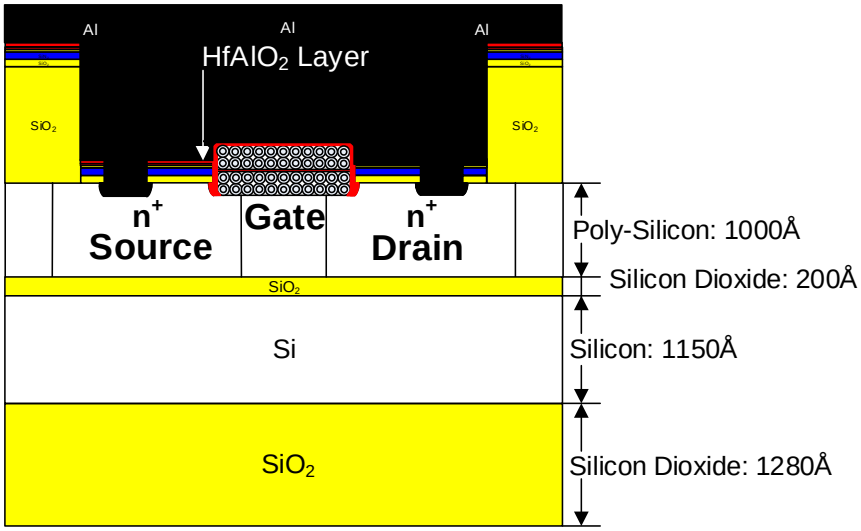
12D. Hafnium Oxide/Aluminum Oxide Combinational Layer Deposition for Control Dielectric



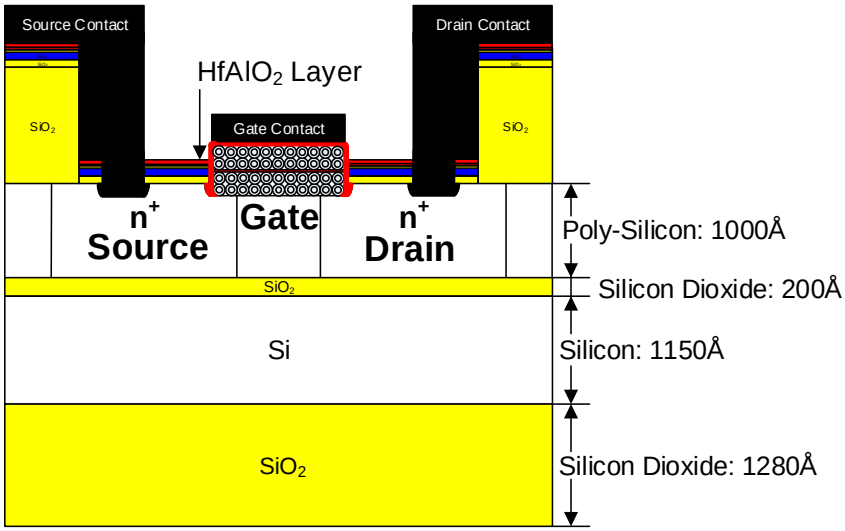
13D. Mask 5: Open Source and Drain Contacts



14.D. Metallization



15D. Mask 6: Interconnect



QDG-QDC Nonvolatile Memory using Germanium Quantum Dots

Appendix 5

Etch Rate

A. BOE Time Estimate for Gate Opening

1. Conventional FET

Material	**Thickness (A)**
SiO_2 (Phosphorus Diffusion)	80A
SiO_2 (Wet Oxidation)	1250A
Total Thickness	1330A
Time Duration Estimate	**133 seconds**

2. QDC FET & QDG-QDC FET using Silicon Quantum Dots

Material	**Thickness (A)**
SiN_4 (Silicon Nitride Deposition)	75Å
SiO_2 (Phosphorus Diffusion)	80Å
SiO_2 (Wet Oxidation)	1250Å
Total Thickness	**1405Å**
Time Duration Estimate	**140.5 seconds**

B. BOE Time Estimate for Contact Holes

1. Conventional FET

Material	**Thickness (A)**
SiO_2 (Dry Oxidation)	250A
Time Duration Estimate	**25 seconds**

2. QDC FET, QDG-QDC FET, and QDG-QDC NVM using Silicon Quantum Dots

Material	**Thickness (A)**
SiO_2 (Si Quantum Dot Oxidation)	70A
Time Duration Estimate	**7 seconds**

3. QDC FET, QDG-QDC FET, and QDG-QDC NVM using Germanium Quantum Dots

Material	**Thickness (A)**
HfO_2 (Hafnium Oxide Deposition)	50A
Time Duration Estimate	**5 seconds**

C. Silicon Wafer Cleaning Procedures

1. Boil wafer in Trichloroethylene (TCE) for 5 minutes.
2. Boil in Acetone for 5 minutes.
3. Boil in Methanol for 5 minutes.
4. Rinse in de-ionized Water.
5. Soak in 5% Hydrofluoric Acid (HF) for 10 minutes.
   HF : Water = 5 : 100, HF : Water = 10 : 200
6. Rinse in de-ionized Water.
7. Soak in freshly made 1 H_2SO_4 : 1 H_2O_2 (always add acid at the end) for 5 minutes.
   Make sure the H_2O_2 has not expired.
   This 1 H_2SO_4 : 1 H_2O_2 solution should be hot when made, and will give off bubbles when the wafers are placed in the solution.
8. Rinse in de-ionized water.
9. Soak in HF for 5 minutes.
10. Rinse in de-ionized Water.
11. Soak in freshly made 1 H_2SO_4 : 1 H_2O_2 for 5 minutes.
12. Rinse in de-ionized water.
13. Soak in HF until the Acid rolls off the Wafer.
14. Rinse in de-ionized Water.
15. Soak in freshly made RCA Solution (6 H_2O: 1 H_2O_2: 1 HCl) at 70°C for 5 minutes.
    H_2O: H_2O_2: HCl=120cc: 20cc: 20cc
    Heat up the Water before adding the H_2O_2 and HCl (always add acid at the end).
    If the RCA solution turns green when you dip your tweezers in it, please discard this RCA solution and remake it.
    Again, there should be bubbles given off when the Wafers are placed in the solution.
16. Rinse in de-ionized water.
17. Soak in HF for 5 minutes.
18. Rinse in de-ionized water.
19. Store in Propanol at 160°.