5-2-2017

Phase Change Devices for Nonvolatile Logic

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Memory access latencies are some of the major limitations on data intensive computation performance nowadays. The possibly achievable CPU clock frequencies must be limited to the maximum access speed of the off-chip memory which constrains the overall system speed, regardless of the power consumption constraints. This computational bottleneck is commonly referred to as the Von-Neumann bottleneck. Memory access latencies can be drastically decreased by integrating the main memory onto the CPU. Phase change memory (PCM) provides the possibility of integration of high-density high-speed non-volatile memory banks on top of the CMOS layer. This computer-on-chip concept has the potential to achieve up to 3-4 orders of magnitude of improvement in computation speed depending on the application. The performance of this computer-on-chip system can be further improved by having the ability to perform logic operations in the memory layer which will also relieve and better utilize the underneath CMOS real estate.

The operation principles and the materials properties of PCM devices allow implementation of functional multi-contact phase-change devices that can be integrated alongside the memory arrays. In this dissertation, a family of multi-contact phase-change devices that are capable of achieving various nonvolatile logic functionalities are proposed. The operation of the proposed devices is demonstrated through unified electro-thermal and materials models that self-consistently solve the current continuity, heat transfer and phase field equations in COMSOL Multiphysics. The access transistors are

modeled using COMSOL nFET SPICE model. The functionality of these devices relies on the novel utilization of the thermal runaway and thermal crosstalk phenomena that PCM devices experience and are often referred to as challenges that need to be overcome. The proposed devices are able to achieve: multiplexing and signal routing, simultaneous NAND & NOR, simultaneous AND & XOR (hence a single device half adder) and JK and T flipflops operation as well as multi-bit state machines. When compared to their conventional CMOS counterparts the proposed devices can offer up to 66% area reduction with the added feature of nonvolatility. The results show the promising potential of the proposed devices for complementing high-performance VLSI as well as reconfigurable-logic.

Phase Change Devices for Nonvolatile Logic

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A Dissertation

Submitted in Partial Fulfillment of the

Requirements for the Degree of

Doctor of Philosophy

at the

University of Connecticut

2017

APPROVAL PAGE

Doctor of Philosophy Dissertation

Phase Change Devices for Nonvolatile Logic

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University of Connecticut
2017

Acknowledgments

Thanks and gratitude are due to Allah.

Secondly, I am grateful and would like to thank my major advisor Prof. Ali Gokirmak for believing in my potentials and providing me with the best support to sail through this path. I would like to thank him even more and Prof. Helena Silva for their mentorship and friendship throughout my Ph.D. career.

I would like, also, to thank my father, Hussien Mohamad Kanan, for being my role model, best friend and inspirer, and my mother, Khitam Mahmod Husien, for being the sweetest heart on this earth and a fountain of passion and care taking. I would like to thank my eldest sister, Hanadi, for being there always for me when I needed, my elder brother, Mohannad, for taking a lot of life burden so early of his life and be the best elder brother could be. I would like to thank my younger sister, Dareen, for being so caring and passionate and my youngest brother, Enad (literally means stubbornness!), for all of the laughs he brings and troubles he causes (I kid). I would like to gratefully thank each one of you my dear family as without of you there will not be any I.

I would like to thank my dear wife, Hebah Allan, for being the best co-pilot in our life journey and to have so much belief in me and provide endless encouragement and motivation; I would also like to thank my little sons Hamza and Ehsan who brought a lot of hope and happiness to our lives

I would also like to thank my other committee members, Prof. Omer Khan, Prof. John Chandy and Prof. Rajeev Bansal for their valuable feedback and suggestions on my thesis work. I would like to thank my former and current lab mates.

Last but not least, I would also like to acknowledge the sources of my funding and support: The National Science Foundation through professor Ali Gokirmak's career grant and the University of Connecticut for the Teaching Assistantship and Research Assistantship.

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1. Introduction

Over the last decades, electronics industry had a tremendous growth and became a main pillar of the overall world's economy. Electronic mobile devices are replacing the conventional ways people used to interact and perceive information, and created unprecedented uses that don't have conventional counterparts: health and fitness trackers, smart watches and virtual assistants to name a few.

The sustained advancement of the semiconductor silicon based technology is the key driver of the performance enhancements and functionality expansion of the electronic devices. This extraordinary growth of the electronic devices types and functionality is imposing urgent needs of higher computational speeds, better data transmission bandwidths and most importantly more memory.

1.1Conventional Computer Architecture

Nowadays, Silicon CMOS is the ultimate winner for the high-speed and/or low power computations and logic race. It is the pillar of the semiconductor industry and the main driver for device scaling. The lithographic process advancement and the integration of new materials (like, SiGe and HfO) [2] with the conventional CMOS had helped in overcoming the key challenge of preserving the low power and high performance which

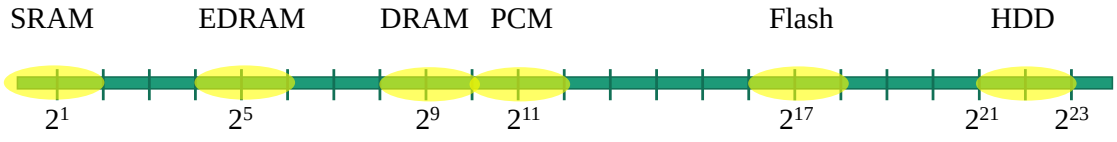


Figure 1-1 Latency of different technologies in memory hierarchy in terms of processor cycles at 4 GHz [1].

was very hard to maintain due to aggressive scaling [3]–[9].

Nowadays, the major limitations on computation performance are memory access latencies and power consumption. Due to memory access latency, for instance, the recently achieved CPU clock frequency of 5.7 GHz must be constraint to the maximum access speed of off-chip memory, that is in the order of 375 ns, which limits the overall system speed to ~2.7 GHz [10]; this computational bottleneck is commonly referred to as Von-Neumann bottleneck[11].

Figure 1-1 shows the access latencies (in cycles) for a 4 GHz processor in computer systems, Static RAM (SRAM) is the fastest memory with the least latency. Although it is volatile (i.e. stored information is lost upon the loss of power), it is very stable and does not require refreshing. An SRAM cell usually consists of six transistors and every cell is used to store one bit. Therefore, this memory is not dense and consumes a large area of the CPU real-estate. There is no nonvolatile replacement, at least nowadays, that can match the switching speeds of the SRAM. The closest rivals' switching speeds are at orders of magnitude slower [12], [13]. The second element in the memory hierarchy is the Dynamic RAM (DRAM), each DRAM cell consists of a single transistor and a capacitor (1T-1C) and only stores one bit. Hence, compared to SRAM it is much denser [14]. The access time of DRAM is in the order of ~10ns. DRAM requires consistent refreshing due to charge leakage and destructive read (i.e. the information is lost upon the cell reading. The embedded version of DRAM (EDRAM) is used as a last level cache (Figure 1-1)[1].

Magnetic storage Hard Drive (HDD) is the densest and the slowest storage element in the memory hierarchy as it provides terabytes (Tb) of memory at very low

cost at the expense of very long access latencies with regarding to a random access operation [1]. NAND flash is the solid-state counterpart of the magnetic HDD with three order of magnitude higher access speeds. It is the highest density memory [15], and is commonly used in high-speed disk systems [16].

Integrating the main memory onto the CPU can drastically improve the computation speed by eliminating the I/O bottleneck to off-chip DRAM. If large amounts of high-speed non-volatile memory could be integrated onto the CPU (Figure 1-2), the need for a hard drive (storage) and a motherboard could also be eliminated. This computer-on-chip concept can deliver > 1000x improvement in computation speed using a fraction of the power compared to the conventional computers.

The ability of performing logic operation and signal multiplexing in the memory layer will drastically improve the overall system performance, and will also allow better utilization of the underneath CMOS layer (Figure 1-2).

Emerging nonvolatile memory technologies such as magnetic random access memory (MRAM) and phase change memory (PCM) can be integrated on the top of conventional 2D CMOS at the back-end-of-the-line using low-temperature processing [17], [18]. Hence, these technologies provide high-density nonvolatile storage with very fast access speeds and high bandwidths, which is a key solution to the Von-Neumann bottleneck.

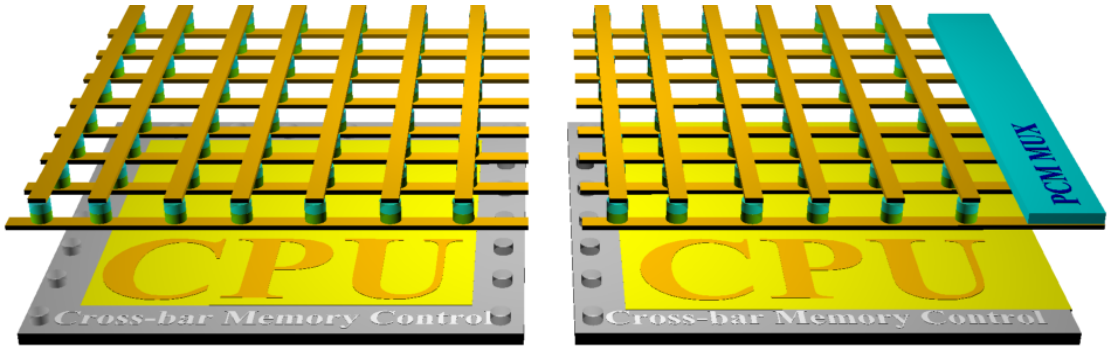


Figure 1-2 Illustration of PCM cross-bar array integrated on the top of the CPU without (left) and with (right) PCM logic devices showing the area relief on the underneath CMOS.

Embedded memory is a term that is used to describe memories that co-exist in the same package with the main processing unit, hence, have no or very low access latencies. The current embedded memories are mainly volatile, and suffer from high power consumption limiting their scalability and accessible bandwidth (MB/s). As is mentioned above, nonvolatile memories can help overcoming the power consumption and provide high bandwidths (x10 GBs). Nowadays the use of nonvolatile embedded memory is limited to the mask programmable or electrically programmable read only memories (ROM) applications. In these applications, the nonvolatile memory is only used to store an execution program.

1.2 Field Programmable Gate Array (FPGA)

Field Programmable Gate Arrays (FPGA) are reprogrammable Silicon-based integrated circuits that allows very high computation speeds and very useful in the prototyping stages of Application-Specific Integrated Circuits (ASICs). FPGAs comprise

programmable computation units that are interconnected with inputs and outputs through a programmable array of switches. Specifically, the connection or the isolation of any subset of the terminals is achieved by controlling electrical switches on the intersections of a matrix of connections. The programmable array provides the flexibility of routing any set of signals to the different computation blocks that can be programmed to implement any logic function.

The FPGA's are comprised of (Figure 1-3):

1 – Logic Blocks: Each logic block consists of a look up truth tables that outputs any function results based on a set of inputs, a D flipflop that holds and synchronizes the output with the FPGA clock and a multiplexer.

2 – Switch Box: Switch boxes control the routing between the various connection blocks and the main inputs and outputs wire segments. Every switch in the switch box is made of a pass transistor and its status is controlled through a memory element.

3 – Connection Blocks: Similar to the switch blocks, connection blocks are composed of pass transistors to control signal routing between logic blocks and main wire segments connecting to switch boxes.

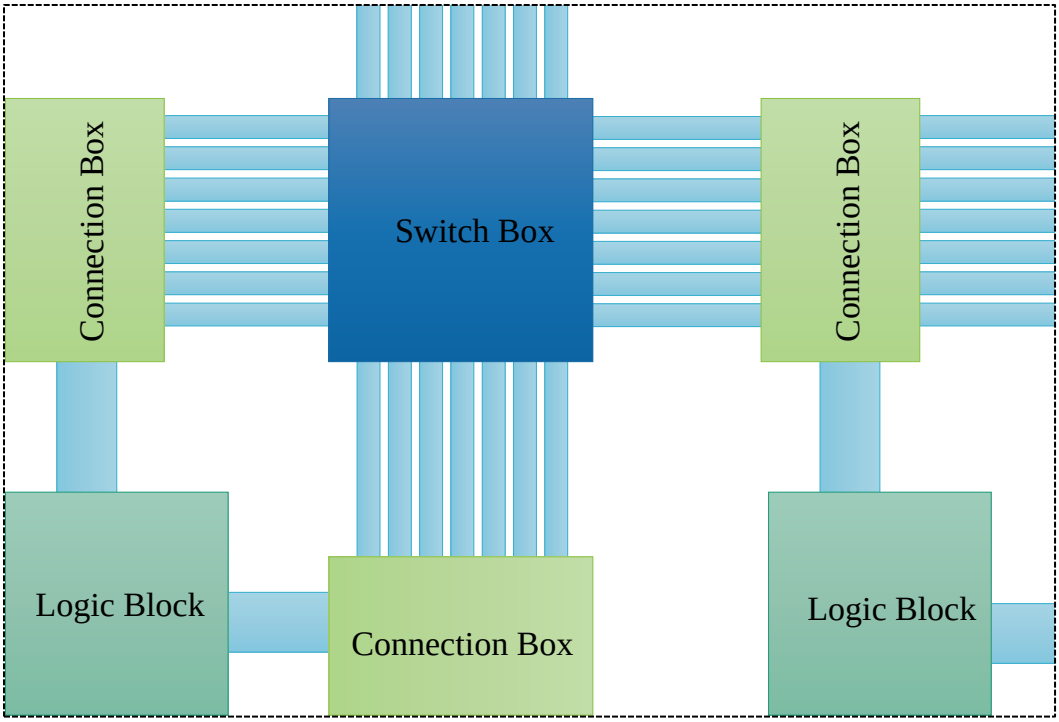


Figure 1-3 Illustration of an island-type FPGA showing the key building blocks.

There are two main types of FPGA based on the memory technology: SRAM based and flash based. SRAM based FPGA are the natural choice for configurable architectures as it provides the highest flexibility. However, other than being a volatile technology this type of FPGA suffers from very high idle power loss (~40% of rated power). Meanwhile, the nonvolatile flash-based FPGA suffers from scalability and fabrication-process compatibility issues.

Emerging nonvolatile memory technologies have very high potential in overcoming the previously mentioned shortcomings, due to the possibility of stacking very dense memory without sacrificing the silicon real estate. Furthermore, due to their nonvolatility, such memory technologies will help reduce the dynamic and idle power losses incurred in the SRAM FPGA counterpart.

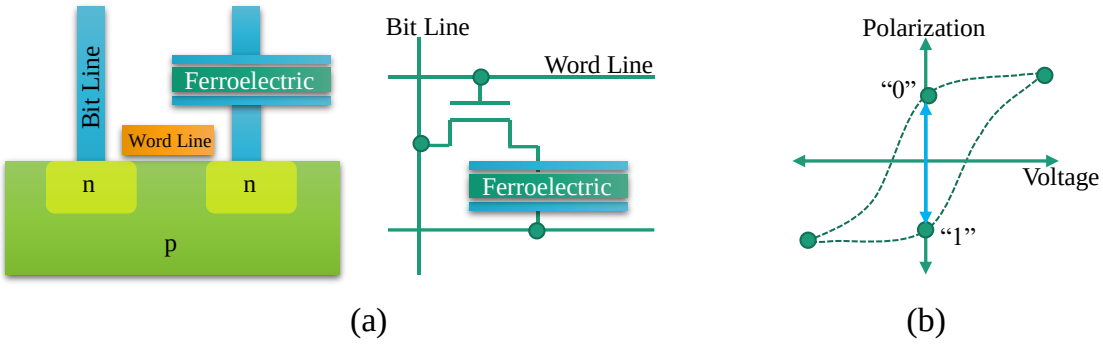
1.3 Outline of Emerging Nonvolatile Random Access Memories

In order to overcome Van Neumann's bottleneck, the nonvolatile main memory has to provide much larger bandwidth compared with the current DRAM. Nowadays, there are three types of emerging nonvolatile memory that have very high potential to solve the memory access latencies that are briefly introduced in this subsection.

1.3.1 Ferroelectric Random Access Memory (FeRAM)

The memory elements of the ferroelectric RAMs are comprised of a ferroelectric material that is sandwiched in-between metal based, Platinum (Pt) or Iridium (Ir) electrodes or metal oxides like IrO2; Lead Zirconate Titanate (PZT) is of the most used ferroelectric material due to its highly stable polarization states, specifically, the ions in the unit cell exhibit two stable configurations in the crystalline lattice. The operation of this memory technology is achieved by switching the polarization of the ferroelectric layer through the application of the electrical field. (Figure 1-4); the polarization remains after the removal of the external electric field, which is the reason for this technology's non-volatility.

FeRAM cell is very similar to the DRAM 1T-1C (One transistor and one capacitor arrangement) and its key advantages are in the very high speed read and write operations around 75ns and endurance of ~10^{12} [19].



(a) (b)

Figure 1-4 Schematic of the FeRAM cell configuration and its respective circuit diagram (a), illustrative V-I curve indicating the two available resistance states.

The FeRAM technology is inhibited from wider use due the following key limitations:

1 – Scalability: The ingoing research is showing that the ferroelectric materials lose their ferroelectric characteristics at smaller device dimensions which inhibits the higher density of these devices in commercialized products. The smallest report FeRAM devices are fabricated at 130nm technology [19].

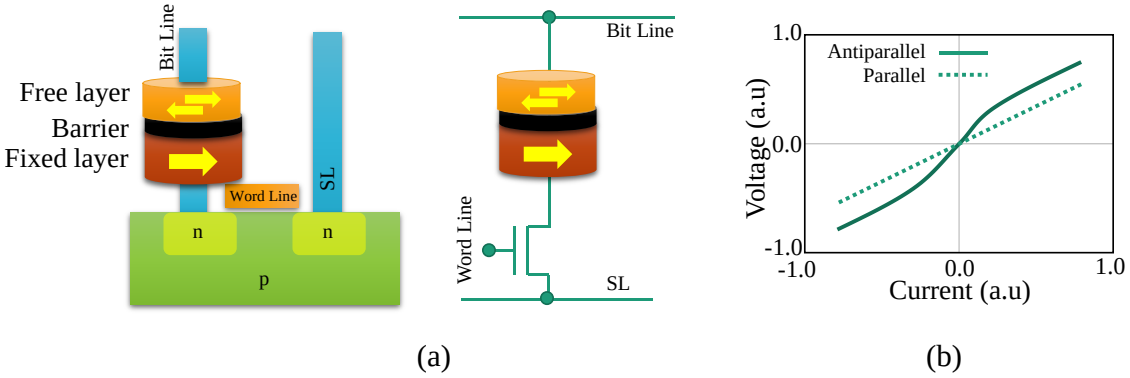
2 – Destructive Read: Although the FeRAM is nonvolatile but it suffers from the destructive read, the device state need to be flipped in order to read it. This leads to a higher energy requirement compared with the other emerging nonvolatile memory technologies (like MRAM).

3 – High Thermal Budget: the PZT materials have very high crystallization temperatures (~700C) which represent a challenge in the fabrication process.

1.3.2 Magnetic Random Access Memory (MRAM)

In Magnetic RAM (MRAM) the information is stored in the magnetization of a magnetic element; the MRAM cell in its simplest form comprises two ferromagnetic layers (like CoFeB) that are separated by a thin tunneling dielectric (like MgO) layer forming a Magnetic Tunneling Junction (MTJ). The magnetic orientation of each of the ferromagnetic layers has a direct impact the resistance of the junction; if the ferromagnetic layers have parallel orientation the MTJ will have a considerably lower resistance compared to when they have an anti-parallel orientation.

Spin Torque Transfer (STT)-RAM cell is the most promising MRAM type. The MTJ of these cells has one of the ferromagnetic layers made significantly thicker (fixed layer) than the other (free layer). The fixed layer will polarize the current passing through it, and the spin torque of this polarized current can then alter the direction of the magnetic orientation of the free layer to be parallel (conductive) or anti-parallel (resistive) to the fixed layer [20]. The schematic of the STT-MRAM cells is depicted in Figure 1-5 with the device V-I curve.



(a) (b)

Figure 1-5 Schematic of the STT-MRAM cell configuration and its respective circuit diagram (a), illustrative V-I curve indicating the two available resistance states.

The very high current requirements to change the polarization of the free layer requires is of the main challenges that inhibit the wide use of this technology as well as the high cell to cell variability due to the active layer roughness [21].

1.3.3 Electro-Thermal Resistive Random Access Memories (RRAM)

The key principle of this type of RRAM operation can be seen in the reversible transition of small volume of material that is sandwiched between two contacts by the means of applied electric field and utilizing the electro-thermal effects. The resistance contrast can be achieved in three different ways depending on the type of the contacts and the material of the switching layer (Figure 1-6)

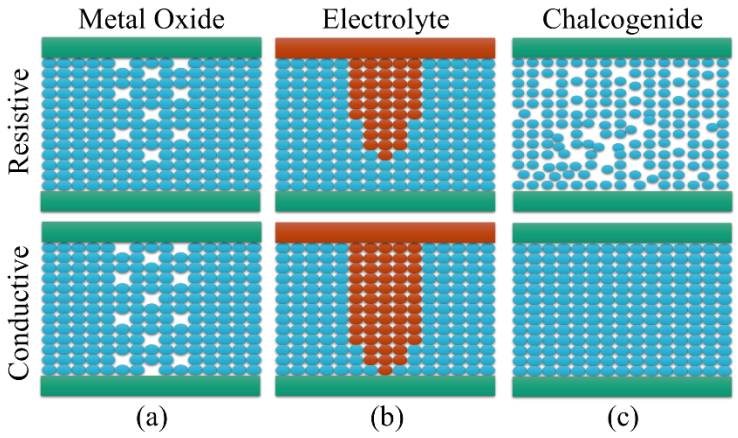


Figure 1-6 The formation of a conductive filament of oxygen vacancies in a metal oxide (a), the annihilation and creation of a metallic Ag protrusion in a solid electrolyte (b) and Phase change between an amorphous and a crystalline chalcogenide (based on [22]).

In Metal Oxide RRAM, relatively high voltage is applied across the dielectric metal oxide layer leading to the forming of a conductive filament of vacancies or metal defects migration across the metal contacts. Upon the initialization of this filament the conductive path can be broken by reversing the polarity of the applied electric field, hence, resetting the cell to the high resistance state (Reset state). The cell can be brought to the low resistance state by applying electrical filed in the same direction as the initialization phase. These types of cells operate at speeds in the order of ~10ns and for an endurance of 10^{10} [23].

Alternatively, conductive filament can form through the electrochemical metallization process without the need of the high electric field to aggregate vacancies or defects. Similar to the electro-plating process the ions of one of the electrodes (Typically Ag or Cu) dissolve freely in the electrolyte layer (like CuS, GeS_2 …etc.) (Figure 1-6b) The application of the electric field will then align the ions and form the conductive filament [24].

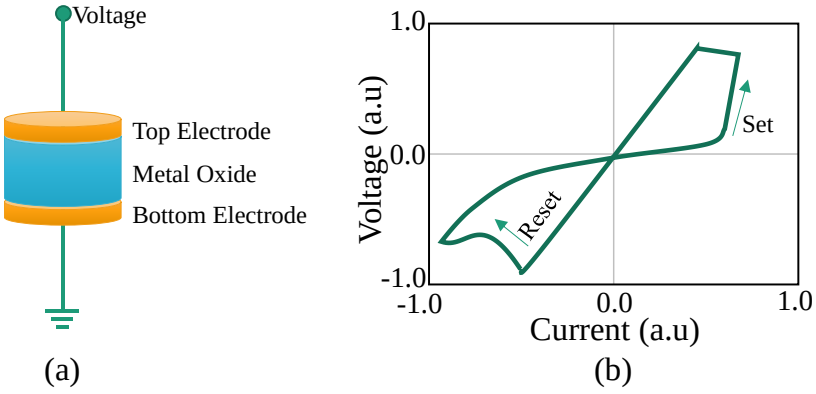


Figure 1-7 Schematic of metal oxide RRAM (a) and an illustrative I-V curve showing the Set and Reset states.

The third possible way to achieve resistance contrast is through changing the phase of the material as in Phase Change Memory (PCM) which is the focus of this dissertation. PCM has entered the electronics market as a random access nonvolatile memory technology and is attracting a significant interest due to its fast read/write times, endurance, long-term data retention and single-bit alterability [25], [26]. The operation of PCM is based on the reversible phase transition of a chalcogenide material between the resistive amorphous and conductive crystalline states through joule heating. The crystalline to amorphous transition (reset operation) takes place as a result of the rapid cooling of the molten chalcogenide material in a manner where atoms do not have sufficient time to rearrange in the crystalline structure. The amorphous to crystalline transition is obtained by heating the chalcogenide material beyond the crystallization temperature and allowing sufficient time for the atoms' rearrangement (Figure 1-8).

Depending on the cell geometry and the chalcogenide material used, a resistance contrast of multiple orders of magnitude can be realized between the different phases; such contrast is the key for reliable data storage.

Mushroom cells are the common PCM cell geometries due to high packing density and relatively easy process integration [27], and $Ge_2Sb_2Te_5$ (GST) is the most studied PCM material due to its stability and high resistivity contrast between the crystalline and amorphous phases[28].

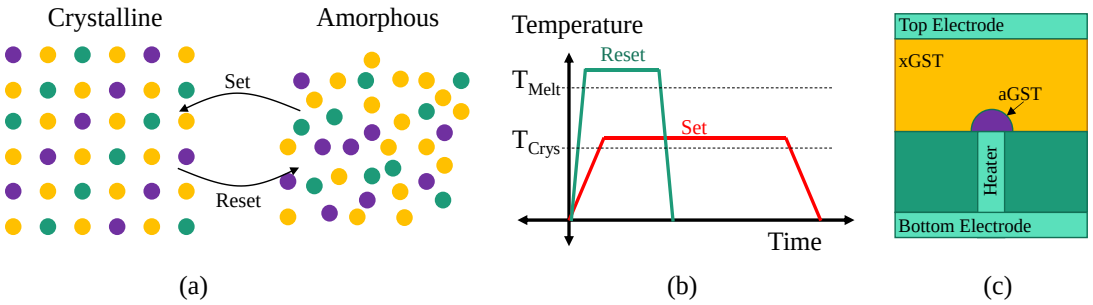


Figure 1-8 Illustration of the molecular structure changes between amorphous and crystalline GST, the drawn arrows indicate the programming operation direction. Please refer to Ref. [29] for the exact molecular structure (a). Set and Reset programming operations temperature–time characteristics (b). Schematic of a PCM Mushroom cell (c).

Each individual PCM cell forming the memory array is addressed via an access device: typically, a field effect transistor (FET), bipolar junction transistor or a diode [30]. The reset current requirements determine the power consumption and the dimensions of the access device, such as the width of the FET. Access device size typically determines the packing density.

The phase change memory as a technology offers great flexibility in fabricating various device structures and allows different ways of operation, with the emergence of this technology that has sparked the interest in using phase-change elements in nonconventional device that provide functionalities beyond the basic memory operation; such as, PCM switches as well as in the artificial neural networks [31], [32]. In this dissertation, a family of multi-contact phase-change devices that are capable of achieving various nonvolatile logic functionalities are proposed. The operation of these devices

relies thermal runaway and thermal crosstalk phenomena that PCM devices experience and are often referred to as challenges that need to be overcome.

2. Phase Change Memory Operation and Modeling

2.1 Introduction

In the previous chapter we introduced the phase change memory and highlighted its key characteristics, we have also indicated that one of the main challenges that face this technology is the high reset current requirements. In this chapter we will shed more light about the basic PCM cell operation and the impact of the current requirements on the access device size, hence, the scalability of this technology. In the relevant literature, different approaches to minimize reset current have been investigated [33]–[36], among these; the rupture oxide approach was demonstrated to reduce the current requirements by orders of magnitude with minimal changes to the device geometry.

Rupture oxide cells are fabricated to have a thin interfacial oxide layer between the heater and the phase-change material. The oxide is ruptured by electrical breakdown, forming conducting nanofilaments. The size of the nanofilaments is directly controlled through the shape/magnitude of the breakdown pulses, and determines the current confinement and the cell behavior [37].

2.1.1 Electro-thermal Assessment of Rupture Oxide PCM

The operation of the phase change memory cells and is illustrated through 2D rotationally symmetric, finite element simulations that are performed using COMSOL Multiphysics [38]. The conducted study analyzes the reset current requirements and resulting resistance contrasts of rupture oxide PCM cells with an nFET access device (**Figure 2-1**a). Rupture oxide cells with varying nanofilament diameters are modeled to

capture the possible outcomes of the rupturing process. The performance of these cells is assessed for various operating conditions, access device specifications, as well as filament materials.

2.1.2 Device Modeling

The schematic of the modeled rupture-oxide PCM cell is shown in Figure 2-1a. The rupture oxide is modeled as a 3 nm thick SiO_2 with a cylindrical nanofilament placed at the center of the oxide layer. Material parameters of the filament are assumed to be similar to the TiN material parameters. The SiO_2 layer is placed at the interface between the GST disk and the TiN heater. The models used in the finite element simulations include temperature dependent material parameters, thermal boundary resistance (TBR), and thermoelectric effects. Thermoelectric effects are shown to have strong influence on the PCM performance [39], [40] but have not been included in similar finite element studies [41].

The reset operation is simulated by solving the current continuity (1) and heat transfer (2) models self-consistently using COMSOL Multiphysics:

$$\nabla \cdot J = -\nabla \cdot \underbrace{\sigma(T)\nabla V}_{Ohm's\ Law} - \nabla \cdot \underbrace{\sigma(T) \cdot S\nabla T}_{Seebeck\ current} = 0 \qquad (1)$$

$$\underbrace{d_G C_P(T)\frac{dT}{dt}}_{Heating} - \underbrace{\nabla(\kappa(T)\nabla T)}_{\text{Heat diffusion}} = \underbrace{\frac{J^2}{\sigma(T)}}_{\substack{Joule \\ heating}} - \underbrace{J\ T\ \nabla S}_{Thomson\ h.} \qquad (2)$$

where J is the current density, V is the electric potential, σ is the conductivity, T is the temperature, S is the Seebeck coefficient, d is the mass density, CP is the heat capacity and κ is the thermal conductivity. This model accounts for the thermoelectric

effects through the introduction of the Seebeck current term in (1) and the Thomson heat term in (2) [42].

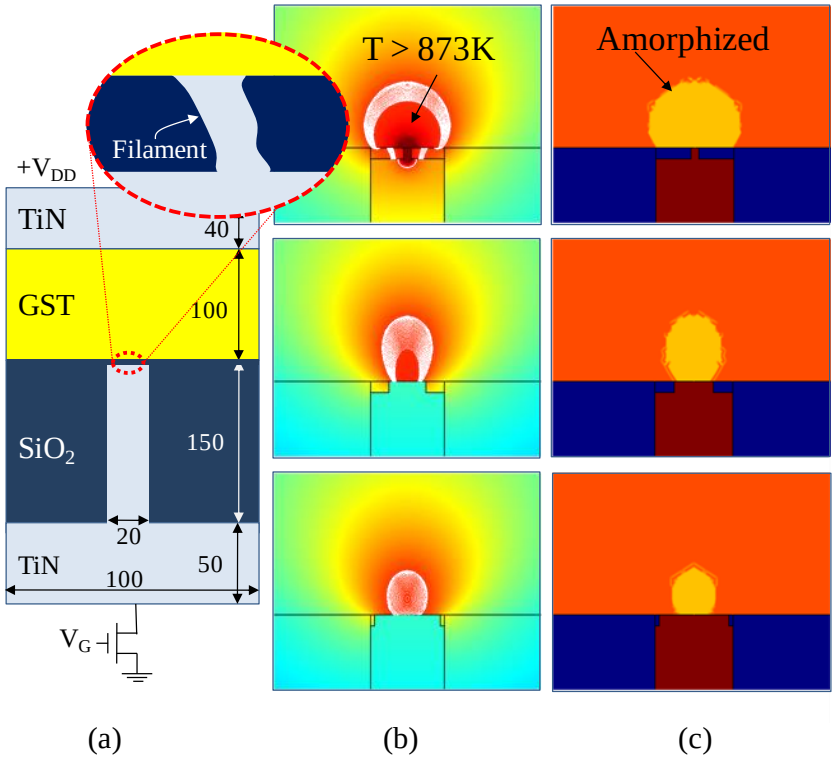


Figure 2-1 (a) Schematics of a rupture oxide cell design with indicated dimensions in nm and magnified active region. (b) Peak thermal profile of a rupture oxide mushroom cell with filament diameters 2, 10 and 18 nm respectively for an applied voltage of (V_{DD} = V_G = 1.5 V). The white contour lines denote the boundaries of melting in the active region. (c) The resulting conductivity profile after the reset operation showing the amorphized regions in yellow.

The temperature dependent material parameters used in the simulations are shown in Figure 2-2. The electrical resistivities of crystalline (FCC) and amorphous GST were reported in previous works, however, these resistivities are obtained by means of slow measurements which would allow the GST to change its phase during the slow heating

process (~1 K/min.). In reset pulses, which require only nanoseconds, GST is unable to undergo intermediate phase transitions before it reaches the molten state. Hence, the exponential behavior for the FCC and amorphous GST resistivities near room-temperature are extrapolated to the melting temperature (883 K) in order to model the meta-stable states. A measured value of 2.1 μΩ·m [42] was used for the liquid state.

The thermal conductivity of GST was estimated based on the phonon (κ_{ph}) and the electronic (κ_{el}) contributions. Phonon conduction is assumed to dominate at low temperatures and decay as the temperature increases; the number of broken bonds increases exponentially with temperature. Likewise, the electrical conductivity and the electronic thermal conductivity are assumed to increase with temperature due to generation of free charge carriers with breaking of each bond. In this study, we neglect heat transfer due to convection in liquid state. Hence, electronic thermal conductivity contribution is assumed to govern heat transfer as the GST becomes highly conductive upon melting. κ_{ph} in the solid state is modeled to be decreasing linearly and vanishing at onset of melting (3); κ_{el} is calculated using Wiedemann-Franz (W-F) Law (4):

$$\kappa_{ph}(T) = \kappa_{ph}(300\ K)\left(1 - \frac{\sigma(T)}{\sigma(873\ K)}\right) \quad (3)$$

$$\kappa_{el}(T) = \underbrace{(2.44 \cdot 10^{-8}\ \mathrm{W \cdot \Omega \cdot K^{-2}})}_{Lorenz\ number}\,\sigma(T)T \quad (4)$$

The total thermal conductivity shown in Fig. 2c is the sum of the modeled phonon and electronic contributions. The latent heat of fusion for GST (L_f =126x103 J/kg [43]) is accounted for using a 10 K wide spike in heat capacity starting at 873 K (Figure 2-2d) [44].

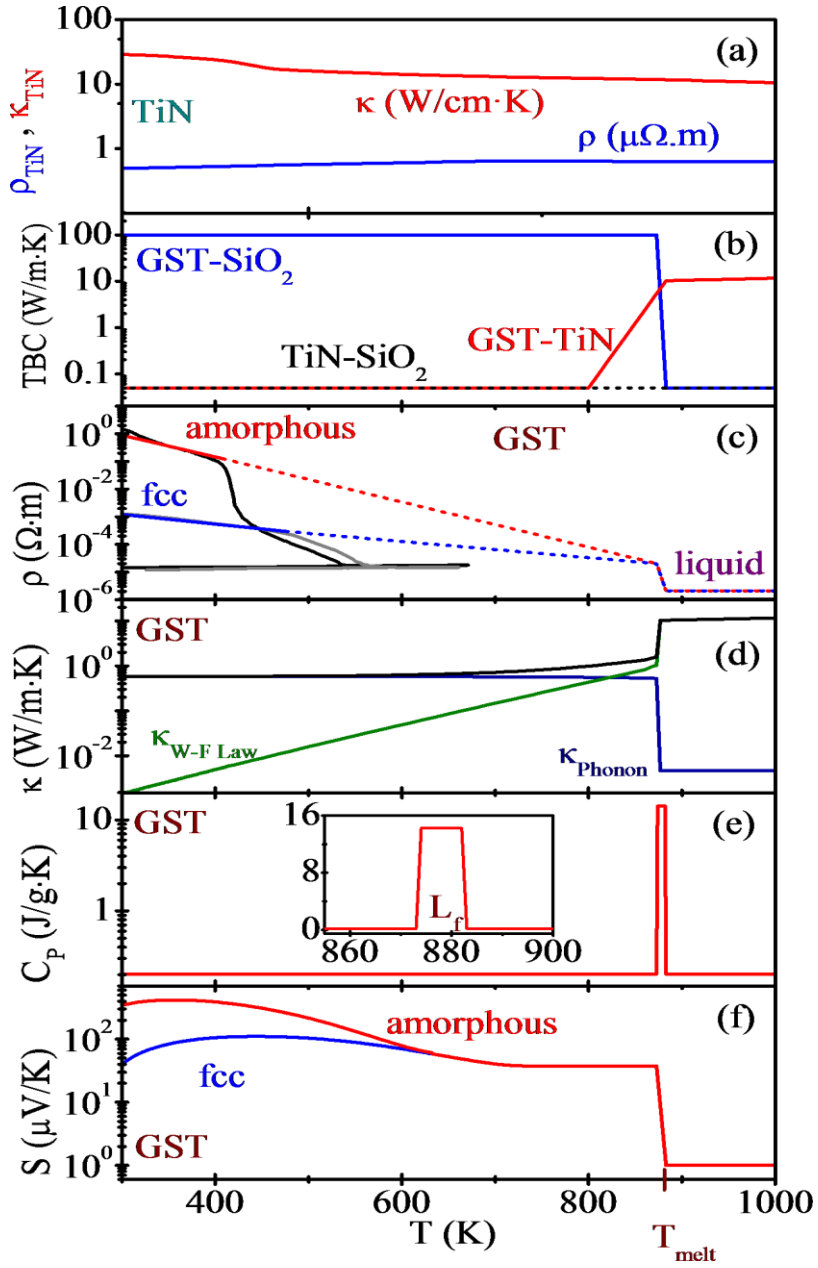


Figure 2-2 Temperature dependent electrical and thermal conductivities of TiN (a), thermal boundary conductivities between GST-SiO_2, GST-TiN and TiN-SiO_2 (b), electrical resistivities of amorphous and fcc GST (c), thermal conductivity of GST (calculated electronic and estimated phonon contributions) (d), Heat capacity of GST around the melting temperature (e), inset showing the peak to incorporate the latent heat of fusion, and Seebeck coefficient of amorphous and fcc GST (f) [45].

Thermal transport at the metallic TiN and nonmetallic GST interface is modeled using κ_{el} of GST calculated using W-F law, assuming weak electron-phonon coupling (negligible κ_{ph}) at the interface; to account for the thermal boundary resistance (TBR). A 1 nm virtual layer with temperature dependent thermal boundary conductivity (TBC) is used to include TBR at these interfaces. An experimental room-temperature $TBR_{GST\text{-}TiN}$ of ~20 m^2K/GW is reported [46]. As free electron concentration increases with temperature, the $TBR_{GST\text{-}TiN}$ is expected to decrease as the heat transfer due to the electron-electron coupling become more significant. In the proposed model, the room-temperature value of $TBC_{GST\text{-}TiN}$ is assumed to be constant for T < 800 K, after which the $TBC_{GST\text{-}TiN}$ is increased linearly until κ_{GST} is matched at 873 K (T_{melt}) (Figure 2-2e). Heat transfer through the SiO_2 and GST interface is assumed to be dominated by an efficient phonon-phonon coupling process at room temperature which is modeled by using a high $TBC_{SiO2\text{-}GST}$ value. Heat transfer through the liquid-GST - SiO_2 interface is assumed to be weak due to significantly reduced phonon coupling in the liquids and it is modeled by using the $TBC_{GST\text{-}TiN}$ value (Figure 2-2e). The operation temperature of PCM cells in these simulations remain significantly under melting temperature of TiN and SiO_2; a constant $TBC_{TiN\text{-}SiO2}$ of 100 W/m·K is assumed

Temperature dependent Seebeck coefficients for crystalline (FCC) and amorphous GST shown in Figure 2-2e are polynomial fits to experimental results in [47]. The Seebeck coefficients are assumed to remain constant (38 μV/K) in the 735 K – 873 K range and decrease linearly to a metallic Seebeck value of 1 μV/K upon melting (873 K - 883 K).

GST is modeled to be amorphized at any particular mesh-point that experiences T ≥ 873 K (onset of melting) at any time-step; assuming that the entropy introduced in the material is sufficient to result in amorphization even though the material did not go through a solid-liquid phase transition (phase transition is modeled to be complete by T = 883 K after absorbing L_f).

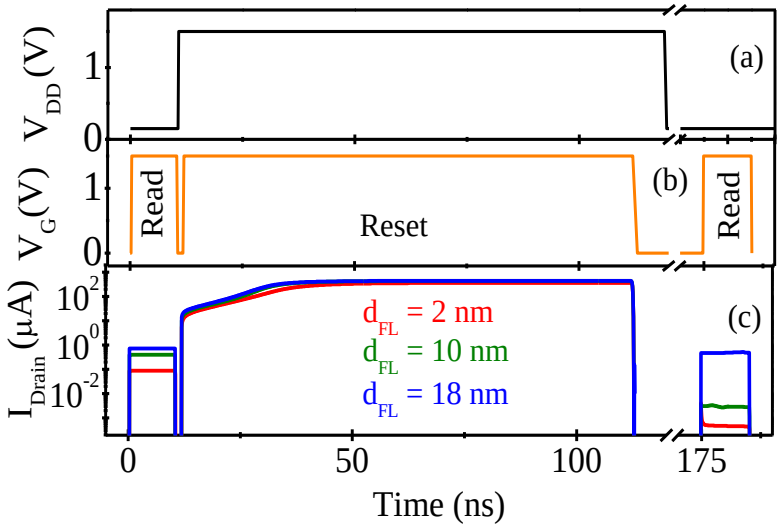


Figure 2-3 (a) Supply voltage, (b) and gate voltage waveforms during the read/reset/read operation. (c) Transistor drain current during the read/reset/read for different filament sizes.

Table 1 Testing Scenarios

Testing Scenario	V_{DD} (V)	V_G (V)	W_{FET} (nm)
Supply Voltage	1→2.3	1.5	85
Gate Voltage	1.5	1→2	85
FET Width	1.5	1.5	25→150

The phase of every mesh point is tracked to enable Read/Reset/Read operation sequence in a single simulation study (**Figure 2-3**). The cells are allowed to cool down to room temperature between the reset and the second read operations. The ratio of the drain current during the first and the second read pulses are used to characterize the resistance contrast. The amorphized volume is visualized by mapping the conductivity in logarithmic scale (Figure 2-1c).

The access transistor is integrated with the finite element simulations by implementing the basic nFET circuit model available in COMSOL with 22 nm channel length (L_{FET}) and width (W_{FET}) varying from 25 nm to 150 nm [30]. The terminals of the nFET are configured as seen in (Figure 2-1a. The transistor is turned on during reset and read operations by applying a constant gate voltage (V_G) for 100 ns duration. The supply voltage (V_{DD}, refer to (Figure 2-1) is maintained high and is lowered to 0.2 V to perform read operations. V_{DD} and V_G voltages during the Read/Reset/Read train of pulses are shown in Figure 2-3a-b.

2.1.3 Filament Diameter, Applied Voltages and Transistor Width Effects

The diameter of the conductive nanofilaments (d_{FL}) embedded in the rupture oxide is varied from 2 nm to 18 nm with increments of 2 nm to assess the impact of the filament size on the PCM cell performance. The Read/Reset/Read pulses are applied to each of these cells with $V_{DD} = V_G = 1.5$ V (Figure 2-3). In this set of simulations, the access transistors operate in saturation regime, hence the reset currents are similar for all cases even though the resulting R_{RESET}/R_{SET} contrast differ significantly (Figure 2-3c).

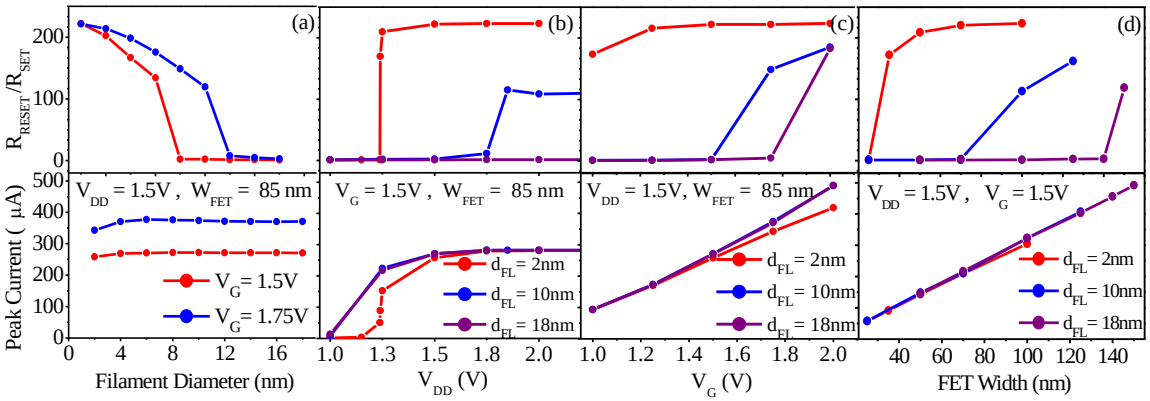


Figure 2-4 The obtained resistance ratio after the reset operation and the peak reset current as a function of: (a) filament diameters, (b) supply voltage (V_{DD}), (c) gate voltage (V_G) and (d) FET width (W_{FET}).

Figure 2-4a shows the R_{RESET}/R_{SET} contrast and peak reset current for the whole simulated d_{FL} range. The cells with small filament diameters (≤ 9 nm) experience sufficient heating to amorphize a volume that completely covers the nanofilament/GST interface, yielding a significant R_{RESET}/R_{SET} contrast. The amorphized volume, and hence the R_{RESET}/R_{SET} contrast, decreases with increasing filament diameter (Figure 2-4a). PCM cells with small (2 nm), medium (10 nm), and large (18 nm) filament sizes are simulated to determine the effect of the supply voltage (Figure 2-4b), the gate voltage (Figure 2-4c) and the transistor width (Figure 2-4d) where only one of these parameters is varied (Table 1). Successful reset operation can be realized for cells with smaller filaments at significantly lower V_{DD}, V_G and W_{FET} while the peak currents are similar for all cases. Narrower filaments give rise to more localized joule heating due to larger filament resistance and current confinement and produce a strong resistance contrast. The R_{Final}-I_{Peak} curves for these cells are shown in **Figure 2-5**.

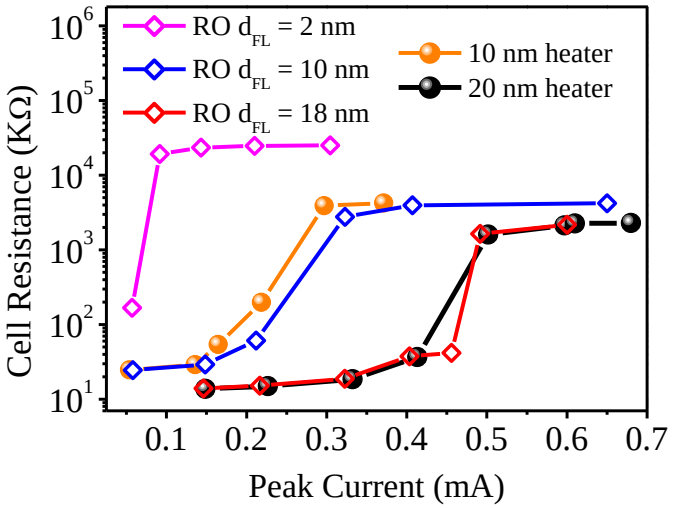


Figure 2-5 The final cell resistance versus peak reset current for rupture oxide cells with 2, 10 and 18 nm filament diameter as well as for two conventional cells with 10 and 20 nm heater diameters.

2.1.4 Comparison with Conventional PCM Cells

Reset current requirements of PCM cells scale with the heater diameter, which is typically limited by fabrication processes in conventional cells. The advantages of rupture oxide cells in reducing the reset currents are illustrated by comparing them to the conventional mushroom cells with similar dimensions, using the same mathematical models: A rupture oxide cell with 20 nm heater diameter and 10 nm filament is compared to conventional cells with 20 nm and 10 nm heater diameters (Figure 2-6). Each of these cells was biased with a V_{DD} of 2 V. The gate voltages were varied to determine the minimum reset current required to amorphize the region covering the heater at each of these cases (**Figure 2-7**). The mushroom cell with the 10 nm heater and the rupture oxide cell with 10 nm filament consume approximately the same power. (**Figure 2-7**c). The R_{Final}-I_{Peak} characteristics for the three different cells are shown in **Figure 2-7**. The RO

cell behaves very similar to the conventional cell with the 10 nm heater and is much better than the conventional cell with the same heater diameter.

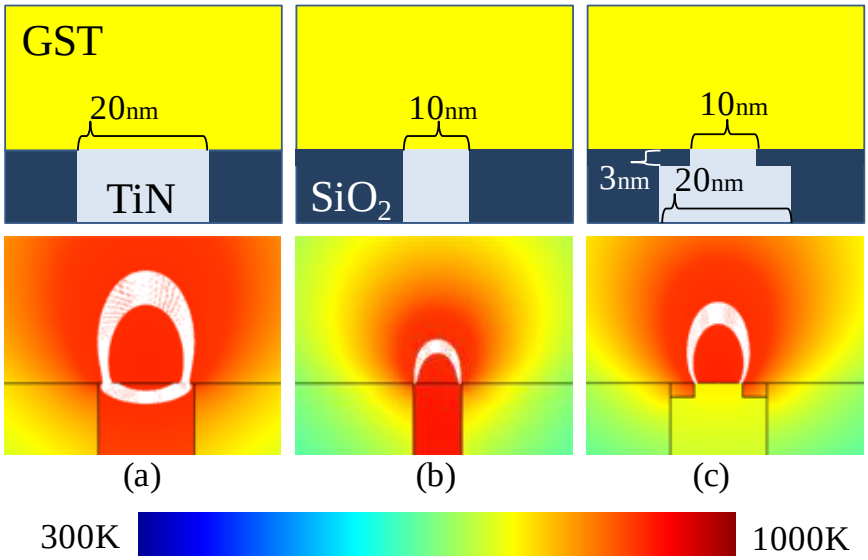


Figure 2-6. Conventional mushroom geometry and peak thermal profile for heater diameters of (a) 20 nm (V_G = 1.9 V) and (b) 10 nm (V_G = 1.4 V). (c) Rupture oxide cell geometry and peak thermal profile for a 20 nm diameter heater (V_G = 1.4 V). White contour lines in thermal profiles indicate regions of GST melting.

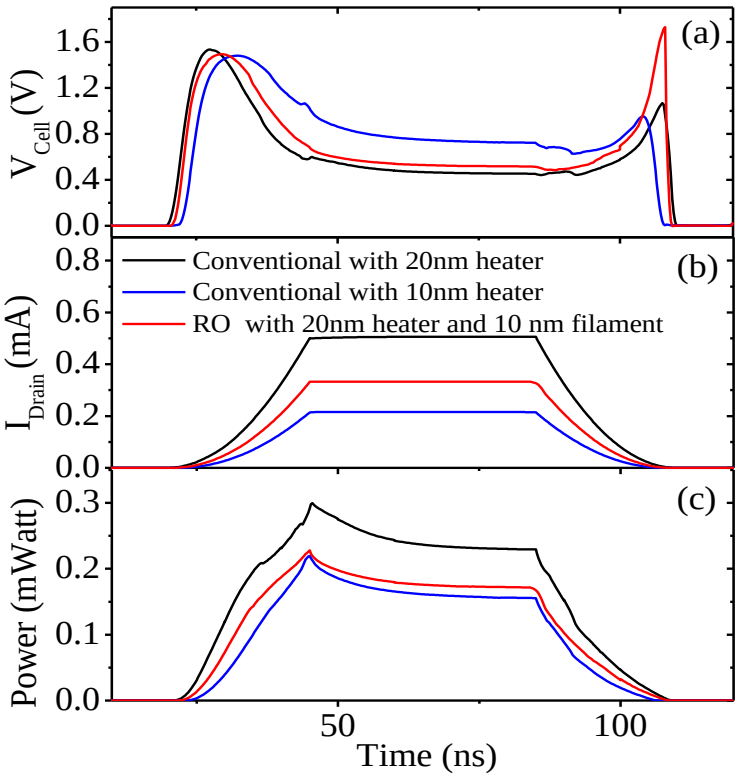


Figure 2-7 (a) Voltage drop across the cell, (b) drain current, and (c) instantaneous power during the reset pulses.

2.1.5 The Effect of Filament Resistivity

The resistivity of the filament is expected to alter the reset dynamics. Metal oxides such as TiO_2, HfO_2 are expected to form highly-conductive metallic filaments compared to SiO_2 in which the nanofilaments are reported to be highly resistive and behave more like Si [48]. Material parameters of Si with [P] = 10^{19} cm^{-3} doping is used (instead of TiN) for a 2 nm filament case to demonstrate the impact of filament resistivity. The material properties for Si are obtained from the literature [49] and calculated using Sentaurus Synopsis modeling tool [50], and $TBC_{Si\text{-}TiN}$ = $TBC_{GST\text{-}TiN}$ and $TBC_{Si\text{-}GST}$ = 0 are assumed. The transistor parameters (W_{FET} = 85 nm, L_{FET} = 22 nm) and

V_G = 1.5 V is kept constant for the simulations. The cell with the Si filament has a larger R_{SET} and requires slightly higher V_{DD} for reset. However, the reset current is smaller by an order of magnitude and the resulting amorphized volume is significantly smaller for a similar resistance contrast using the same V_{DD} (Figure 2-8). The increase in the amorphized volume beyond what is necessary to cover the filament interface leads to a slight linear increase in the cell resistance but requires a significantly larger V_{DD} for set operation: The breakdown voltage of the amorphized volume for the Si filament case in Figure 2-8b is only 224 mV while it is 952 mV for the TiN filament case.

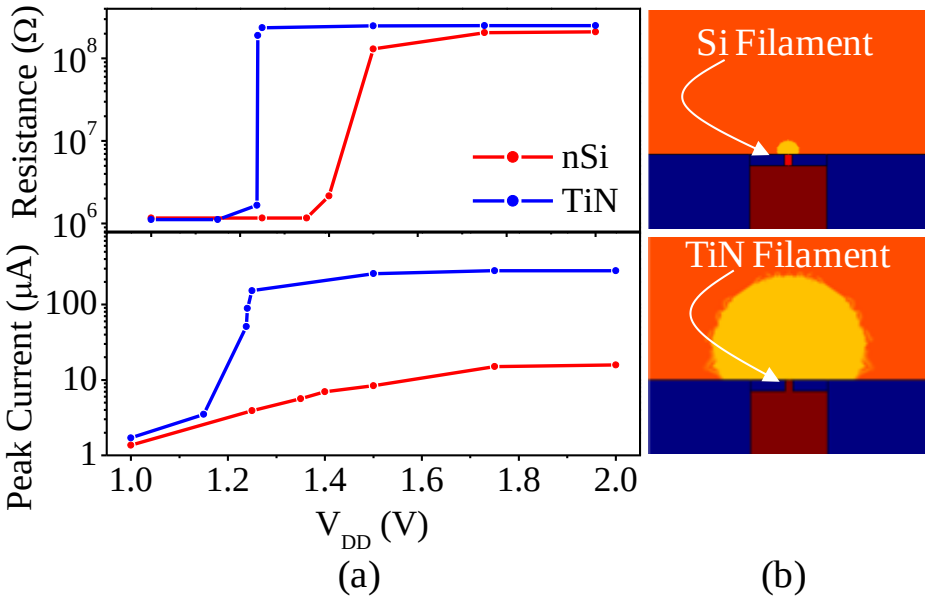


Figure 2-8 (a) The resistance ratio after the reset operation and the peak reset current as a function of the supply voltage. (b) The resulted amorphous region for the 2 nm Si filament and the 2 nm TiN filament (V_{DD} = 2 V , V_G = 1.5 V)

2.1.6 The Effect of Rise Time

Typical rise-times used in reset operation are in the same order as the heat diffusion time scales. Hence, the cells typically do not experience a uniform temperature distribution in this transient period. Shorter rise-times, in conjunction with GST's exponential decay in electrical resistivity with increasing temperature, leads to thermal runaway and formation of a molten filament within GST (**Figure 2-9**). If the pulse duration is kept sufficiently long, the molten filament widens and takes form of a candle flame and can finally collapse to a molten mushroom. However, rapid solidification is expected to amorphize all the volume which reach melting. Hence, the amorphized volumes tend to take an elongated form for shorter rise-times.

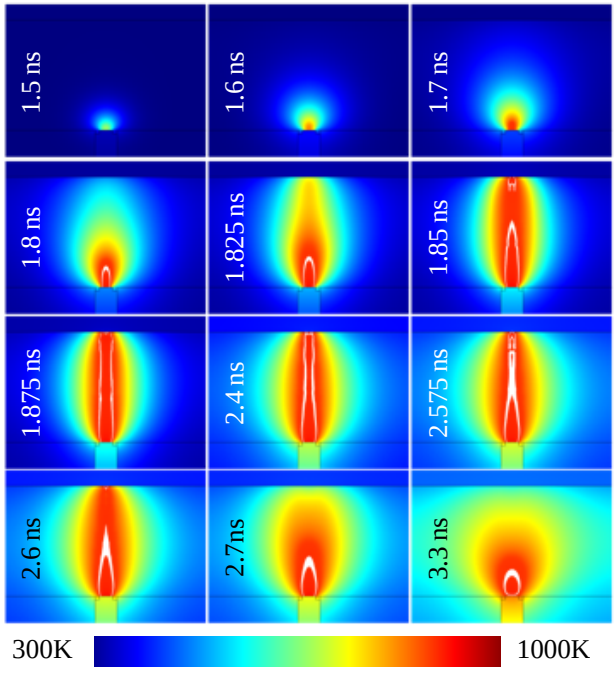


Figure 2-9 The thermal profile for rupture oxide cell showing the candle formation as result of a reset pulse with 0.5 ns rising time. (d_{FL} = 12 nm (V_{DD} = 2 V , V_G = 1.75 V).

The amorphization patterns for 0.5 ns to 97 ns rise-times are illustrated in **Figure 2-10**. The volume resolidified during the pulse can crystallize if the duration is kept > 100 ns or growth-from-melt takes place. Both of these possibilities are neglected in this study.

The read operations after the reset pulses show almost identical cell resistances (**Figure 2-11**) for all cases illustrated in **Figure 2-10**, even though the amorphized volume is very different. Hence, pulses with faster rise time tend to amorphize an elongated path rather than making an amorphous plug over the bottom contact, increasing switching energy by > 3x for the same resistance contrast: The reset pulse with τ_r = 97 ns consumes 23 pJ while the pulse with τ_r =0.5 ns consumes 80 pJ. It is worth mentioning that although the thermal runaway phenomenon was presented in the context of the rupture oxide cells, it can also take place in the conventional PCM cells.

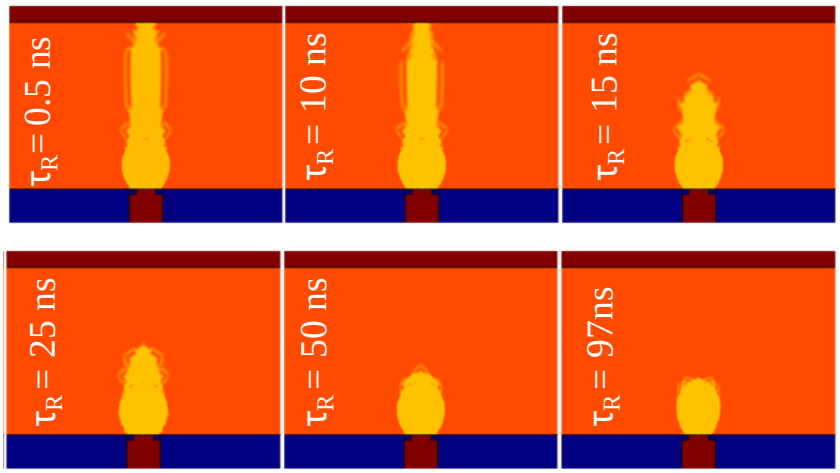


Figure 2-10 The conductivity profile for a rupture oxide cell as a result of changing the reset pulse rise time (τ_r). The cell has a filament diameter of 12 nm and is biased with a supply 2 V and a gate pulse of 1.75 V.

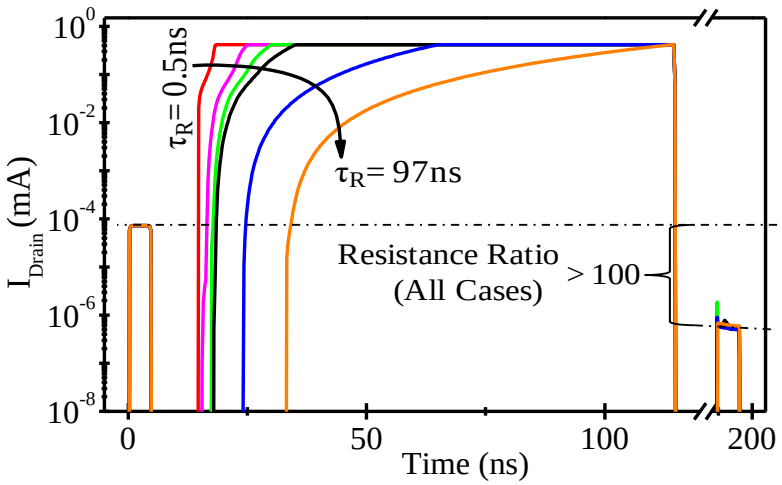


Figure 2-11 Transistor drain current for different reset pulse rise times.

2.1.7 The Analyses of RO-PCM Study Findings

In this chapter, rupture oxide PCM cells were evaluated using finite element simulations with temperature dependent materials parameters assuming an effective medium, while neglecting percolation and impact of grain boundaries. Rupture oxide cells can be operated using smaller voltages, currents and access transistors compared with the conventional mushroom cells. The cell behavior significantly depends on the size and the resistivity of the nanofilament formed in the oxide. Small and more resistive filaments lead to reduced energy consumption and improved resistance contrast. Narrower filaments have significantly sharper transitions between Set and Reset states at lower operation voltages. Performance of rupture-oxide cells with metallic filaments is expected to be comparable to conventional cells if the bottom contacts of the conventional cells can be fabricated to be as small as the filaments. Rupture-oxide cells with more resistive semiconducting filaments are expected to significantly outperform their conventional counterparts. Increased filament resistivity can result in > 10x

reduction in reset current and power consumption for the same resistance contrast but requires higher operation voltages. The resistivity of the filaments will be primarily determined by the composition of the rupture-oxide. It is to be noted that in actual devices, the location and size of the filaments cannot be exactly controlled. Increased variability will require larger than necessary operation voltages which impacts packing density and reliability along with power consumption. The requirements for fabrication of the rupture oxide cells are not as stringent as their conventional counter parts but they require an initial rupturing process prior to their use as memory elements. The results of this analysis show that rupture-oxide approach is viable for scaling of PCM, especially if narrow and resistive filaments can be reliably formed.

3. Multi Contact Phase Change Devices

3.1 Introduction

In the last chapter, it was shown that an elongated amorphous volume of GST could form between the bottom and top contacts if fast-rise-time pulses are applied. We have also showed that this operation incurs more energy and does not have any foreseen advantages for the vertical mushroom cells.

Phase change memory devices can be fabricated in a vertical (Mushroom cells) or lateral arrangement (like bridge cells), the ability to form elongated a-GST volumes in lateral devices can open the door of nonconventional operation and extended functionality. To better understand the mechanisms to form elongated aGST volumes, we did extensive analysis on a simple lateral GST device that emulates the mushroom cell device structure; we examined the effect of changing the top contact width on the formed GST plug shape. We realized that linear GST volumes can be achieved with slow write pulse rise time if the width of the contacts is made narrow enough. Figure 3-1 illustrates the effect of varying the top contact width on the formed amorphous volume. The reduction of the top contact width results in forming an amorphous volume that extends between the top and bottom contacts. Shrinking the width of the top contact, in this case, confines the current to the straight path between the contacts and result in melting an elongated GST volume (refer to Figure 3-2). Furthermore, wider top contacts operate as heat sinks. As the contacts width shrink they start acting as heater contacts, which in turn, enhances the thermal runaway and result in forming the elongated amorphous volumes as well.

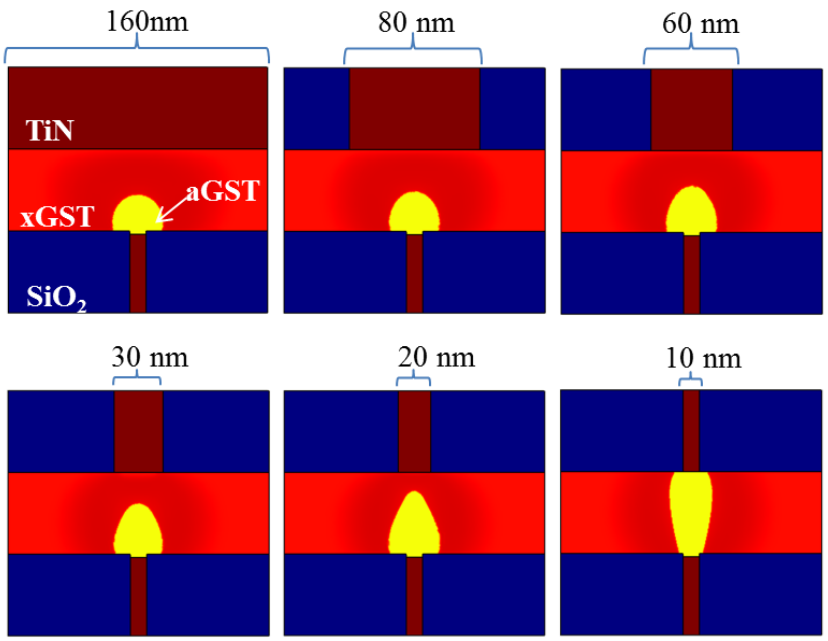


Figure 3-1 The formed a-GST volume for different lateral mushroom devices with different top contact widths. Larger top contacts operate as heat sinks and yield to the formation of mushroom like amorphous plugs, while narrow top contacts resulted in a more elongated a-GST plugs.

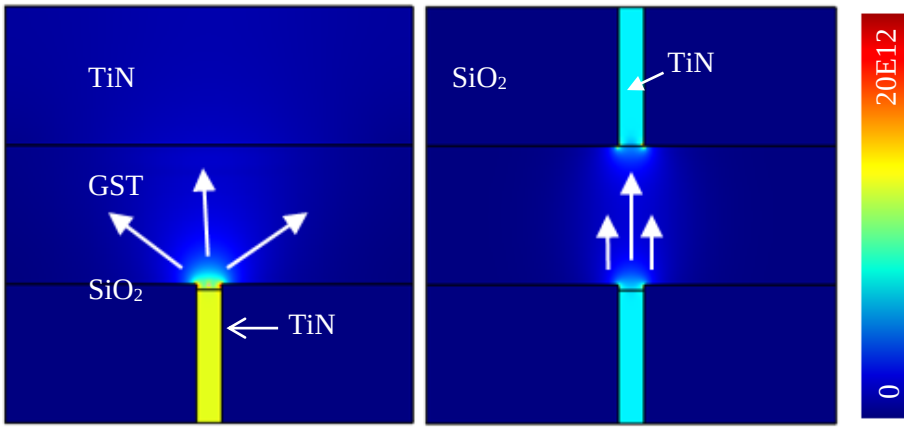


Figure 3-2 Current Density during the write operation for a two PCM cells with different top contact widths. The scale bar has the units of A/m^2.

3.2 Multi-contact GST patch

Different geometries of multi-contact lateral GST devices are studied to explore the advantages of forming linear a-GST regions; a simple device is shown in Figure 3-3 that is a square GST patch with four metal contacts at each of its corners. The square GST patch is interfaced with FET access devices at three of its terminals and the forth terminal is connected to the ground. Passing sufficient current between any subset of the terminals resulted in forming a strip of the a-GST. Depending on the activated subset of contacts, the formed a-GST strip can isolate different parts of this simple device. We also have looked into the effect of the pulse timing and the sequence of pulses on the formed a-GST volumes; as it can be seen from Figure 3-4, various a-GST formations can be obtained for different sequences of the applied write pulse.

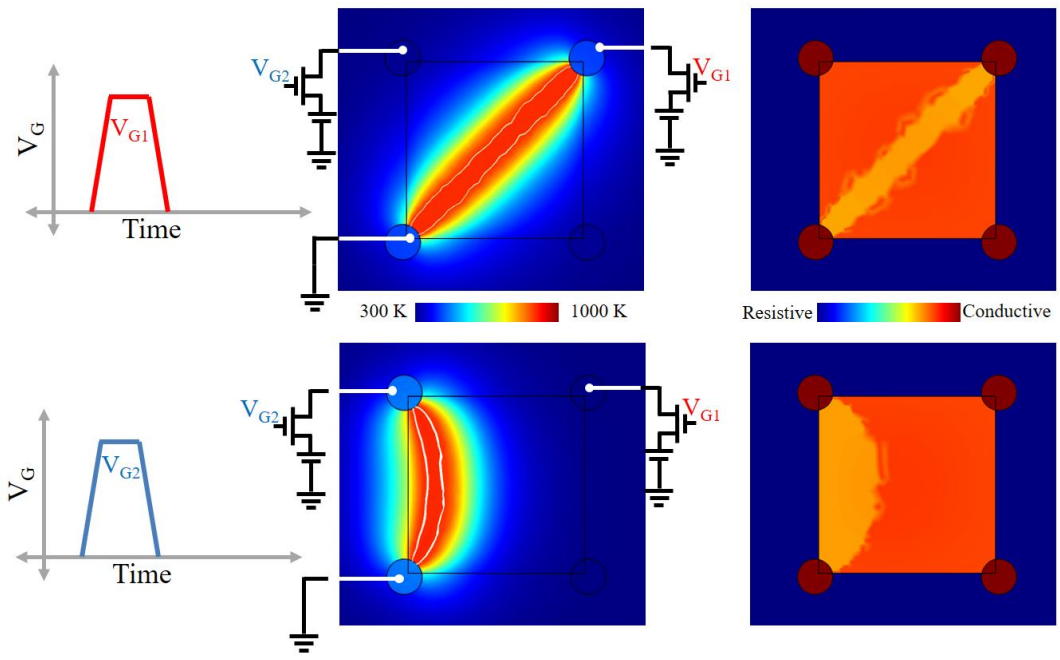


Figure 3-3 Simple square GST patch with four metal contacts; passing sufficient current between any two contacts results in forming an amorphous strip between them.

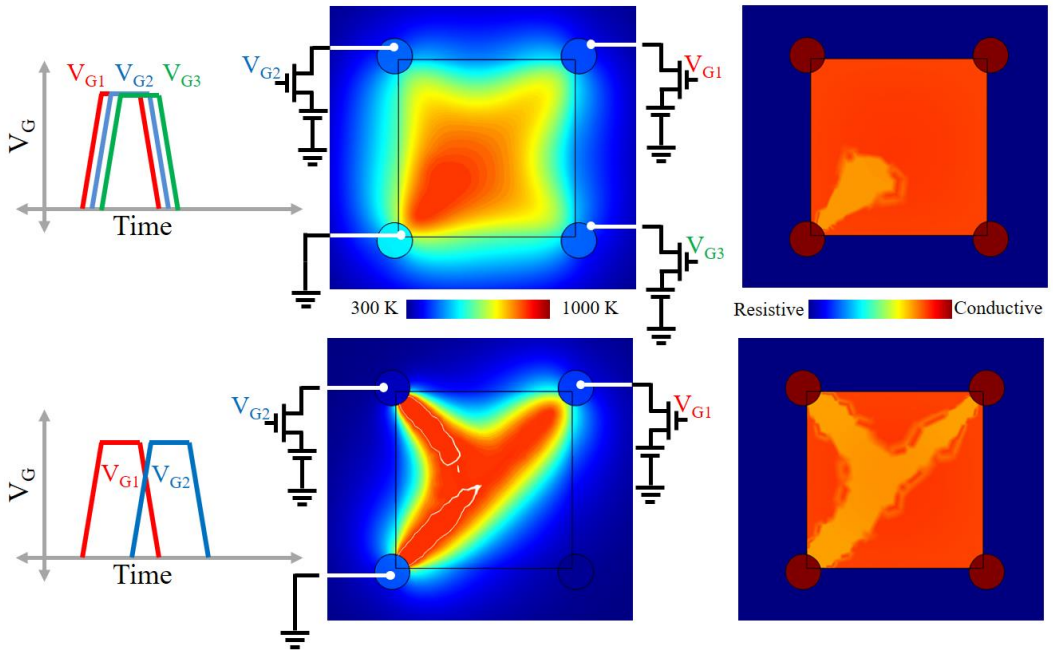


Figure 3-4 An illustration of how controlling the sequence and the timing of the applied pulses can result in different formations of the amorphous strips.

The initial investigations of the simple GST square patch paved the path to study more complicated device structures with higher number of contacts and more useful functionality. In the next subsection, we will introduce an eight-contact device that is capable of achieving the signal routing functionality.

3.3Phase Change Pipe for Nonvolatile Routing

The 8-contact phase-change-pipe device concept discussed here is designed to control data routing between 2-input and 2-output terminals using 4-write terminals. The operation of the proposed device is achieved by forming highly resistive amorphous strips between pairs of 'write' (control) terminals; isolating sections of the phase change element (Figure 3-5). Depending on the sequence at which the control contacts are activated, different amorphous strips are formed leading to a variety of device configurations.

3.3.1 Device Description and Proposed Fabrication Steps

For the 8-contact GST rectangular thin-film "patch" shown in Figure 3-5, passing sufficient current between W_1 and W_3 contacts to self-heat, melt followed by a sudden quench forms an aGST strip between these contacts. If this operation is repeated between W_2 and W_4, another aGST strip can be formed isolating the in-between xGST regions

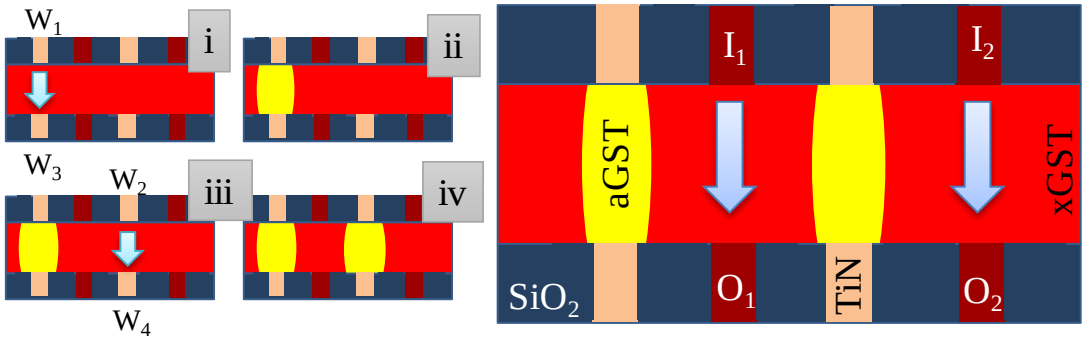


Figure 3-5 Isolation of crystalline sections on a GST patch with the 8 TiN contacts; current flow between the activated write terminals resulting in amorphized strips that isolate the conductive regions.

from each other. Hence, any electrical signal applied to I_1 shall be easily passed to O_1 without affecting the other terminals. The same is also true for I_2 and O_2 terminals. Hence, the GST patch is configured to have $I_1 = O_1$ and $I_2 = O_2$ for this specific case.

Other configurations can be written by passing sufficient current through the different pairs of write-contacts ($W_1 \rightarrow W_4$). The patch has to be interfaced with access devices, such as MOSFETs, to control the write and read operations (Figure 3-6). For instance, applying a voltage pulse to the gates W_1 and W_4 while keeping the other gates at ground potential (writing with W_{1234}= 1001), will lead to an aGST strip formation between W_1 and W_4. The configuration shown in Figure 3-6 was achieved by two consecutive write words (1010, 1001). The write pulses have to be short (≤ 10 ns) to prevent the recrystallization of the previously formed aGST strips for that configuration

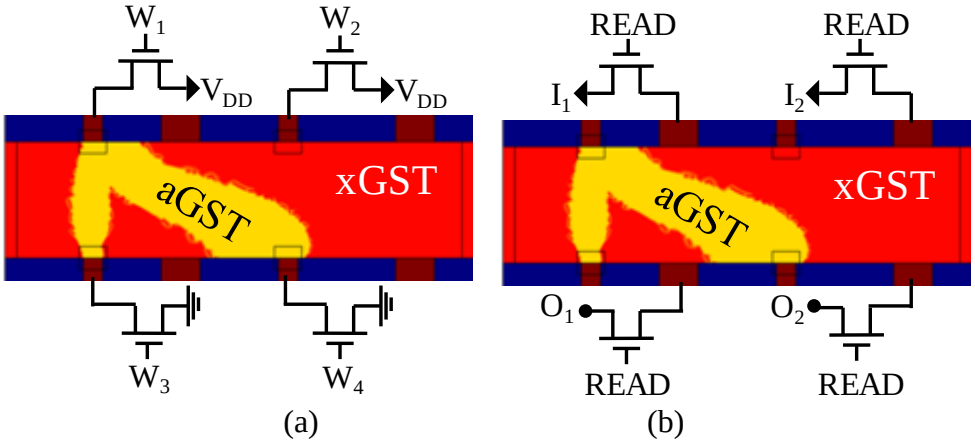
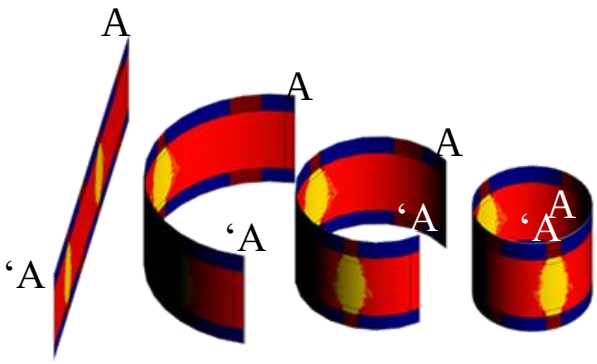
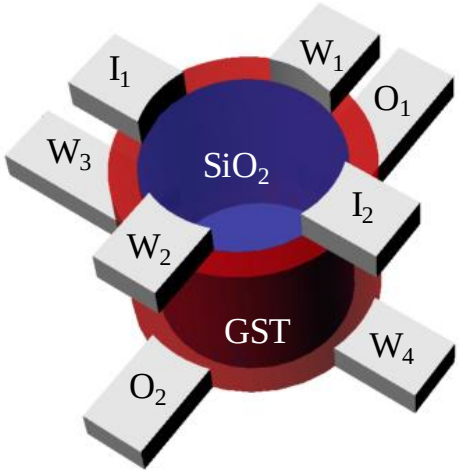


Figure 3-6 Simulated 8-contact phase-change patch with 2-inputs (I), 2- outputs (O) and 4-write terminals (W) showing the access transistors for write (a) and read (b) operations.

The possible configurations of the GST patch are limited due to its 2D nature. However, significantly improved functionality can be achieved if a swap function ($O_1 = I_2$, $O_2 = I_1$) can be implemented. This is possible if the two sides (left and right edges) of the patch are connected together (Figure 3-7a) in a ring geometry, forming a GST pipe where the height and the diameter of the pipe are significantly larger than the wall thickness (Figure 3-7b). Such geometry can be fabricated using a side-wall process as illustrated in Figure 3-8.



(a)



(b)

Figure 3-7 (a) 3D schematic view of the wrapped 2D GST patch. Connecting the two edges of the 2D GST sheet allow a swap function. (b) Schematic view of the phase change pipe and the contact configurations that forms the phase-change router.

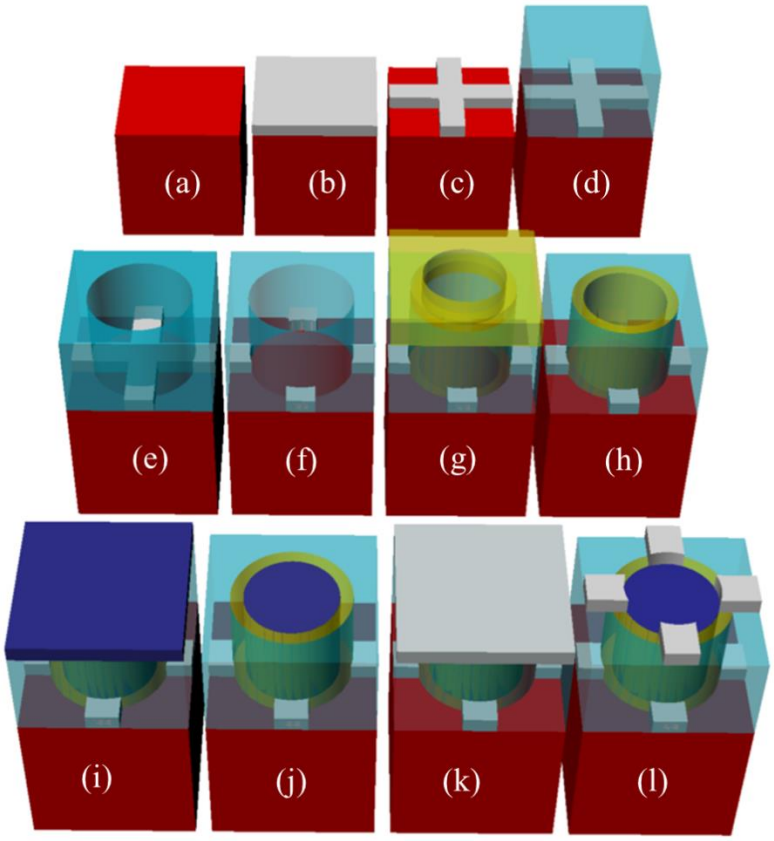


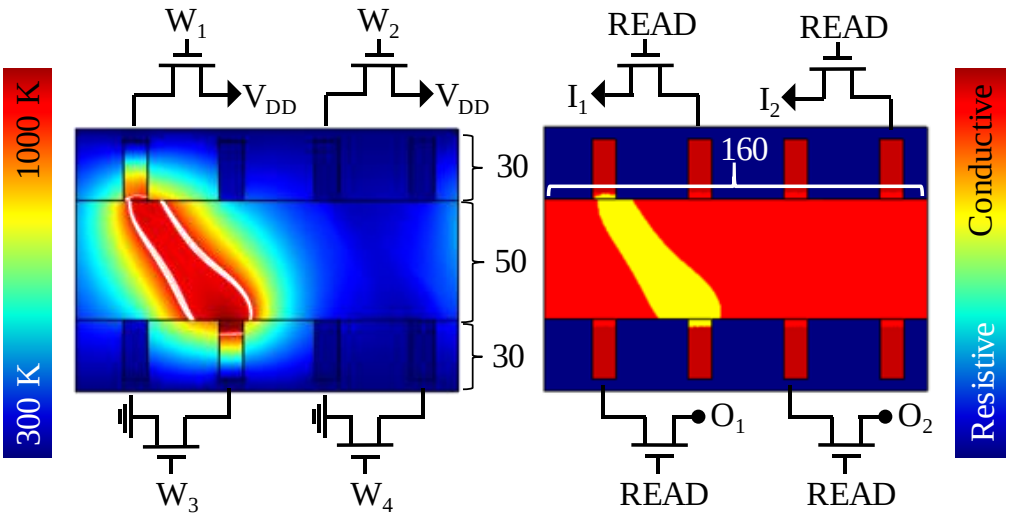
Figure 3-8 Schematics of a sample fabrication procedure for the GST pipe: Thermal oxide growth on Si (a) followed by a thin metal layer deposition (b), etching to form a cross with 4 contacts (c), SiO_2 deposition (d), lithography and etching of SiO_2 forming a well (e), metal etching (f), GST deposition (g), reactive ion etching (RIE) of GST, making a GST side-wall (h), deposition of an insulating layer (SiO_2 or Si_3N_4) (i), planarization (j), metal deposition (k), and top electrode definition (l).

In this short-pipe geometry, the top and the bottom write terminals are staggered (W_1 aligned with O_1, I_1 aligned with W_3, etc.) to force the current flow in diagonal paths. This makes the amorphization paths equal in length and ensures a symmetric device operation for all write combinations

3.3.2 Device Modelling and Simulation Results

The schematic of the modeled PCM-Router is shown in Figure 3-9. The pipe is modeled by an LxWxD = 110x160x10 nm GST patch with eight TiN contacts. Periodic boundary conditions are applied at the left and the right sides of the patch to simulate the pipe structure. The finite element simulation model included temperature dependent material parameters, thermal boundary resistance, and thermoelectric effects.

The electro-thermal simulation platform presented in the previous chapter was extended and modified to include more detailed crystallization model (eqn. 3 below).



(a) (b)

Figure 3-9 Schematics of the modeled phase change pipe with indicated dimensions in nm, the periodic boundary conditions are applied to A and A' axes. (a) Peak thermal profile while applying a 3.5 V write pulse that activates transistors W_1 and W_3 (W_{1234} = 1001), The white contour lines denote the boundaries of the melting GST. (b) The resulting conductivity profile after sending the write word showing the amorphized regions in yellow.

The development work to extend this model was mainly carried by Zack Woods of the Nanoelectronics Lab at UCONN. This comprehensive model facilitates the tracking of local crystallinity and material properties that depends on the thermal history. In this simulation platform, a crystal density approach is employed where each mesh point is tracked by a variable (CD) that represents a crystallinity fill factor; this technique allows for the use of non-uniform meshing which provides for more numerical flexibility compared with the discrete (either crystalline or amorphous) approach.

CD is self-consistently solved for using a rate expression that relies on the published growth velocities and nucleation rates [51]; the rate equation is a function of local CD and T, and CD of neighboring mesh elements; this equation captures nucleation-and-growth, growth-from-melt and amorphization:

$$\frac{dCD}{dt} = Nucleation\,(T, CD, random) + Growth\,(T, CD) + Diffusion\,(T, CD) * \nabla^2 CD - Amorphization(T, CD) \qquad (3)$$

The diffusion function captures the mesh-point to mesh-point interaction of crystallinity.

Figure 3-10 shows the simulated pulse sequence for the writing operations of {O_1 = I_1, O_2 = I_2} and {O_1 = I_2, O_2 = I_1} configurations along with the resulting thermal profiles and the resistivity maps. Some of the other simulated configurations are shown in Table 1. Each of the configurations in Figure 3-10 is achieved by sending two write words with sufficient time in-between to allow the device to cool down.

The configurations are read by applying overlapping voltage pulses to the I_1 and I_2 and measuring the currents passing through the O_1 and O_2 outputs (Figure 3-11). Table I, illustrates the read/write voltage and current levels as well as the corresponding on/off resistance values. The device can be erased by applying a longer duration (> 20 ns) lower

amplitude (< 2 V) pulse to all write terminals. The access transistors have to be sized properly to satisfy the current and energy requirements for the write operation. For the device in Figure 3-9 transistors with LxW = 22x110 nm were used to deliver a peak power of 230 μW. A total energy of ~2.5 pJ was required to form an aGST strip. The current requirements primarily depend on the device dimensions and the phase change material. Other phase change materials can be utilized for lower-power operation if the applications do not require 10 year retention of the configured state at 90 C, which is excessive for logic operations.

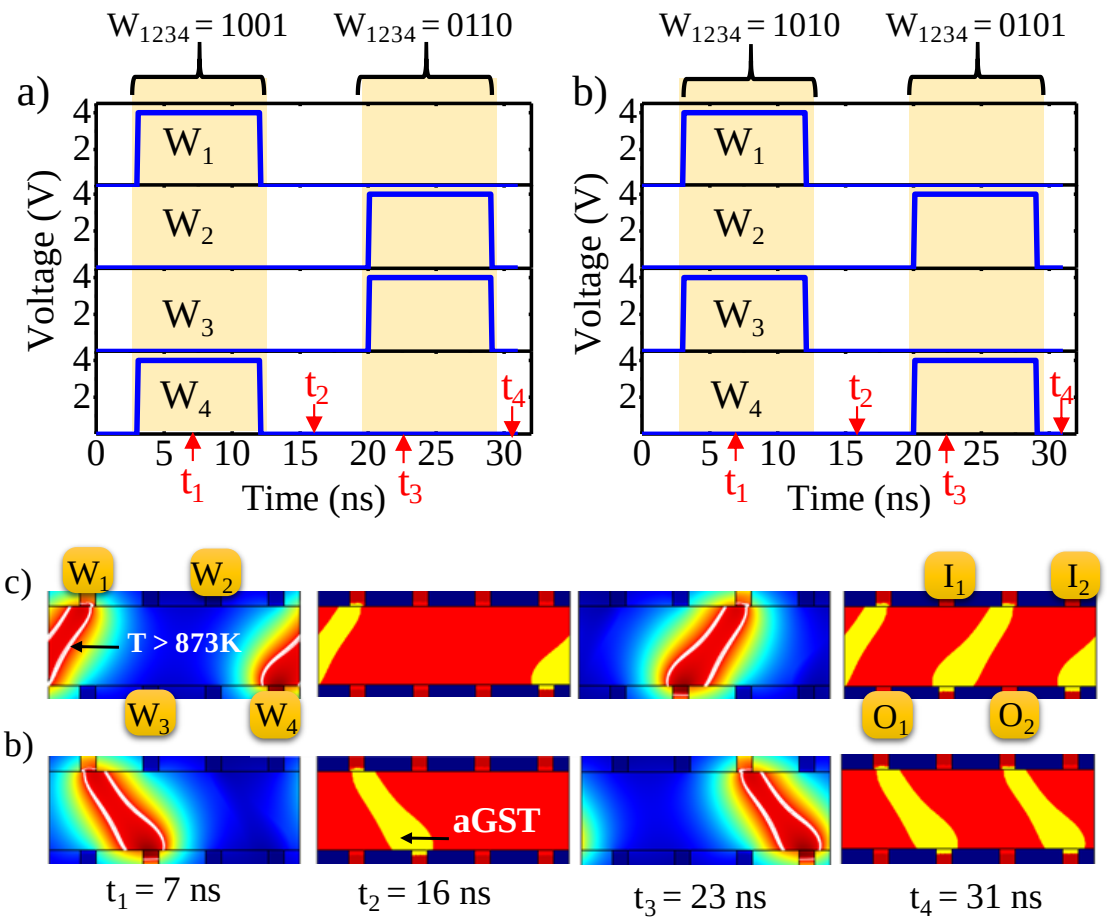
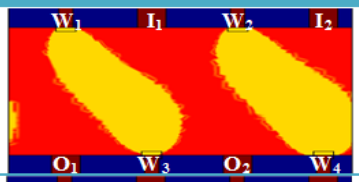
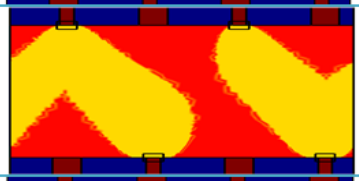


Figure 3-10. The write pulse sequence for {$O_1 = I_1$, $O_2 = I_2$} configuration (a) and {$O_1 = I_2$, $O_2 = I_1$} configuration (b). The thermal profiles at (t_1, t_3) and the resulting conductivity maps at (t_2, t_4) during the write operation of {$O_1 = I_1$, $O_2 = I_2$} (c) and {$O_1 = I_2$, $O_2 = I_1$} (d) configurations.

Table 3-1 Possible input-output configuration with the corresponding write commands and achievable truth table

	Configuration	Description	Write Command(s) ($W_1W_2W_3W_4$)	Implemented Functions O_1 and O_2		
1		$O_1 = I_2$ $O_2 = I_1$	Two write words (0101) , (1010)	**I_1I_2**	**O_1**	**O_2**
				00	0	0
				01	1	0
				10	0	1
				11	1	1
2		$O_1 = I_1$ $O_2 = I_2$	Two write words (0110) , (1001)	**I_1I_2**	**O_1**	**O_2**
				00	0	0
				01	0	1
				10	1	0
				11	1	1
3		Output O_2 isolated	Two write words (0110) , (0101)	**I_1I_2**	**O_1**	**O_2**
				00	0	0
				01	1	0
				10	1	0
				11	1	0
4		input I_1 isolated	Two write words (1010) , (0110)	**I_1I_2**	**O_1**	**O_2**
				00	0	0
				01	1	1
				10	0	0
				11	1	1
5		input I_2 isolated	Two write words (1001) , (0101)	**I_1I_2**	**O_1**	**O_2**
				00	0	0
				01	0	0
				10	1	1
				11	1	1
6		Output O_1 isolated	Two write words (1010) , (1001)	**I_1I_2**	**O_1**	**O_2**
				00	0	0
				01	0	1
				10	0	1
				11	0	1
7		Output O_2 and input I_1 are isolated.	Three write words (1010) , (0110), (0101)	**I_1I_2**	**O_1**	**O_2**
				00	0	0
				01	1	0
				10	0	0
				11	1	0
8		Output O_1 and input I_2 are isolated.	Three write words (1001) , (1010), (0110)	**I_1I_2**	**O_1**	**O_2**
				00	0	0
				01	0	0
				10	0	1
				11	0	1
9		Device is totally isolated.	Four write words (1001), (1010), (0110), (0101)	**I_1I_2**	**O_1**	**O_2**
				00	0	0
				01	0	0
				10	0	0
				11	0	0

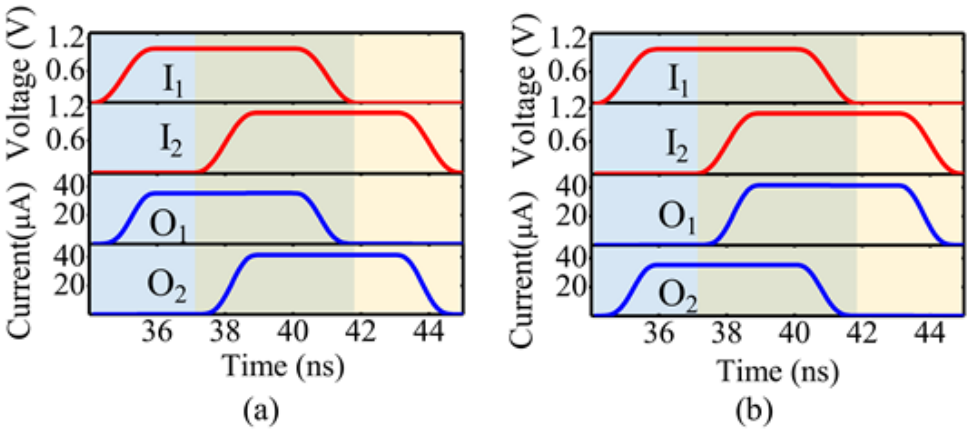


Figure 3-11 Device read operation showing applied voltages on the input terminals transistors' gates and the measured currents at the output terminals for {$O_1 = I_1$, $O_2 = I_2$} configuration (a) and {$O_1 = I_2$, $O_2 = I_1$} configuration (b).

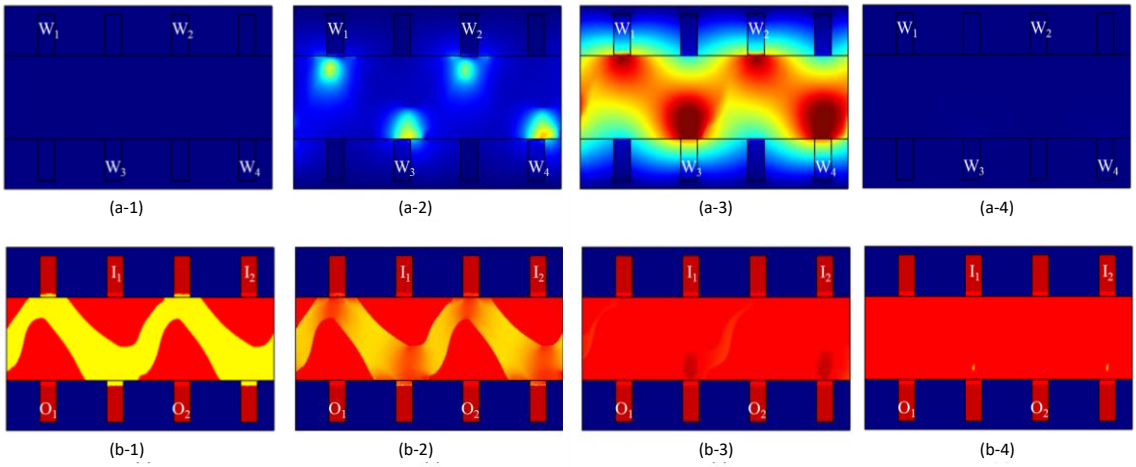


Figure 3-12 Frames from device erasing process, the frames on the top show the thermal profile during and the frames on the bottom show the resistivity map.

For the chosen device dimensions, a total energy of 2.5 pJ was required per amorphous strip. The write access transistors were sized to have LxW = 22x110 nm to satisfy the current requirements to achieve xGST to aGST phase transition.

3.4Phase Change Patch for Nonvolatile Routing

The 2 x 2 router functionality can be achieved by an alternative planner structure compared to the pipe geometry of the previous subsection. In this case, the side to side electrical connection is achieved by short circuiting two extra side contacts as is depicted in Figure 3-13. This device operates exactly as the pipe device and it can be configured with high-speed pulses to amorphize the paths between the top contacts and the bottom contacts. Pulses would be applied in a sequential fashion to each pair. Similar to the pipe device, pulse durations would be kept short to avoid recrystallization of the paths for the second pulse of the sequence. The first pulse can be kept long to recrystallize the areas amorphized in the last pulse sequence.

The major limitation of this device compared with the pipe device, is that this device would require more energy. The two new contacts on the sides add extra resistance to the device and eliminate the side-to-side thermal connection. Forming an amorphous strip, across the side contacts, in the planner device requires ~3 pJ while only ~2.5 pJ were required to form the amorphous strip in the pipe case.

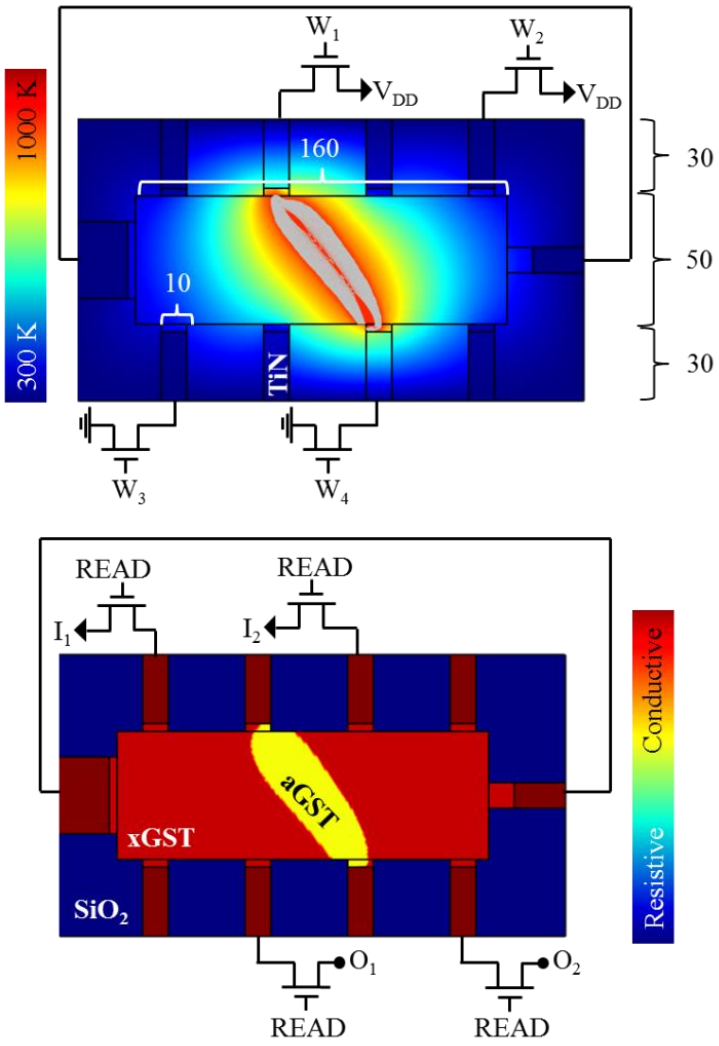


Figure 3-13 Simulated thermal profile during a write pulse (top) and the resulting resistivity map during the read cycle (bottom) for a planar 10-contact router structure. The identified dimensions are measured in nm. The side contacts are electrically short circuited through a wire. Sizing one of the side contacts wider than the other is desired to decrease the electrical resistance. Blocking of the narrower contact with amorphized GST is sufficient to electrically isolate the two sides.

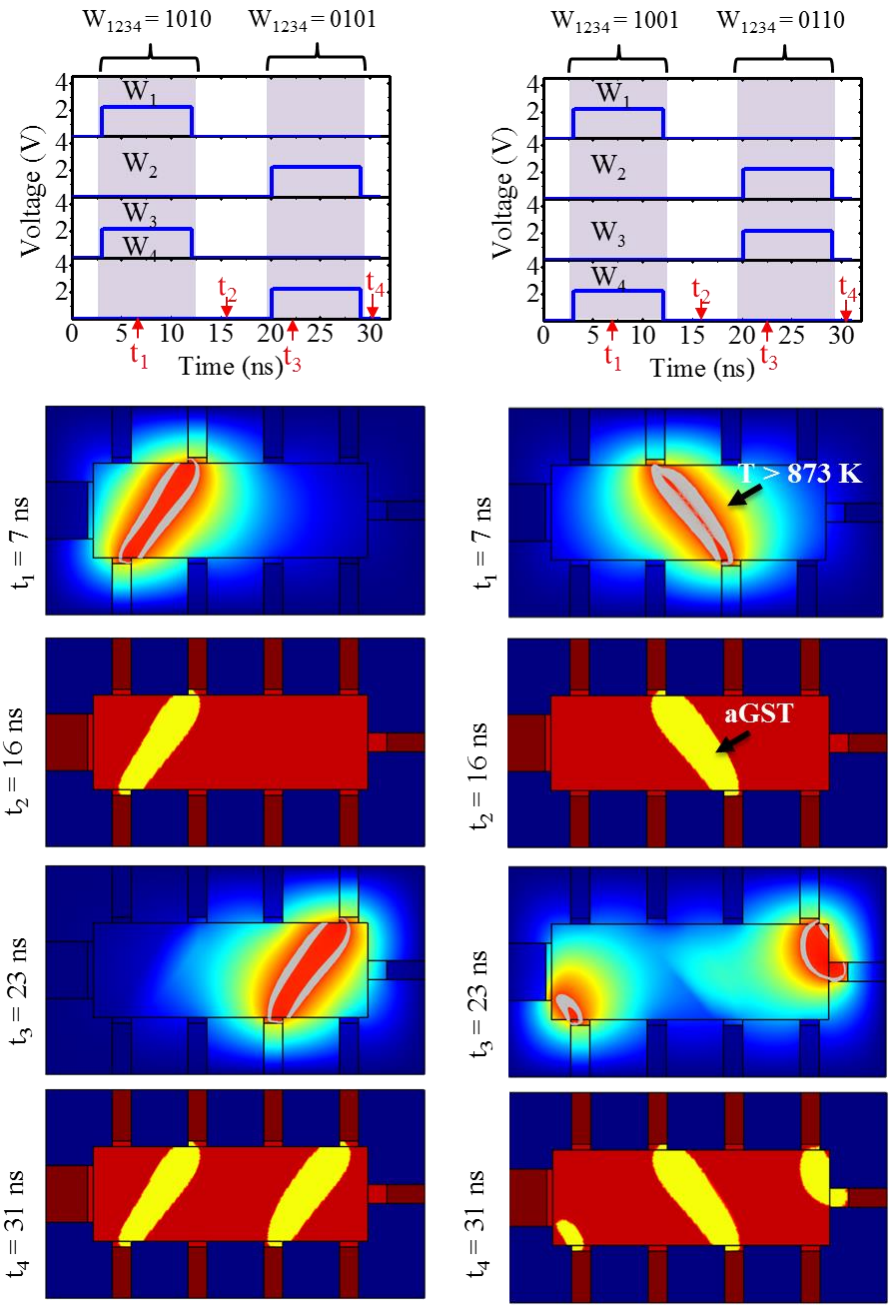


Figure 3-14 The write pulse sequence for {$O_1 = I_1$, $O_2 = I_2$} configuration (a) and {$O_1 = I_2$, $O_2 = I_1$} configuration (b). The thermal profiles at (t_1, t_3) and the resulting conductivity maps at (t_2, t_4) during the write operation of {$O_1 = I_1$, $O_2 = I_2$} (c) and {$O_1 = I_2$, $O_2 = I_1$} (d) configurations.

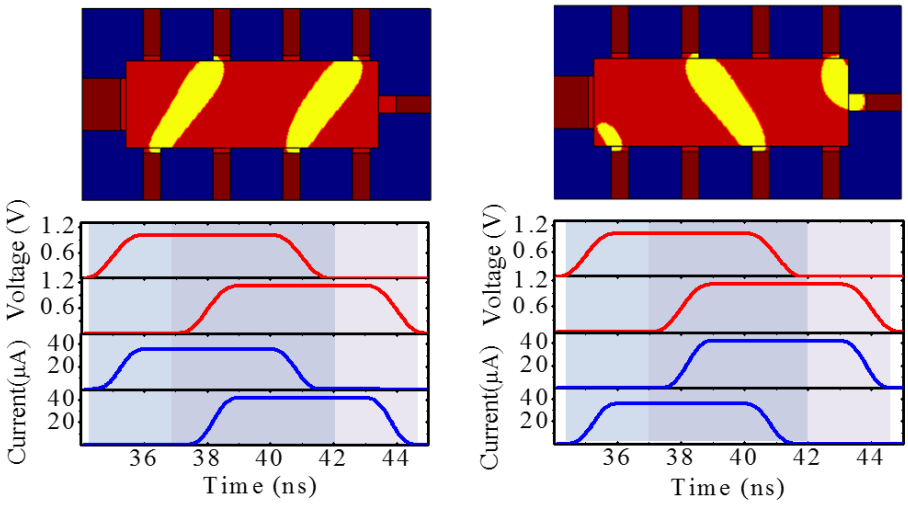


Figure 3-15 Device read operation showing applied voltages on the input terminals transistors' gates and the measured currents at the output terminals for $\{O_1 = I_1, O_2 = I_2\}$ configuration (a) and $\{O_1 = I_2, O_2 = I_1\}$ configuration (b).

We have simulated 10-contact structure (**Figure 3-14**) using the same simulation platform used for the pipe structure. A wider contact is used on the left-side to reduce electrical resistance for this realistic design. The pulse sequence and the timing is shown for two configurations in Figure 3-14.

For the devices presented in the chapter, GST material parameters are used for the phase change material. It is worth mentioning that, it is possible to achieve much faster operation than what is shown through the thermal engineering of the structures, sizing the access devices and engineering the write pulses. The energy requirements the access transistor sizes mainly depend on the chosen device dimensions and the phase change material. The results show the promising potential of these devices for complementing high-performance VLSI as well as reconfigurable logic.

4. Utilization of Thermal Runaway for sequential operation in multi-contact phase change devices.

In phase-change memory devices, the thermal runaway occurs due to the exponential decay of resistivity in response to temperature rise. Passing current through these devices leads to joule heating, which results in reduced resistance and thermal runaway [52]–[57]. Thermal runaway can be controlled by the appropriate choice of the access device [45],[30]. For instance, in PCM mushroom cells FETs are used to limit the current and control the PCM switching.

In this chapter, we demonstrate how the thermal runaway can be utilized to achieve sequential operation. We will begin with a step-by-step operation description and simulation of the sample trapezoidal device interfaced with a single access device shown below (Figure 4-1).

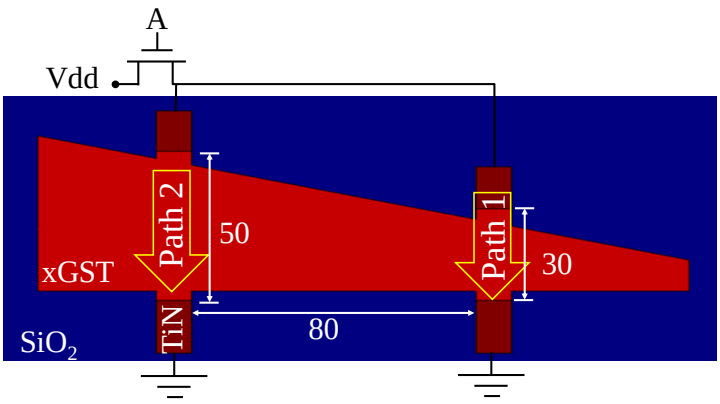


Figure 4-1 Sample trapezoidal GST device with indicated dimensions in nm showing the two major current paths.

When the transistor gate, A, is activated with the sufficient voltage the trapezoidal device will have two major current paths as is shown in Figure 4-1. The transistor operates in the saturation regime and the voltage source with the transistor can be represented as a current source parallel to a resistance and a switch, the two major paths can be represented as two different variable resistances R_1 and R_2. The equivalent circuit is represented in Figure 4-2. Here, The mutual path to path resistance is ignored.

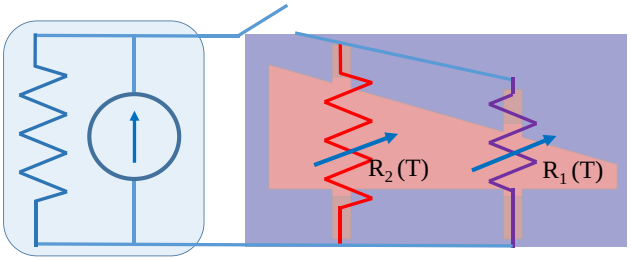


Figure 4-2 The equivalent circuit representation of the trapezoidal device.

For the shown device dimensions and geometry $R_1 < R_2$ due to the length difference of the respective current paths, furthermore, R_1 and R_2 are functions of temperature and decay exponentially as current flows in them due to joule heating and thermal runaway.

Assuming that the device is initially in the crystalline phase; when the switch is closed, i.e. the transistor gate A is activated, more current will flow in R_1. This will result in heating R_1 more than R_2. Consequently, R_1 resistance will drop even further and faster than R_2 and will attract even more current due to the thermal runaway. This positive feedback will result in short-circuiting R_2 (depending on the minimum value that R_1 will reach). In the context of phase change materials: there are about 2-4 orders of magnitude in resistance difference between an amorphous or crystalline phase and the molten liquid

phase. Hence, minimal current will flow R_2 (Figure 4-3a). As it can be seen in Figure 4-4, as the voltage difference across the device terminal increases the shorter path starts to heat up faster than the longer path, hence, attracting more current leading to its melting; the remainder current that flown in the longer path has led to a slight temperature increase but not to melting or phase transition. When the switch is open again, the molten phase change material rapid melt-quench resulting in a crystalline to amorphous phase transition of R_1 (Figure 4-3b).

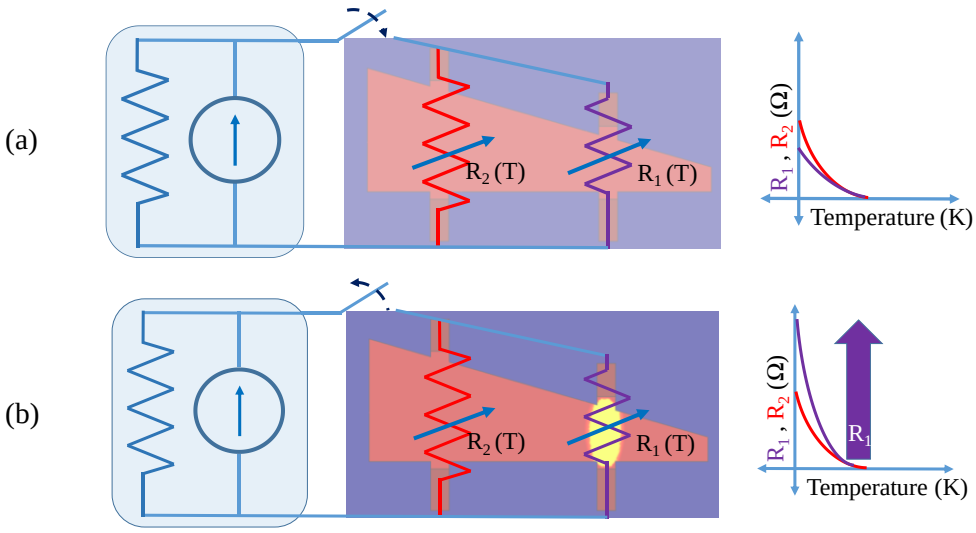


Figure 4-3 Illustration of transistor switching, more current will follow in R_1 due to the geometric length difference which would result in a faster thermal runaway and short-circuiting R_2 (a). Illustration for the device status after opening the switch showing the formed a-GST plug on path 1 (R_1) highlighting the resulted resistance increase due to the phase change (b).

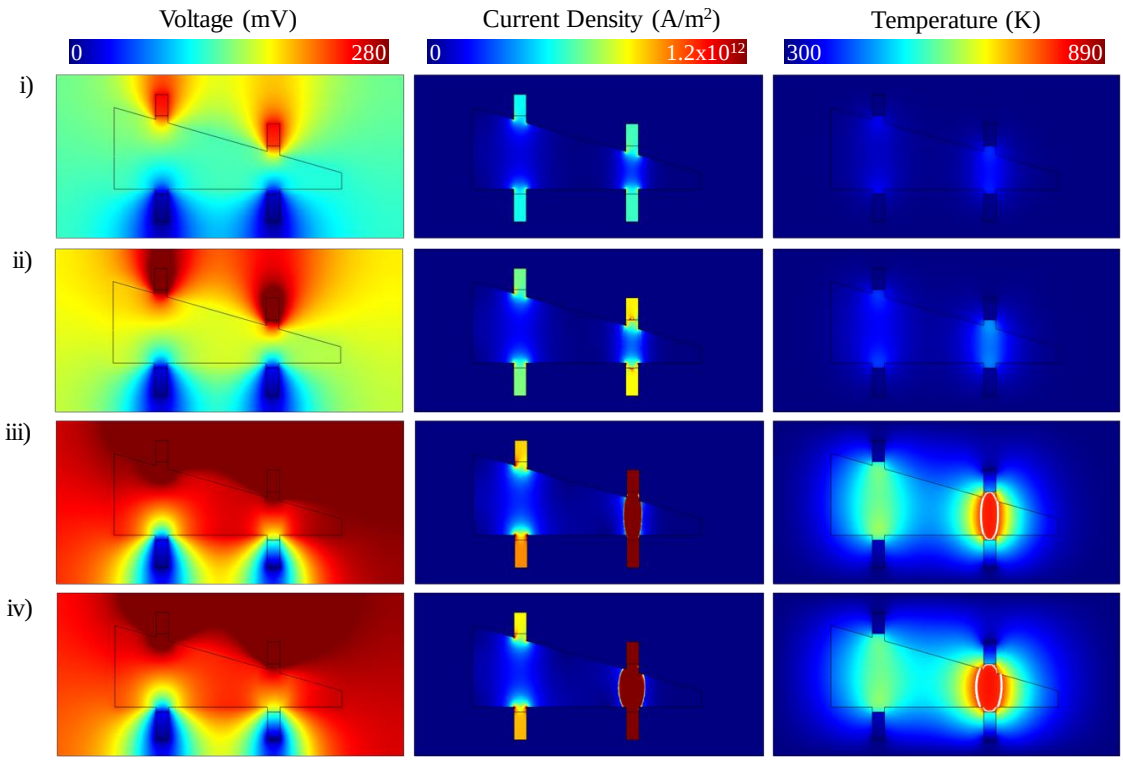


Figure 4-4 The simulation timeframes of the voltage, current density distribution and thermal maps during the application of a voltage pulse (V_{GATE} = 2.2 V) on a fully crystalline device.

When the switch is closed for the second time R_1 will have much higher resistance compared with R_2 and the current will mainly flow in R_2 and result in self heating that path leading to the crystalline to amorphous phase transition (Figure 4-6). Assuming that the pulse duration is short and the generated heat is not sufficient to alter the phase status of the previously written path (R_1) the device now will have two different amorphous strips (Figure 4-5).

This simple illustration shows that it is possible to achieve more than two states of the device using a uniform input signal in a sequential matter by utilizing the thermal

runaway. With this approach, we can selectively activate a certain pair of contacts without the need of having a dedicated access device in multi-contact devices.

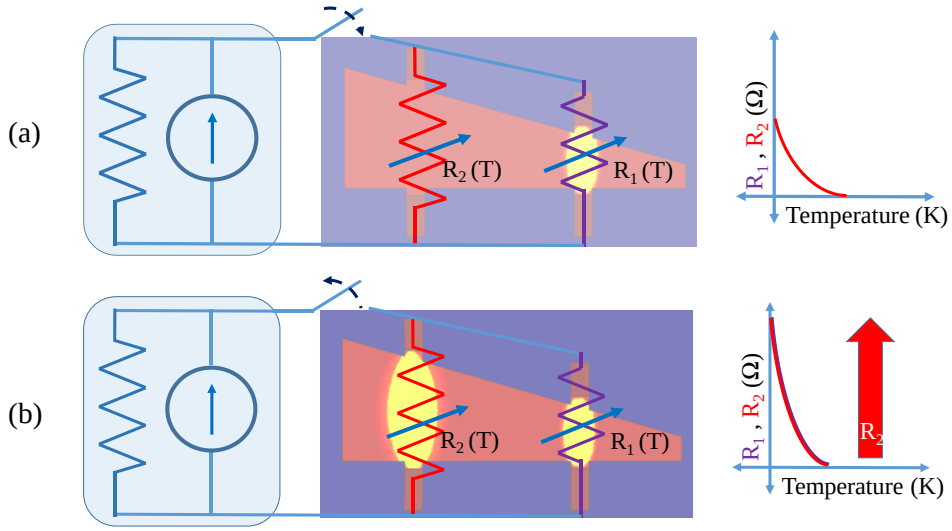


Figure 4-5 Illustration of transistor switching after the first pulse, more current will follow in R_2 as R_1 is in the highly resistive amorphous state, consequently, R_2 will undergo a crystalline to amorphous phase transition (a). An Illustration for the device status after opening the switch showing the formed a-GST plug on path 2 (R_2) highlighting the resulted resistance increase due to the phase change (b).

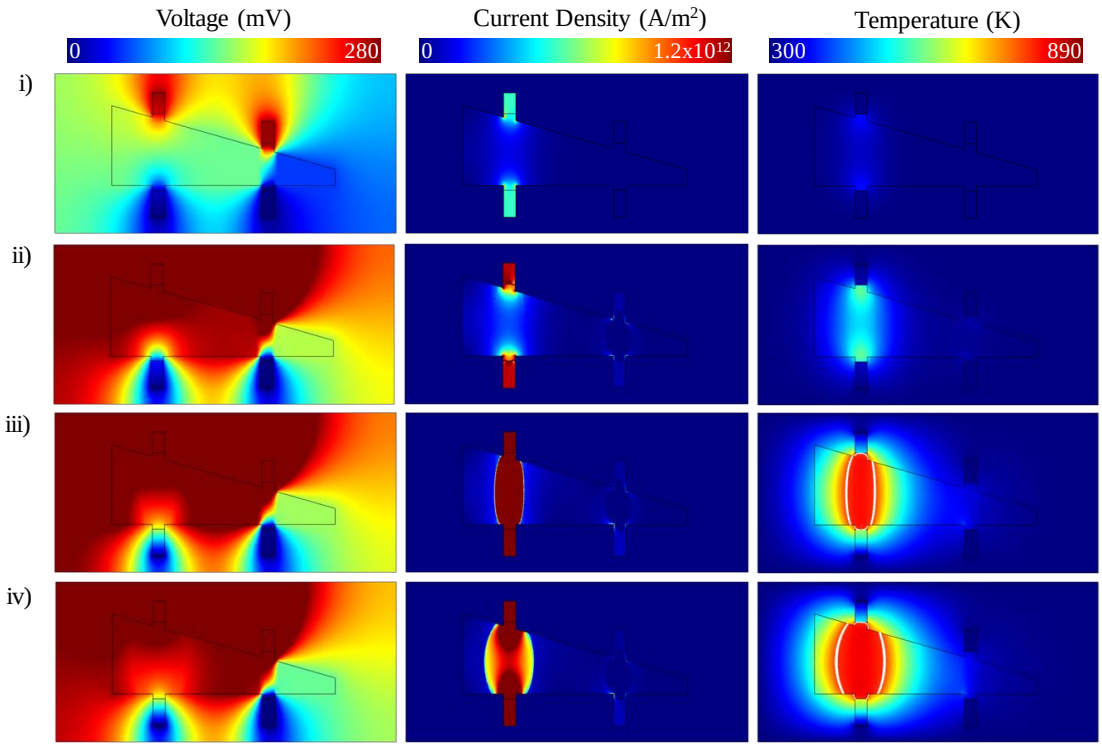


Figure 4-6 The simulation timeframes of the voltage, current density distribution and thermal maps during the application of a voltage pulse (V_{GATE} = 2.2 V) on a previously pulsed device and formed amorphous GST strip. Compared with the first pulse, the shorter path has almost no current as it is in the highly resistive amorphous phase.

A straightforward application of this concept is a onetime counter that is illustrated in Figure 4-7. This device has four access transistors: designated as two write devices and two read devices. The read device will always read low resistance (high current) unless the right number of right pulses is applied. This device can be useful in in security applications were the device enters a hardware lock state after certain number, 3 in this case, of wrong access trials. Due to the fact that this device will always change its status for every write pulse and consumes roughly the same power, it is immune to the

side-channel attacks, were the functionality of the devices is revealed through the monitoring of power consumption at the chip.

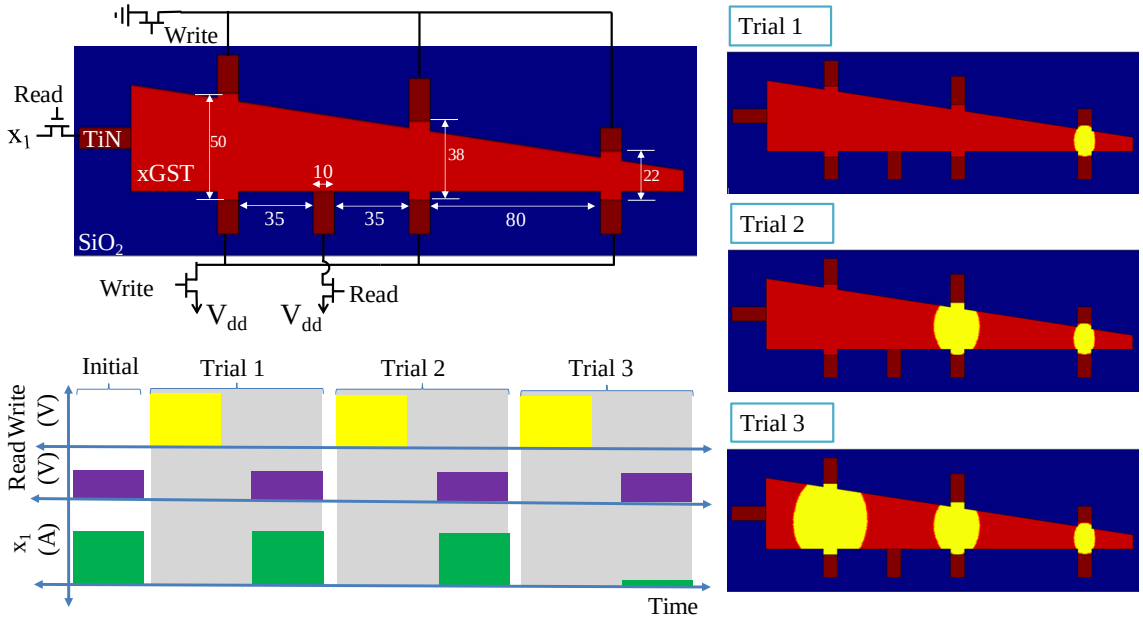


Figure 4-7 An illustration of a onetime 3 bit counter operation, the device is initially in the crystalline state and the current read through terminal x_1 is high, as the number of trials increases (write pulses applied) the shorter crystalline paths phase change to the amorphous phase; once the maximum number of trials is reached the device will be locked and only a small amount of current can be read through x_1 terminal.

In the previous examples, we showed that the thermal runaway can be utilized to selectively amorphize portions of PCM devices that are different in the geometric lengths. The shorter paths will have more current flowing in them, hence, they amorphize earlier and so on. In a symmetric PCM device, where all the paths are of equal lengths,

the grain orientations and boundaries can result in a resistance mismatch leading to sequential operation but in a random fashion.

A sample device that makes use of the random current path selection is shown in Figure 4-8. In this device, Path 1 and Path 2 have the same length but their resistances are slightly different due to the variations in the grain sizes and grain boundaries. Sending a write pulse will only amorphize one path at a time due to thermal runaway; if Path 1 was less resistive it will amorphize first the device will read 1; instead if Path 2 was the least resistive it will amorphize first the device will read 0. Having a string of these devices can be used to generate a unique and totally random signature code; the process variations and nucleation randomness will assure the variation of device to device operation.

The utilization of thermal runaway to achieve sequential device operation is illustrated by two different sample devices, as is mentioned previously; both of these devices are suitable for a one-time operation as the device will lock in the last achieved state. More useful device functionality can be achieved if these devices can be reinitialized to the all crystalline state after each operation. One possible way of doing this, is by interfacing the device with independent access device at each terminal of interest to clear the amorphous volume independently from the sequential operation.

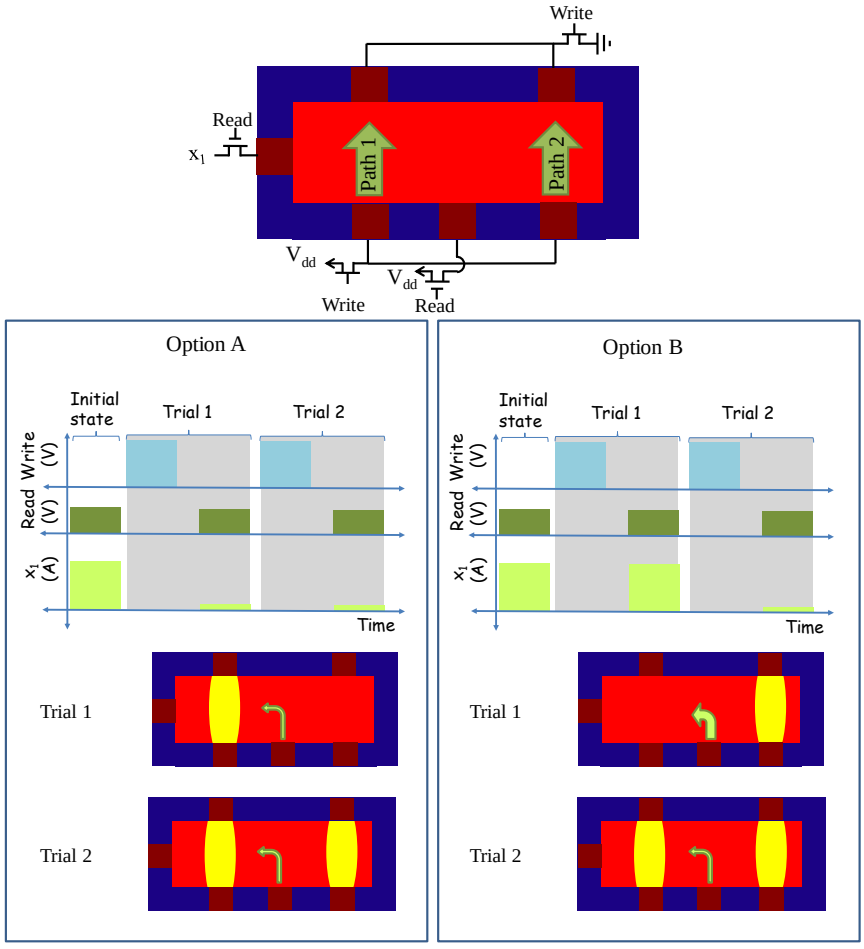


Figure 4-8 An illustration of a onetime one bit random number generator, based on the grain orientation and boundaries, Path 1 and Path 2 will have a random chance of being slightly less resistive and amorphize first. The outcomes of each possible scenario are illustrated as option A and B.

4.1Simultaneous NAND and NOR Operation (PCM-NANOR)

As is shown earlier in this chapter, it is possible to achieve sequential operation in multi-contact phase change device by making use of the thermal runaway. A more sophisticated device that makes a better use of this operation concept is illustrated in Figure 4-9.

The modeled seven-contact device, is capable of achieving a simultaneous NAND and NOR operations for consecutive pulses that are sent to the transistor gate A. The state of the device can be read from the side contacts, where each side represents one logical operation. In this case, reading the device from the left side will give the results for the NAND operation, while the right side read will provide the results for the NOR operation.

Every logic operation is obtained after sending two consecutive pulses through terminal A, a first high pulse V_{GATE} = 2.2 V “logical one” will always result in self-heating the geometrically shorter path and result in amorphizing it only, due to the thermal runaway. The longer path is only amorphized if two high voltage pulses are sent consecutively.

The logic operation results are read by applying low voltage pulses through the middle contact (Read/Erase terminal) and measuring the currents passing through the side logic terminals. A high resistance read, i.e. low current, designates the logic output zero while a low resistance read, i.e. high current, designates the logic output one.

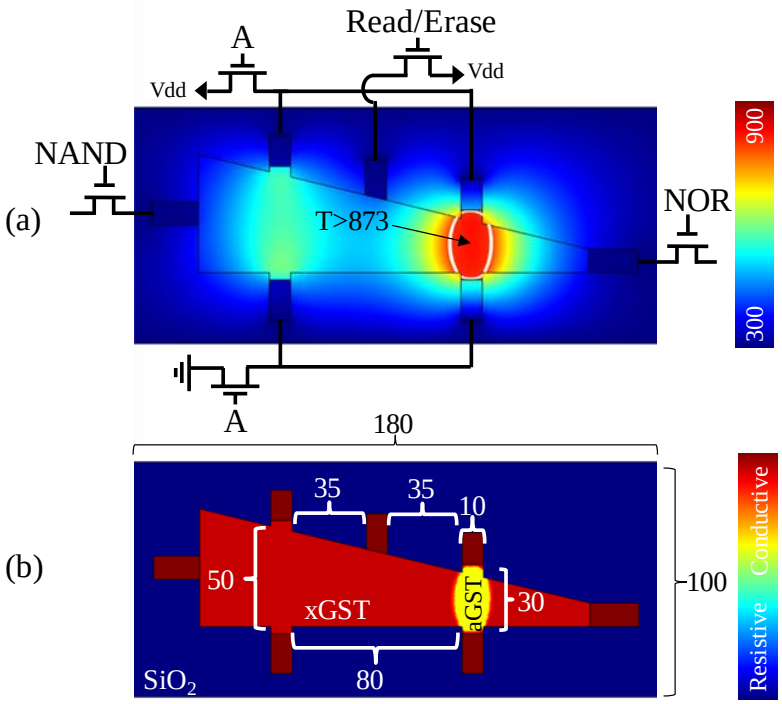


Figure 4-9 Schematics of the modeled phase change NAND and NOR (PCM-NANOR) device with indicated dimensions in nm. (a) Peak thermal profile while applying a high input pulse (V_{GATE} = 2.2 V) that activates the transistor A, the white contour lines denote the boundaries of the melting GST. (b) The resulting conductivity profile after sending the high input pulse showing the amorphized regions in yellow.

Figure 4-10 shows the applied voltage pulses for all possible logic inputs, the applied read voltages and the resulted measured currents as well as the logic truth table for the simultaneous NAND and NOR operation.

Taking case II in Figure 4-10 as an example, sending 1 followed by 0 will only amorphize the region between the shorter contacts (Figure 4-12-case II); The read operation is executed by applying a low voltage pulse to the read transistor (V_{read} = 0.05 V) and applying high voltage pulses (V_{GATE} = 2.2 V) to the side transistor gates and

measuring the output current. For the indicated pulse sequence, high current "Logical 1" will be measured through the NAND terminal and low current "Logical 0" will be measured through the NOR side (Figure 4-10b). The longer path remains intact, in the crystalline state, during and after the indicated pulse sequence, and will only amorphize if the input pulses sequence consisted of two 1's (case-IV in Figure 4-10). The peak thermal profiles as well as the resulted conductivity maps after every pulse and for all the operation cases are shown in Figure 4-12.

The access transistors must be sized properly to satisfy the current and energy requirements for the device operation. For the indicated device dimensions in Figure 4-9, transistors with LxW = 22x130 nm were used to deliver a peak power of ~168 µW to the device terminals.

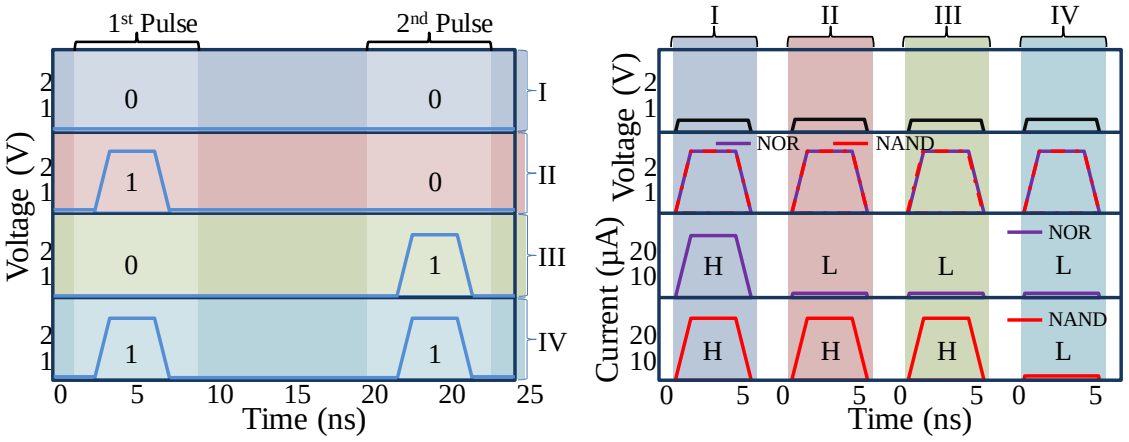


Figure 4-10 (a) The write pulse sequence for all possible logic inputs (cases I-IV), (b) Device read operation showing the applied voltages on the READ and side logic terminals transistors' gates and the measured currents at the output terminals for all possible logic inputs (cases I-IV).

	A (1st pulse)	A (1st pulse)	L. S. Read	R. S. Read
I	0	0	1 (5KΩ)	1 (8KΩ)
II	0	1	1 (5KΩ)	0 (55MΩ)
III	1	0	1 (5KΩ)	0 (55MΩ)
IV	1	1	0 (30MΩ)	0 (55MΩ)
			NAND	NOR

Figure 4-11 The device truth table showing the simultaneous logic results and measured resistances after each logic operation for the left and right sides of the device.

The device must be brought back to the initial all-crystalline state (erased) after every complete logic operation. This can be achieved by sending long erase pulses to the read/erase terminal (V_{Erase} < 1 V) and activating the side NAND and NOR transistors. The erase operation relies on the electric filed breakdown of the formed aGST volumes and crystalline growth mechanism, therefore, it only requires very small amount of current (I_{Erase} = 6.75 µA) to bring GST to the crystalline temperature. In order to ensure the success of the erase operation, the device is erased in two steps one side at a time. The peak thermal profile during the erase operation is shown in Figure 4-13.

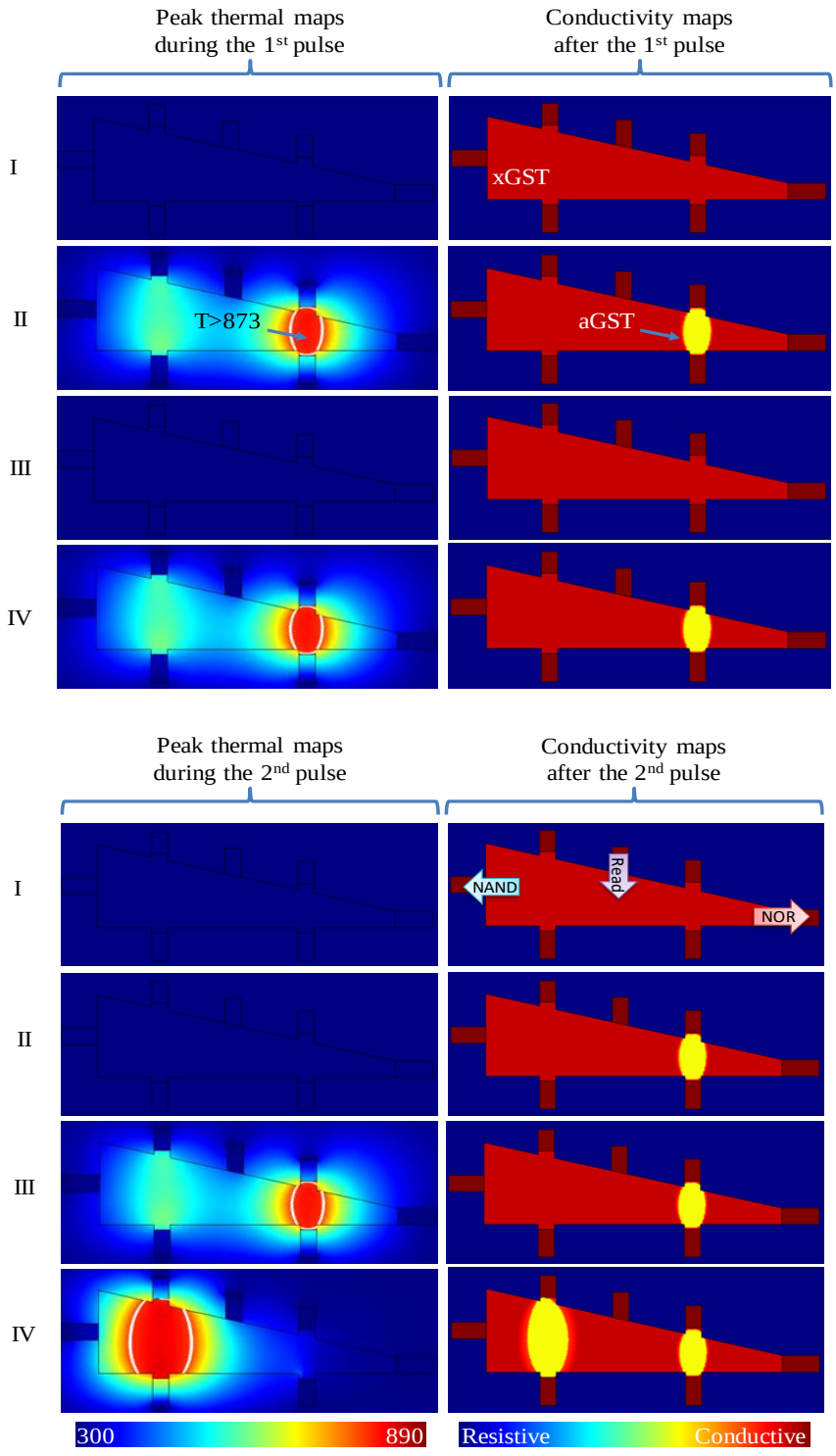


Figure 4-12 The peak thermal profile during the first and second input pulses and the resulted conductivity map after each pulse of the all possible input cases (I-IV) illustrated in Figure 4-10

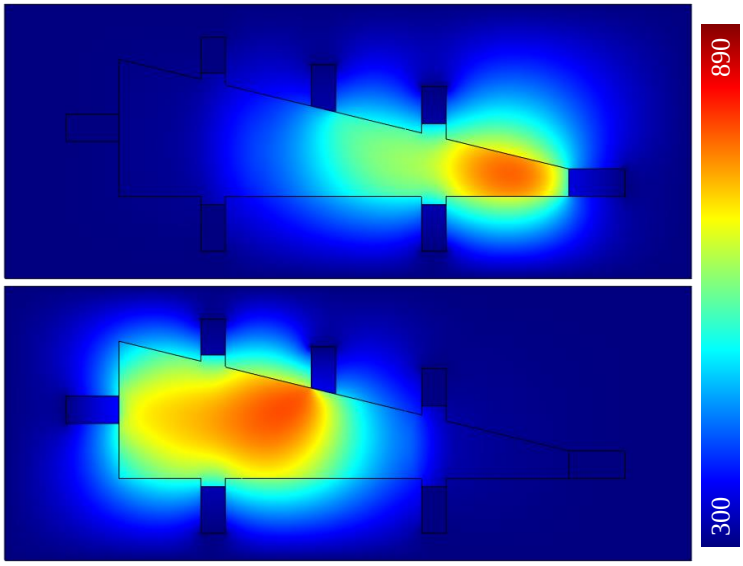


Figure 4-13 Peak thermal profile during the erase operation performed on two steps: for the right side (a) and the left side (b).

The NAND and NOR gates are the universal building blocks in most of the logic circuits, each conventional volatile gate require four transistors (Figure 4-14), eight transistors in total for the combined NAND and NOR operation. This device requires only 5 transistors for the combined operation. In other words, the proposed device offers ~40% real estate reduction with the added feature of nonvolatility. Nonetheless, it must be noted that the conventional gates operate on parallel signals and are almost instantaneous, while the proposed device operates on serial signals. Since the logic operation of the device only depend on the crystalline to amorphous phase transition through melting, its operation be very fast, in the order of 1 ns.

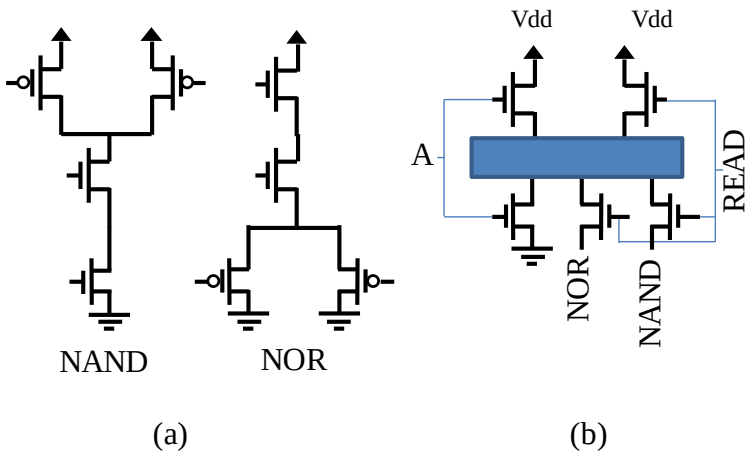


Figure 4-14 Comparison between the schematic of the conventional (a) NAND and NOR and (b) the proposed phase change device showing the footprint reduction advantages in terms of the number of transistors needed by each device.

5. Thermal Crosstalk in multi-contact Phase Change Devices

Phase change memory has proven its scalability across the various technology nodes; the single device operation is proven consistent at any achievable dimension, nonetheless, new concerns have risen due to the thermal crosstalk between neighboring devices in volume production especially below the 54 nm node [58] [59]–[67]. As is mentioned in the earlier chapters, the programming operation of PCM requires the melting of the chalcogenide and for GST that occurs around ($T \approx 900$ K). As the device scaling progresses, the distance as well as the thermal insulation between adjacent devices decreases, hence, neighboring devices start reacting to the generated heat of the cell undergoing a write operation and begin to crystalize in a matter that will affect their data retention [58].

The thermal cross-talk phenomenon has significant impact on the proposed multi-contact devices. The contacts are placed very close to each other without any thermal barriers in between. Referring to the GST-pipe for instance, a amorphzing new paths can end up crystalizing the previously programmed paths due to the close proximity and the thermal interaction. Nonetheless, if the write pulses were designed to be very fast and short (<10 ns), the negative impact of the thermal crosstalk can be constraint to slight deformation of the previously amorphized paths that is also significantly depends on the device dimensions; smaller the device the faster the write pulse has to be.

5.1 The effect of pulse duration and proximity

In order to analyze the effect of the thermal cross talk and the duration of programming pulses, a 4-contact GST patch is simulated. (Figure 5-1); the device is initially programmed by sending a write pulse between contacts A_1 and A_2 and the amorphous path is formed accordingly. Upon the device initialization, the effect of the pulse duration on the crystallization of the formed amorphous path is studied by sending various programming pulses between contacts B_1 and B_2 with different pulse durations.

As expected and can be seen in Figure 5-3, shorter pulse durations <25 ns have a very minimal effect on the adjacent amorphous path. The path A starts to crystalize during slightly longer pulses. In this particular case pulses >90 ns resulted in the roughly the full crystallization of path A.

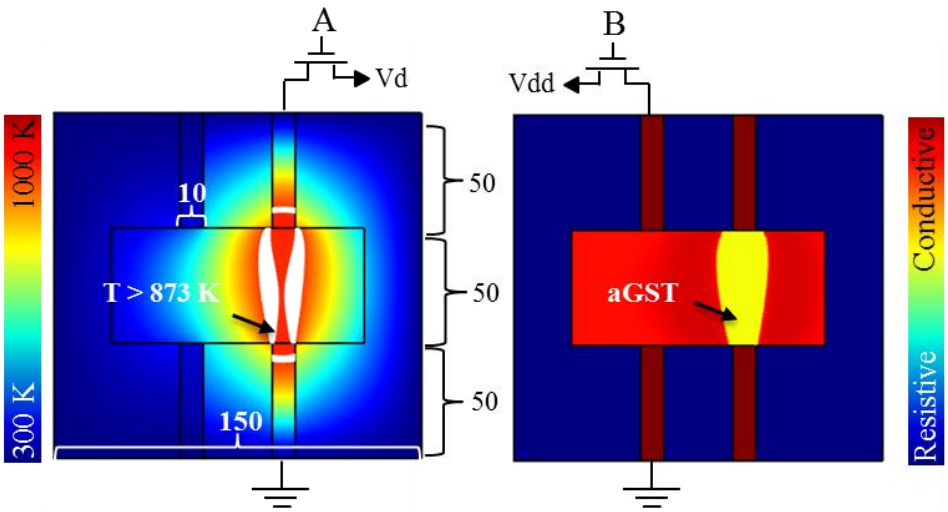


Figure 5-1 Schematic of 4-contact GST patch with dimensions indicated in nm. The peak thermal profile during the device initialization with the molten region surrounded by the white contour lines (left). The resulted conductivity map showing the amorphous volume (right).

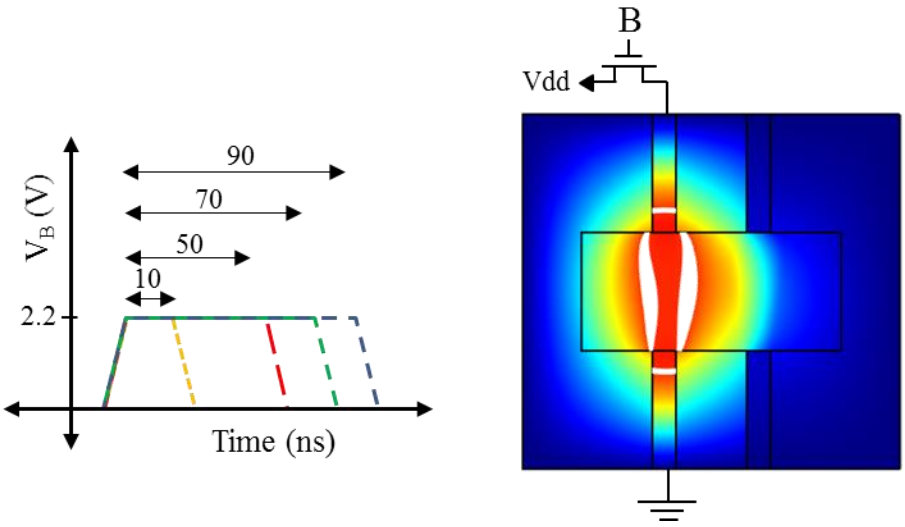


Figure 5-2 Illustration of the applied reset pulses with various pulse widths applied to terminal B. The peak thermal profile during the device initialization with the molten region surrounded by the white contour lines (right).

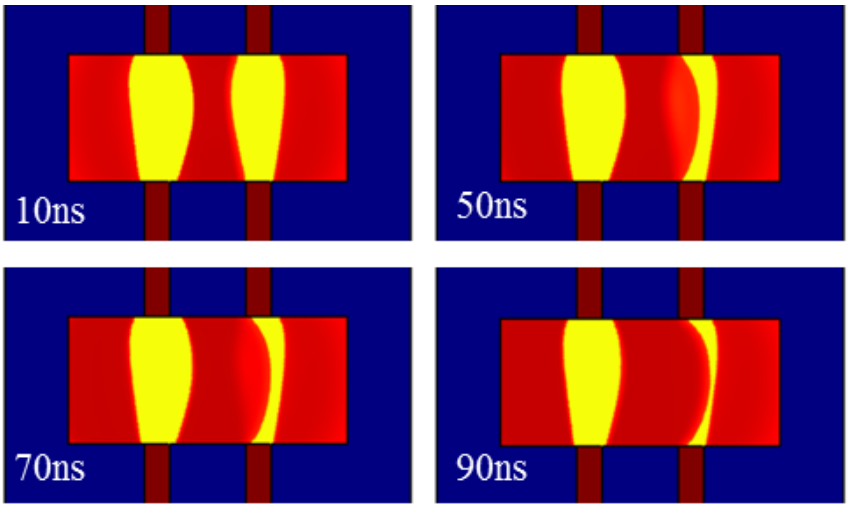


Figure 5-3 The resulted conductivity map after each of the write pulse sent to the B terminal; showing the effect on the neighboring, previously-formed, amorphous volume.

It has to be noted that the results shown in Figure 5-3 are for the indicated device geometry, contact separation and phase change materials, and they are expected to change if any of these factors changed.

5.1 Phase change T-flip flop and Toggle switch

The thermal crosstalk can be employed to achieve an extended functionality of the multi-contact phase change devices. In this subsection, we introduce a six-contact device that is capable of achieving a 2-input (x_1 and x_2), 1-output (y) multiplexing using one control terminal with a total of six contacts (Figure 5-4). Two of the top contacts are electrically shorted and connected to the same access transistor. The output of this device toggles between one input to the other with the application repeated control pulses. The device is interfaced with nFETs at the control (write) terminals and pFETs at the output terminal (read) terminals; this configuration allows the disabling of the read operation while the device is reconfiguring.

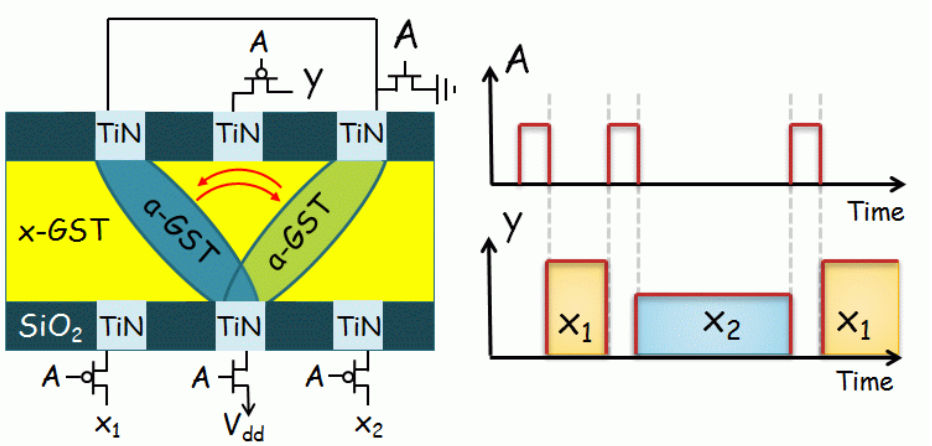


Figure 5-4 A 2-input (x_1, x_2) one output (y) toggle multiplexer using a single control input (A). Only one path is amorphized at a time; during amorphization of the second path, the first one recrystallizes.

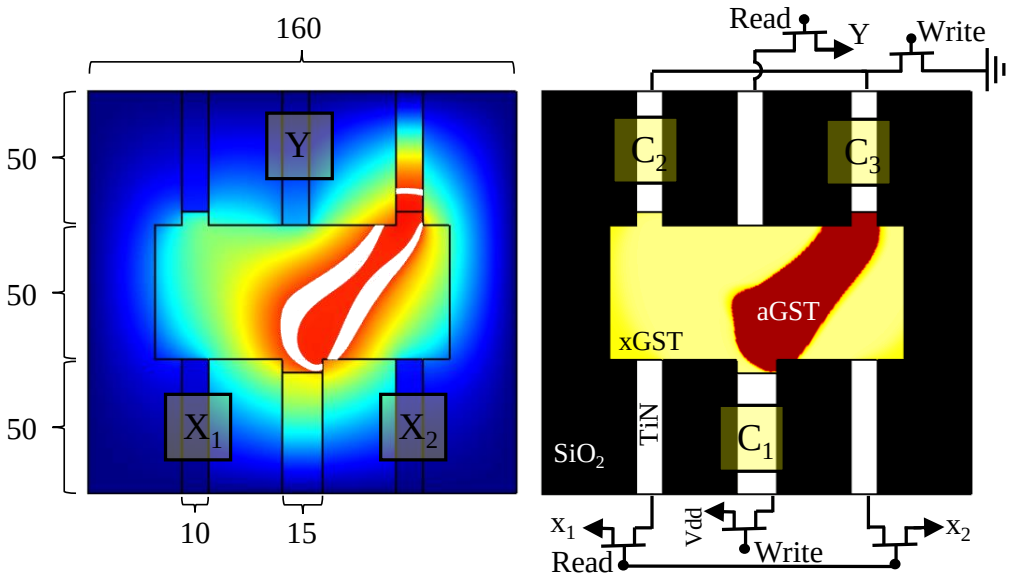


Figure 5-5 Schematics of the modeled phase change toggle with indicated dimensions in n. (left) Peak thermal profile while applying a 3.5 V write pulse that activates the write transistors (right) The resulting conductivity profile after sending the write pulse showing the amorphized region in red.

The operation of the PCM-Toggle is demonstrated through electro-thermal models of $Ge_2Sb_2Te_5$ discussed in the previous chapters, the schematic of the simulated device is illustrated in Figure 5-5.

Starting from a totally crystalline device, when a control pulse is received at the *write* terminal, the two diagonal paths {$C_1 \rightarrow C_2$ and $C_1 \rightarrow C_3$} will start conducting currents. The path with slightly less resistance will attract most of the current and undergo self-heating and melting prior to the other path due to thermal runaway. For this device, the resistance mismatch between the two diagonal paths can occur due to the variation of grain size and grain orientation across the device geometry. In this simulation

study, the resistance mismatch can happen due to the nonuniform meshing across the device geometry.

When the pulse is terminated the molten GST region will amorphize (Figure 5-5). Now any signal applied through the input terminal X_1 can be observed at the output terminal Y, while any signal applied through the input terminal X_2 will be blocked by the highly resistive amorphous strip.

When a second control pulse is received, identical to the first pulse, the device will only have one crystalline path and one amorphous path; the current will flow in the crystalline path resulting in its self-heating and melting, during this process, the previously amorphized regions will recrystallize. As the second pulse is terminated, the molten region will amorphize and the initially amorphous region will become crystalline. After the second pulse, any signal applied through X_2 will be observed through the output terminal while signals through X_1 will be blocked. Accordingly, a toggle operation is achieved.

Figure 5-6 shows the simulation results of successive cycles with consistent behavior. The pulse durations and device geometry have to be designed to assure thermal crosstalk, for the specified device dimensions a 2 V write pulse with 120 ns width is used. Smaller device dimensions and different types of phase change materials may result in a faster operation.

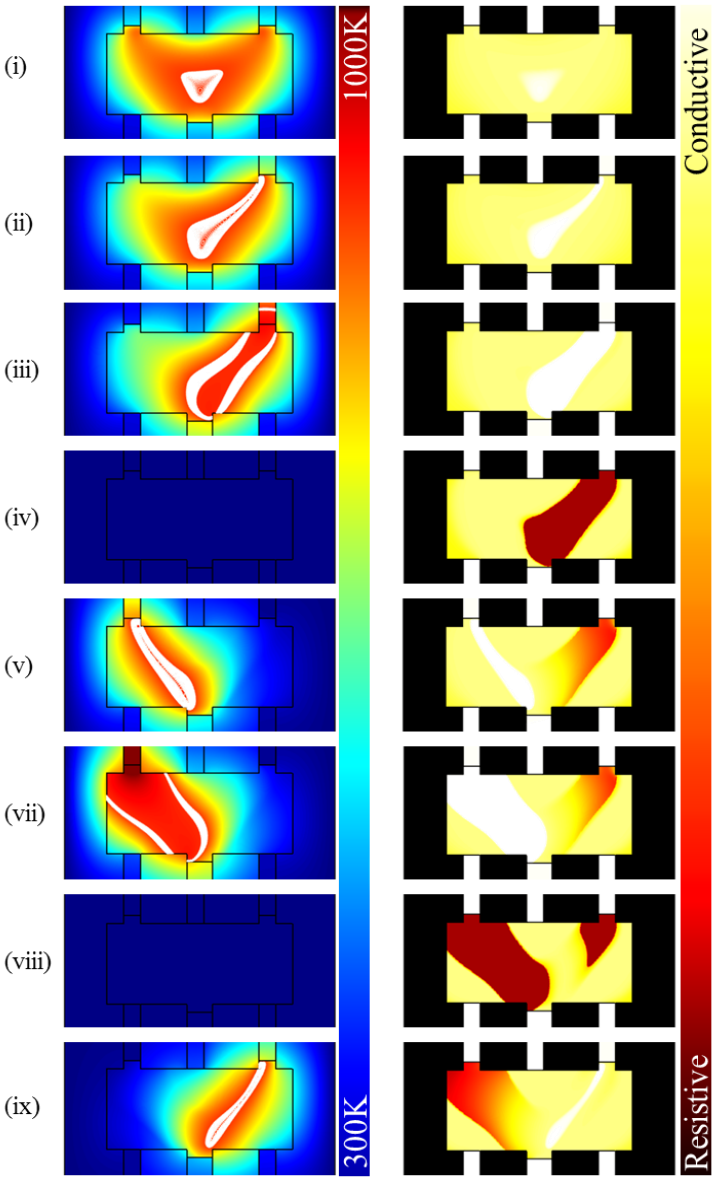


Figure 5-6 Frames from the electro-thermal simulation for the toggle operation showing the thermal profile (left) and the conductivity map (right). The device is initialized in crystalline state and a molten filament is formed between C_1 & C_3, leaving an amorphized region at the end of the pulse after the device cools down (iv) setting the device to $Y = X_1$ state. The next pulse (identical to the first) forms a molten path between C_1 & C_2 and crystallizes the previously amorphized areas. With the termination of this pulse the device is set to $Y = X_2$ state and one cycle of toggle operation is achieved (viii). The cycles continue in the same fashion (ix).

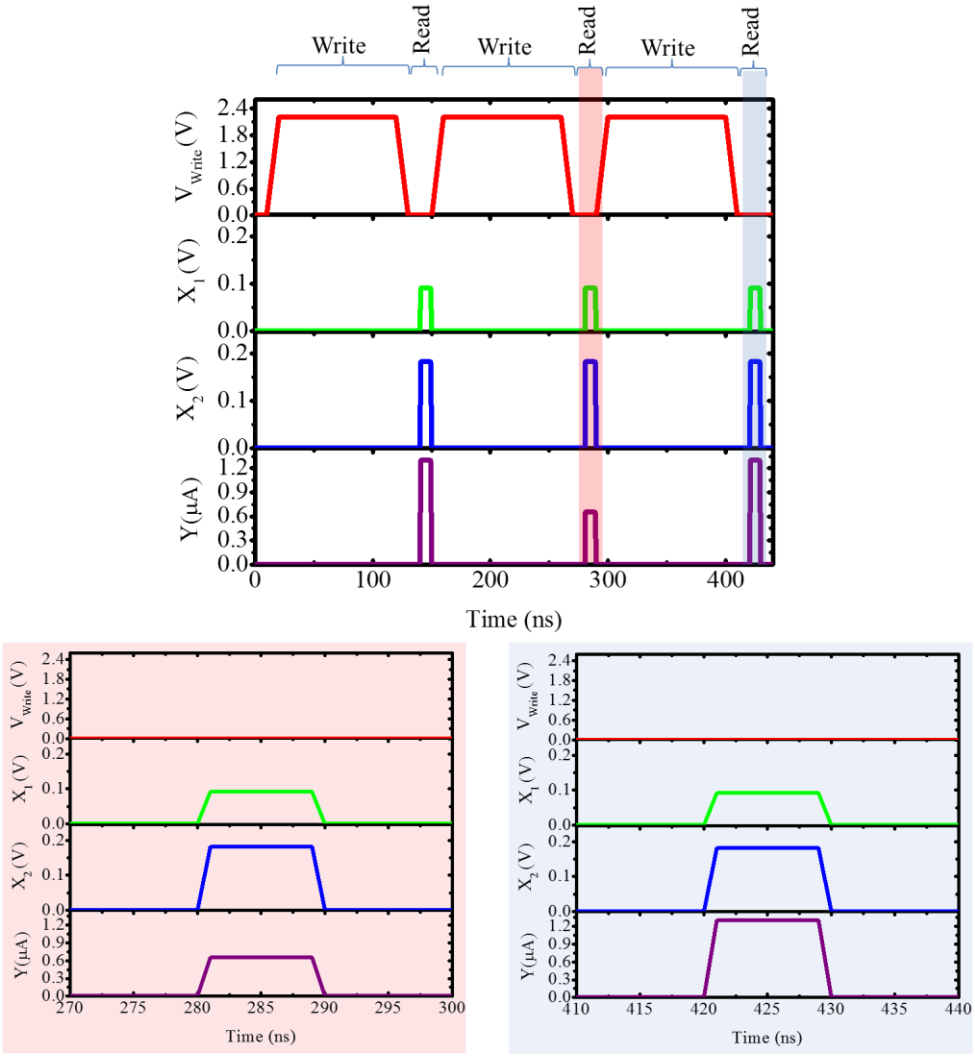


Figure 5-7 The write pulse waveforms the and in the measured read currents resulted after each write operation.

The applied control signals and read operation are illustrated in Figure 5-7; as it can be seen from the figure; the device will pass the signal applied through X_1 and will toggle to the input form X_2 upon the receipt of the consistent control signal. The proposed PCM-Toggle can be fabricated easily with two lithography stages as is shown in Figure 5-8.

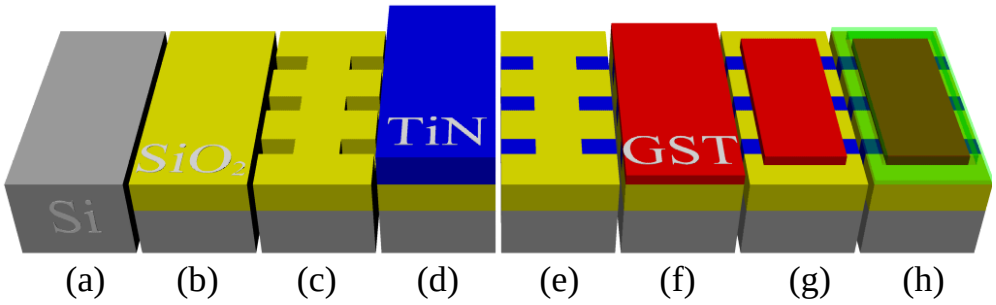


Figure 5-8 Illustration of fabrication processes for 2D-planar patch starting from bulk Si (a): SiO_2 growth for isolation (b), trench formation using photo-lithography and RIE (c), sputter deposition of TiN (d), planarization (e), GST and SiO_2 cap deposition (f), GST patch definition using e-beam lithography and RIE (g), and encapsulation (h).

If the inputs of this device (X_1 and X_2) are implemented with fixed logic "0" and "1", it will operate as T-flip-flop with ~50% less footprint compared to conventional CMOS counterpart and added advantage of non-volatility (Figure 5-9).

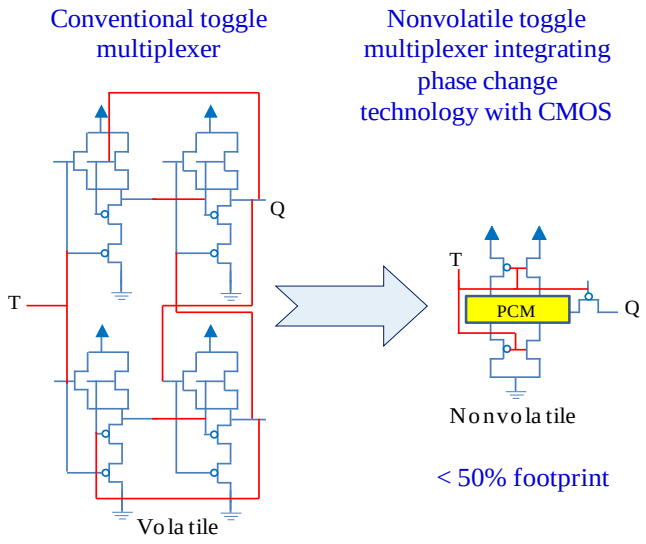
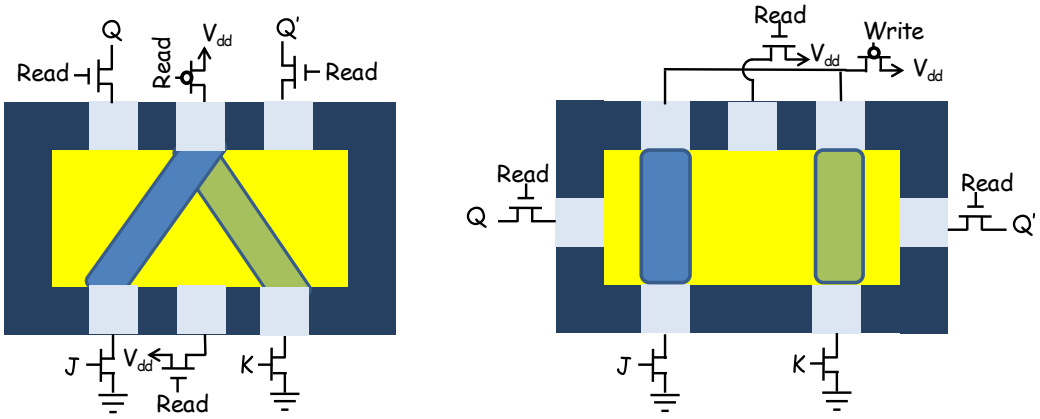


Figure 5-9 Comparison between the schematic of the conventional T-flip flop and the proposed phase change T-flip flop showing the footprint as well as the reduction advantages in terms of the number of transistors needed by each device.

5.2PCM JK-flip flop

A JK flipflop functionality can be achieved from the device presented in the previous subsection, if we modified the transistor interface with the GST patch and added one extra transistor. Similar to the PCM T-flipflop, the device can be implement using a six contact and a seven-contact variant Figure 5-10. The latter variant is simulated in this subsection to illustrate the operation of this device.



(a) (b)

Figure 5-10 (a) Six contact GST patch interfaced with six transistors that can operate as JK flipflop (b) alternative PCM JK flipflop device structure with seven contacts that has the same functionality.

The schematic of the modeled PCM JK flip-flop is shown in Figure 5-11; the device can be operated exactly in a similar way to the conventional, COMS based, JK-flipflop. The logic input pulses are applied to the transistor gates (J and K) and the logic operation results, the device states, (Q and Q') are read from the side contacts. Depending on the activated transistor gate (J or K) and the previous state of the device, an amorphous strip will form, isolating the Q or Q' from the read terminal placed in the middle of the device. This device operation relies on the thermal crosstalk as it requires

the existence of only one amorphous strip after any logic operation. Accordingly, the logic pulses are made long (>50 ns) to insure the successful recrystallization of the previously formed, adjacent amorphous strip.

Figure 5-12 shows the applied voltage pulses for all possible logic inputs, the applied read voltages and the resulted measured currents as well as the device states before and after the logic operation. The truth table for the simulated PCM JK flipflop is shown in Table 5-1. Taking the SET (J =1) operation case II in Figure 5-12 as an example, and starting from the Reset state; applying a high voltage pulse (V_{GATE} = 2.2 V) " Logical 1" at the transistor gate J will lead to selfheating the current path between the bottom and top terminals, respective to the J terminal, resulting in its melting. The generated heat from the SET process will result in crystalizing the previously formed

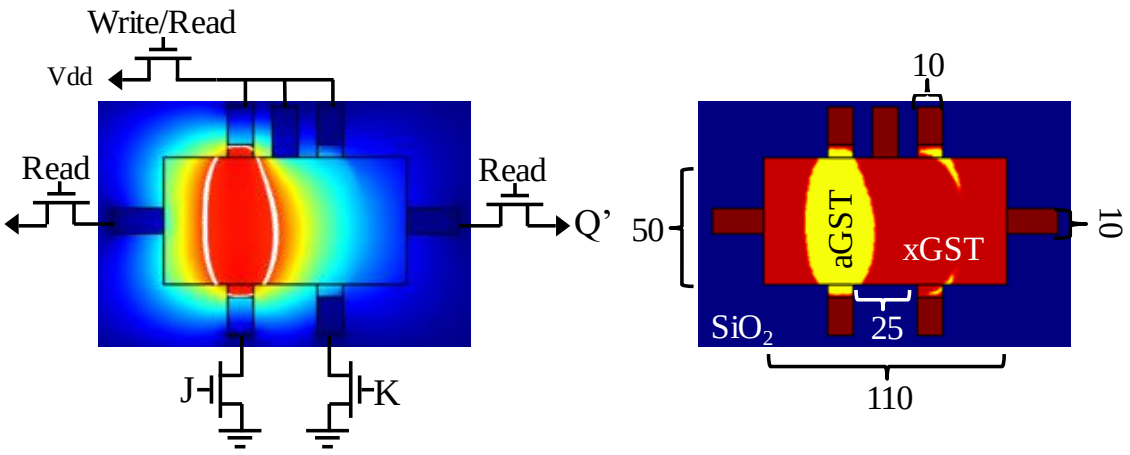


Figure 5-11 Schematics of the modeled phase change JK flipflop device with indicated dimensions in nm. (a) Peak thermal profile while applying a high input pulse (V_{GATE} = 2.2V) that represents a SET operation J = 1, the white contour lines denote the boundaries of the melting GST. (b) The resulting conductivity profile after sending the SET pulse showing the amorphized regions in yellow.

aGST strip isolating Q'. Figure 5-13 illustrates timeframe snapshots of the SET operation, as it can be seen the aGST strip start crystalizing by the generated heat during the SET operation; at t = 60 ns nucleus can be seen forming inside the aGST strip. After the end of the SET pulse the molten strip will cool down and phase transition to aGST and the previous aGST strip will fully crystalize. If the SET pulse was sent to the device while already in the SET state, the device will not heat as the applied voltage is not sufficient to breakdown the existing aGST strip. The device can transition from any previous state to any desired state without the need to erasing it and bringing it back to the all crystalline state.

The read operation is executed by applying a low voltage pulse to the read transistor and measuring the output currents of the Q and Q' terminals. For the indicated

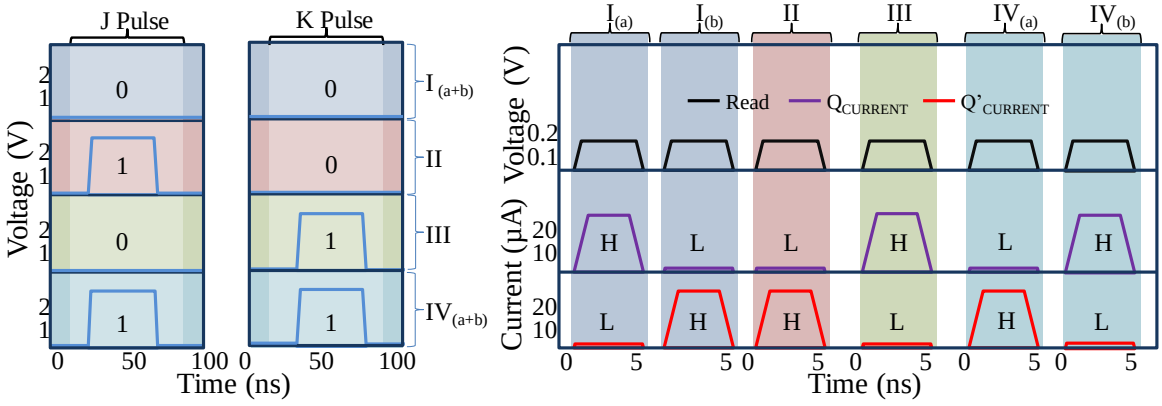


Figure 5-12 (a) The write pulse sequence for all possible logic inputs (cases I-IV), (b) Device read operation showing the applied voltages on the READ and side logic terminals transistors' gates and the measured currents at the output terminals for all possible logic inputs (cases I-IV)

SET pulse above, low current “high resistance” will be measured through the Q terminal and high current “low resistance” will be measured through the Q’ terminal (Figure 5-11).

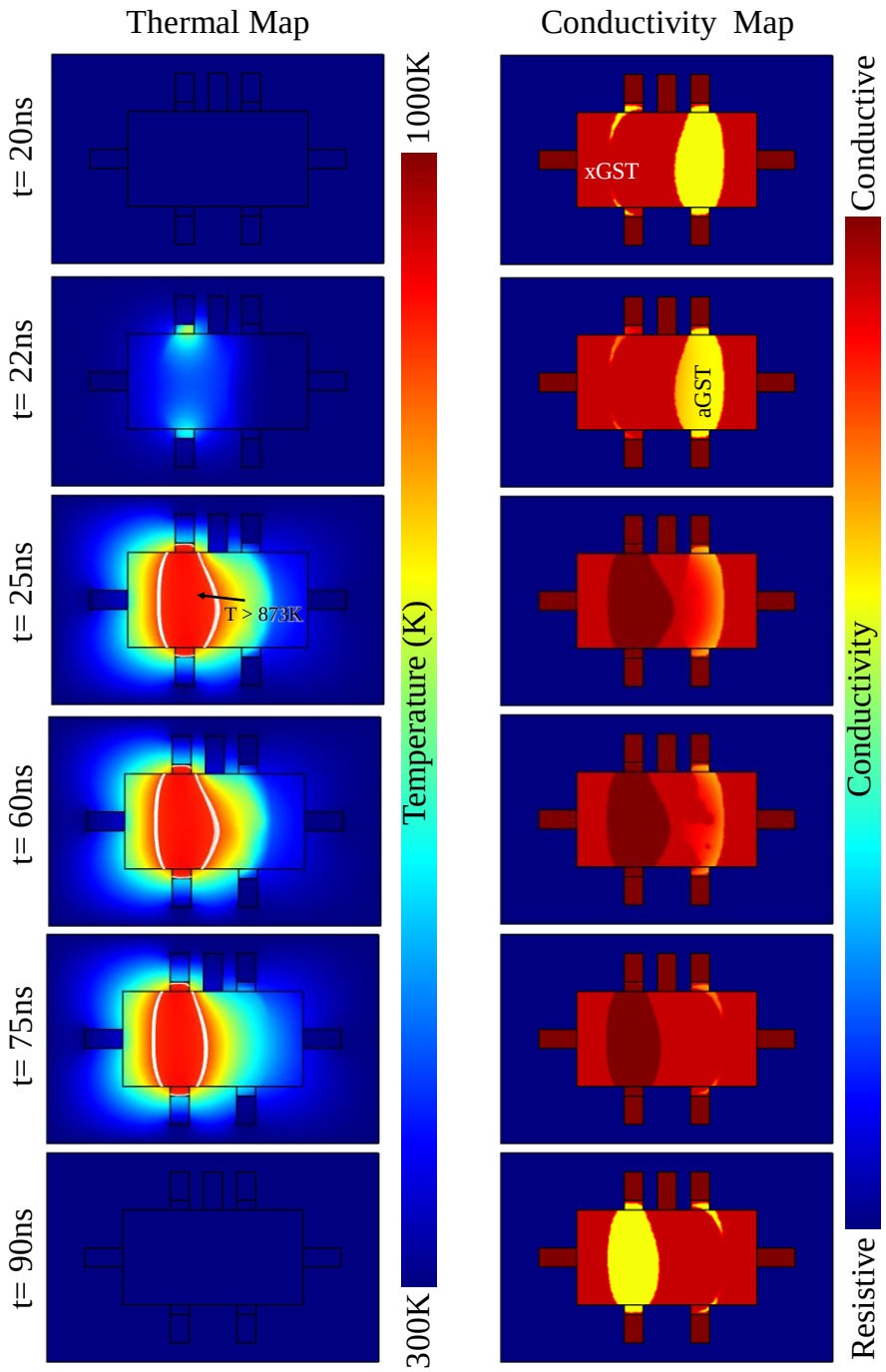


Figure 5-13 Timeframes of the SET process showing (a) The thermal profile during the write process as well as (b) the device conductivity during the same process.

The access transistors must be sized properly to satisfy the current and energy requirements for the device operation. For the indicated device dimensions in Figure 5-11, transistors with LxW = 22x110 nm were used to deliver a peak power of ~168 µW to the device terminals. The current requirement for device operation mainly depend on the type of the phase change material and the device dimensions. Depending on the desired application, alternative phase change materials can be used for reduced power operation.

The JK flipflops are the universal building blocks in most of the sequential logic circuits, each conventional JK flipflop require four logic gates, and sixteen transistors in total. The proposed device here, only requires 6 transistors for its operation, in other words, the proposed device offers ~66% real estate reduction with the added feature of nonvolatility. Nonetheless, it must be noted that the conventional JK flipflops operate on a much faster speed when compared with the PCM flipflop (~10ns depending on the device geometry and phase change material used).

Table 5-1 The device truth table showing the simultaneous logic results and measured resistances after each logic operation for the left and right sides of the device.

$Q^{(t)}$	$Q'^{(t)}$	J	K	$Q^{(t+1)}$	$Q'^{(t+1)}$	Comment
0 (5.5KΩ)	1 (24MΩ)	0	0	0 (5.5KΩ)	1 (24MΩ)	Latch
1 (24MΩ)	0 (5.5KΩ)	0	0	1 (24MΩ)	0 (5.5KΩ)	
0 (5.5KΩ)	1 (24MΩ)	1	0	1 (24MΩ)	0 (5.5KΩ)	SET
1 (24MΩ)	0 (5.5KΩ)	1	0	1 (24MΩ)	0 (5.5KΩ)	
0 (5.5KΩ)	1 (24MΩ)	0	1	0 (5.5KΩ)	1 (24MΩ)	RESET
1 (24MΩ)	0 (5.5KΩ)	0	1	0 (5.5KΩ)	1 (24MΩ)	
0 (5.5KΩ)	1 (24MΩ)	1	1	1 (24MΩ)	0 (5.5KΩ)	Toggle
1 (24MΩ)	0 (5.5KΩ)	1	1	0 (5.5KΩ)	1 (24MΩ)	

5.3 Phase change simultaneous AND & XOR gates and single device half adder.

As is shown earlier, it is possible to achieve toggle operation in multi-contact phase change devices by making use of the thermal crosstalk, also in the previous chapter we have shown that it is possible to achieve sequential operation by utilizing the thermal runaway in geometrically asymmetric structures. In this subsection, we introduce a device that is utilizing both thermal runaway and thermal cross talk to achieve simultaneous logic functionality. The proposed device is very similar to the trapezoidal device presented in Chapter 4 but with different contact spacing to better utilize the

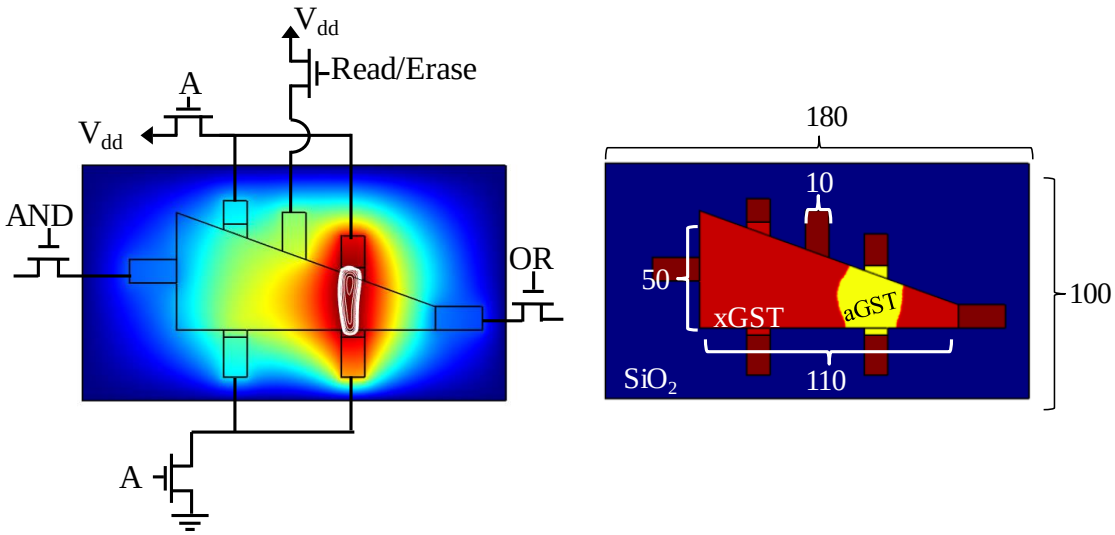


Figure 5-14 Schematics of the modeled phase change XOR and AND (PCM-Half-adder) device with indicated dimensions in nm. (a) Peak thermal profile while applying a high input pulse (V_{GATE} = 2.2 V) that activates the transistor A, the white contour lines denote the boundaries of the melting GST. (b) The resulting conductivity profile after sending the high input pulse showing the amorphized regions in yellow.

thermal crosstalk. The modeled seven-contact device, is capable of achieving a simultaneous XOR and AND operations, hence, a half adder operation, for consecutive pulses that are sent to the transistor gate A.

The state of the device can be read from the side contacts, where each side represents one logical operation. For the presented device, reading the device from the right side will give the results for the XOR operation, while the left side read will provide the results for the AND operation.

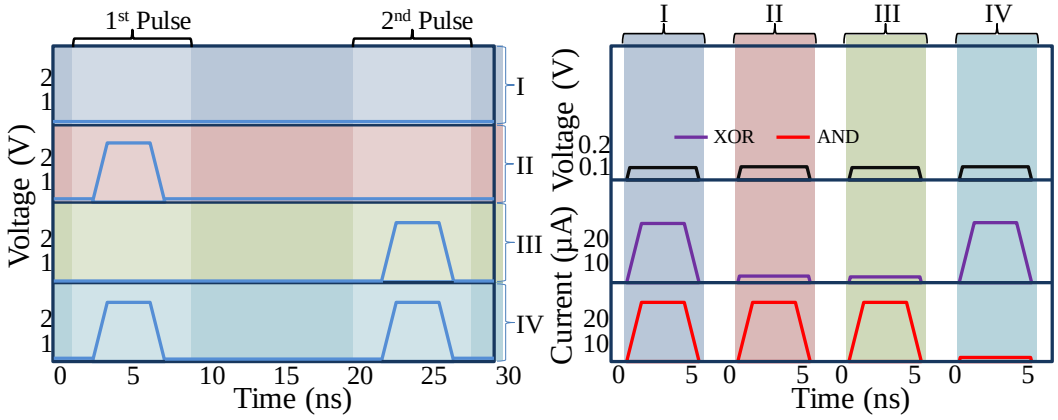
Every logic operation is obtained after sending two consecutive pulses through terminal A, a first high pulse V_{GATE} = 2.2V "logical one" will always result in self-heating the geometrically shorter path and result in amorphizing it only, due to the thermal runaway. The longer path is only amorphized if two high voltage pulses are sent consecutively, when such event happen, the generated heat from amorphizing the longer path will result in crystalizing the short amorphous strip through thermal crosstalk.

The logic operation results are read by applying a low voltage pulse through the middle contact (Read terminal) and measuring the currents passing through the side logic terminals. A high resistance read, i.e. low current, designates the logical *one* result while a low resistance read, i.e. high current, designates the logical *zero* result.

Figure 5-15 shows the applied voltage pulses for all possible logic inputs, the applied read voltage and the resulted measured currents. The logic truth table for the simultaneous XOR and AND operation is shown in Figure 5-16. Taking case VI in Figure 5-15 as an example, sending 1 followed by 1 will amorphize the region between the shorter contacts after the first pulse due to the thermal runaway and then melting the longer path during the second pulse, the generated heat will, in turn, crystalize the shorter

path. The read operation is executed by applying a low voltage pulse to the read transistor (V_{read} = 0.05 V) and measuring the output current. For the two-high pulse sequence, low resistance "Logical zero" will be measured through the XOR terminal and high resistance "Logical 1" will be measured through the AND side. The peak thermal profiles as well as the resulted conductivity maps after every pulse and for all the operation cases are shown in Figure 5-17.

The device must be brought back to the initial all-crystalline state (erased) after every complete logic operation. This can be achieved by sending long erase pulses to the read/erase terminal (V_{Erase} < 1 V) and activating the side AND and XOR transistors. The erase operation relies on the electric filed breakdown of the formed aGST volumes and



(a) (b)

Figure 5-15 (a) The write pulse sequence for all possible logic inputs (cases I-IV), (b) Device read operation showing the applied voltages on the READ and side logic terminals transistors' gates and the measured currents at the output terminals for all possible logic inputs (cases I-IV),

	A (1st pulse)	A (2nd pulse)	L. S. Read	R. S. Read
I	0	0	0 (5KΩ)	0 (8KΩ)
II	0	1	0 (5KΩ)	1 (55MΩ)
III	1	0	0 (5KΩ)	1 (55MΩ)
IV	1	1	1 (30MΩ)	0 (8KΩ)

AND XOR

Carry Addition

Half adder

Figure 5-16 The device truth table showing the simultaneous logic results and measured resistances after each logic operation for the left and right sides of the device.

crystalline growth mechanism, therefore, it only requires very small amount of current ($I_{Erase} \approx 6.75$ μA) to bring GST to the crystalline temperature. In order to ensure the success of the erase operation, the device is erased in two steps, one side at a time, similar to the erase process of the PCM-NANOR device presented previously.

The half adder is of building blocks in most of the logic circuits and an essential component in the Arithmetic Logic Unit (ALU), the conventional volatile half adder is built using two logic gates: XOR and AND, and requires twelve transistors (eight for the XOR gate and 4 for the AND gate) in total. The proposed device here, only requires 5 transistors for the combined operation, in other words, the proposed device offers ~40% real estate reduction with the added feature of nonvolatility. However, the conventional CMOS adder operates on parallel signals and are almost instantaneous, while the proposed device operates on serial signals. A conventional CMOS serial adder a built

from the conventional adder and a D-flipflop and its combined circuit will have 16 transistors, which means that the proposed device offers about 63% of real-estate reduction when compared with a device that offers the same functionality with the added feature of nonvolatility.

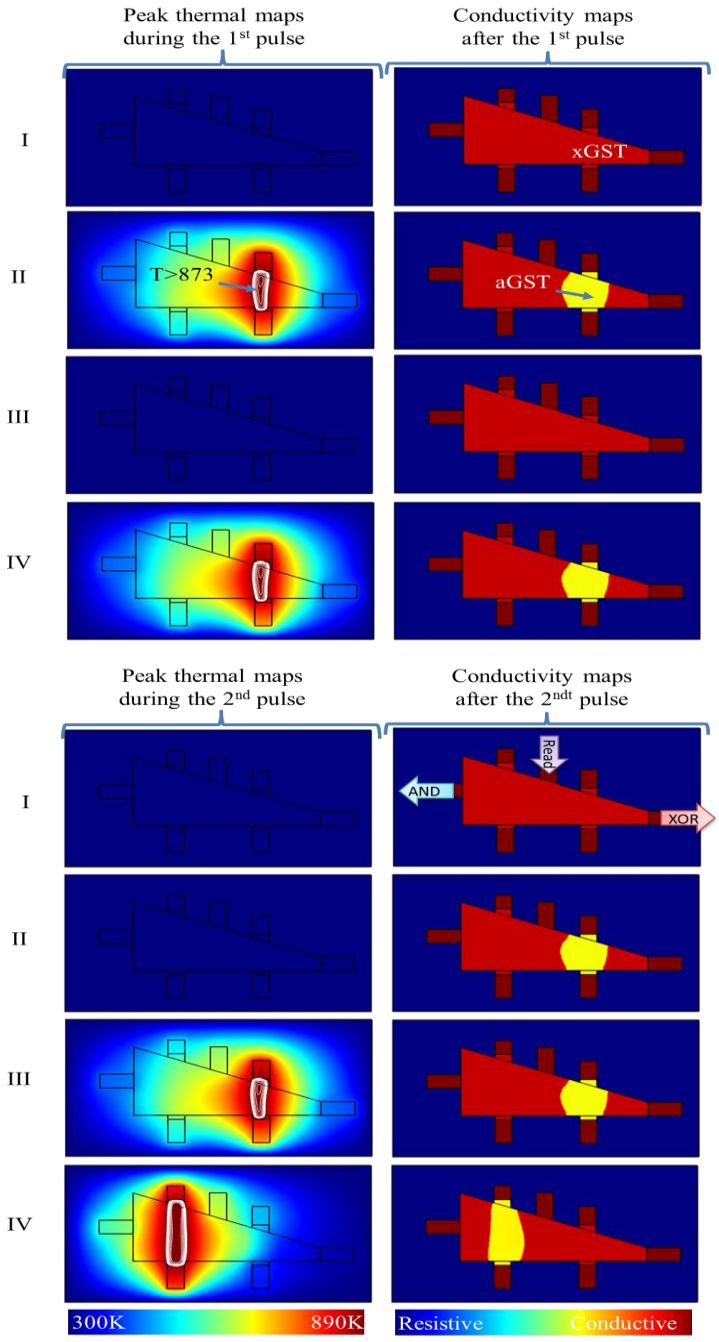


Figure 5-17 the peak thermal profile during the input pulse sequence and the resulted conductivity map after each pulse of the all possible input cases illustrated in Figure 5-15

6. State Machines through Interconnected Multi-Contact Phase Change Devices

6.1 Introduction

In previous chapters, we have shown how it is possible to achieve logic operation in phase change devices employing both the thermal runaway and thermal crosstalk phenomena. In this chapter, we extend the proposed devices functionality by interconnecting devices to each other and make them share the same control pulses.

6.2 Sequential n-bit State Machine

Connecting more than one device in series in a way that they share common control signals will result in a sequential state machine operation with 2^n states, which is usually achieved by flip-flops. The proposed device interconnection concept achieves the state machine operation with less number of transistors and smaller footprint. Plus, the state machines obtained by the proposed device are non-volatile which makes them will suited for low and intermittent power applications.

The simplest state machine utilizing this concept consists of two devices and is illustrated in Figure 6-1. The devices are initialized by amorphizing their shorter paths, here, this state is named the (0) state. The (1) state is defined when the device has the longer path amorphized. Starting from the (0,0) state in Figure 6-1 and activating any transistor (i.e. applying A or B signal) will result in changing the state of the device and transition the device pair to another state. For the indicated devices and illustrated connection, there are three possible states {(0,0), (1,0), (0,1)}.

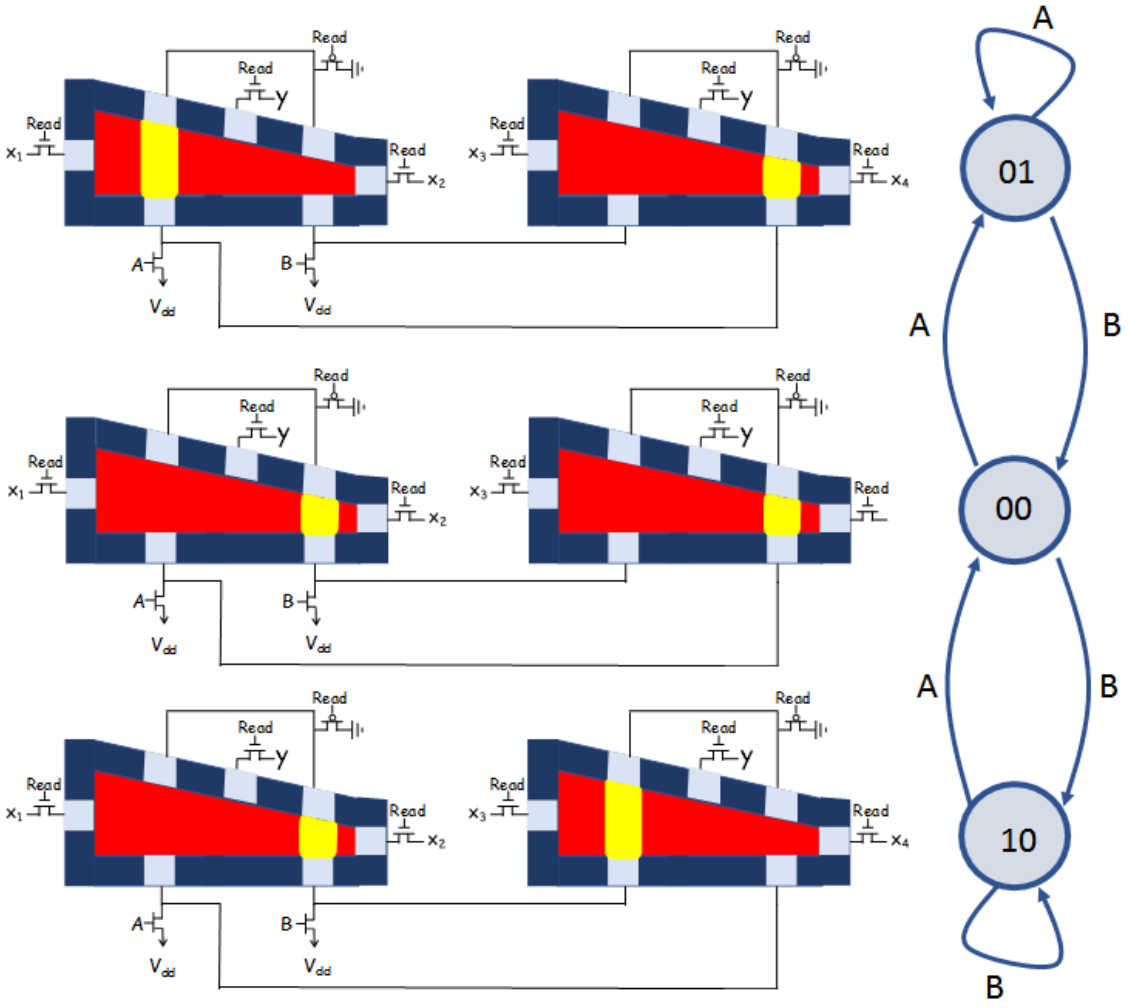


Figure 6-1 A two-device (2 bit) state machine achieved by connecting two devices in with each other. Every control transistor is connected to two terminals in two different devices; transistor B, for instance, is connected to the short terminal of device 1 and the long terminal of device 2.

Based on the sequence at which the transistors are controlled, different state transition will be achieved. Every state has a unique input and output relationship. For instance, for the state (0,0) shown in Figure 6-2 of the above example: the inputs X_1 and X_3 are connected to the outputs Y_1 and Y_3 respectively. Meanwhile, for the state (1,0) the

output of device 1 is connected to the input X_1 terminal and the output terminals of device 2 is connected to the input X_4.

For the cases with the number of devices (n>3), the devices can be linked together forming a ring geometry where the last device is connected back to the first device in the sequence. Figure 6-3 is showing a state machine that is formed using three devices forming a ring.

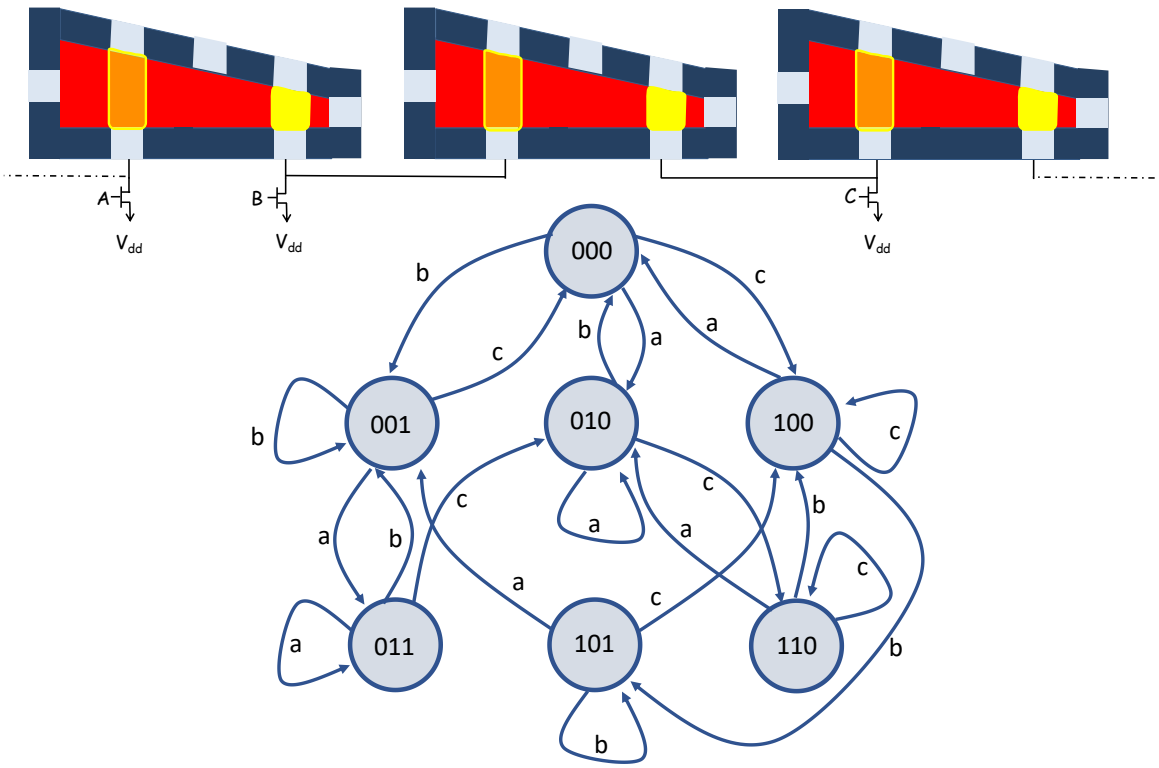


Figure 6-3 n=3 device in a ring configuration forming a state machine of 7 distinct states.

Different states and operation can be achieved for different ways of device connection; for instance, instead of having every control transistor connected to only two devices it can be connected to n devices. Furthermore, the devices may not be needed to form a ring (the last device connected to the first).

7. Conclusion

In this dissertation, a family of multi-contact phase-change devices that are capable of achieving various nonvolatile logic functionalities are proposed. The operation of these devices relies on the novel utilization of linear amorphous strips formations as well as the thermal runaway and thermal crosstalk phenomena that PCM devices experience and are often referred to as challenges that need to be overcome. An international patent application (PCT/US2015/027349) is filed for the novel utilization of these phenomena and the respective device structures.

The operation of the proposed devices is demonstrated through electro-thermal models that self-consistently solve the current continuity, heat transfer and phase field equations in COMSOL Multiphysics. The access transistors are modeled using COMSOL nFET SPICE model. The results show the promising potential of the proposed devices for complementing high-performance VLSI as well as nonvolatile reconfigurable logic.

The formation of linear amorphous strips was utilized to achieve signal routing functionality in two novel device structures. These devices are able to achieve all possible 2x2 routing combinations at a smaller footprint compared with conventional volatile counterparts.

The thermal runaway phenomenon was utilized to achieve sequential operation for geometrically asymmetric devices. A simple onetime trial counter as well as a device that is capable of achieving a simultaneous NAND and NOR functionality was presented; furthermore, a geometrically symmetric device that can be used to produce purely random signature by making use of the random nature of nucleation is also presented.

Thermal crosstalk was employed in novel device structures that operate exactly as the CMOS based JK and T flipflops. Moreover, a simultaneous AND & XOR (hence a single device half adder) was also presented which makes a use of both the thermal crosstalk and the thermal runaway. Additionally, we have showed that an extended functionally can be achieve through the interconnection of the proposed devices and state-machines like operation can be achieved.

When compared to their conventional CMOS counterparts the proposed devices can offer up to 66% area reduction with the added feature of nonvolatility.

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