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Modeling of Multi-State Spatial Wavefunction Switched (SWS) FETs for Logic Gates and Memories

Bander Saman M
University of Connecticut, bander.saman@uconn.edu

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Bander Mahfouz Saman, PhD

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Abstract

This dissertation aims at developing circuit models for complementary (n- and p-channel) Spatial Wavefunction Switched Field-Effect Transistors (SWS-FETs). Unlike conventional FETs, SWS-FETs are comprised of two or more vertically stacked coupled quantum well or quantum dot channels. In SWS-FETs, carriers from one inversion layer is transferred to the other as the gate voltage (Vg) is changed, and the spatial location of carriers within these channels is used to encode the logic states 00, 01, 10 and 11.

The development of n-SWS-FET logic gates and quaternary logic using 20nm FETs is presented. In addition, simulation of a 3-bit flash Analog-to-Digital Converter (ADC) using 180 nm complementary SWS-FETs is presented. The accuracy of the SWS-FET circuits is verified by SWS-FET models in Cadence. The proposed models are based on integration between the Berkeley Short-channel IGFET Model (BSIM4.6) and the Analog Behavioral Model (ABM).

Modeling of SWS-FET lays the groundwork for further investigation of SWS-FET performance of logic functionality. The model is based on integration of Berkeley Short-channel IGFET Model (BSIM) and the analog behavioral model (ABM). The model is suitable to investigate the device configuration and transient analysis at circuit level in Cadence-OrCAD CIS v16.5 simulator.

The SWS-FET model is used to design and simulate digital circuits (logic gates, half adder, differential encoder), memories (D Latch and SRAMs), and analog to digital converter (ADCs),

The transient simulations present to verify the functionality of SWS-FET circuits with logic agreements, all SWS-FET circuits perform the same function as CMOS circuits with less numbers of transistors.

In SWS-FET circuits, the total number of the FETs is reduced by 25% for NAND-NOR and %75 for XOR-XNOR, also the savings are reported as 60% for implementing SRAM cell and 54% for a 3-bit ADC. These reduce cell areas and power dissipations, making SWS-FET a promising circuit element for digital analog applications.

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Bander Mahfouz Saman

B.Sc. in Electrical and Computer Engineering, King Abdul-Aziz University (KAU), Jeddah, Saudi Arabia, 1998

M.Sc. in Quality Management, Arab Academy for Science, Technology & Maritime Transport, Alexandria, Egypt, 2003

M.Sc. in Electrical and Computer Engineering, King Abdul-Aziz University (KAU), Jeddah, Saudi Arabia, 2008

M.Sc. in Electrical and Computer Engineering, University of Connecticut (UCONN), Storrs, Connecticut, USA, 2016

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APPROVAL PAGE

Doctor of Philosophy Dissertation

Modeling of Multi-State Spatial Wavefunction Switched (SWS) FETs for Logic Gates and Memories

Presented by

Bander Mahfouz Saman, B.A., M.A.

Major Advisor

_____

Faquir Jain

Co-Major Advisor

_____

John Chandy

Associate Advisor

_____

John Ayers

Associate Advisor

_____

Lei Wang

Associate Advisor

_____

Evan Heller

University of Connecticut
2017

To my parents
Amnah Bashamrakh and Mahfouz Saman

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1-INTRODUCTION

1.1. Overview and Objectives

The Spatial Wavefunction Switched Field-Effect Transistor (SWS-FET) has two or more vertically stacked Quantum Well/Dot channels. SWS-FET allows the drain current to flow in multiple quantum well channels in a single transistor. The device was first introduced by Jain et al. [1]. The transistor offers conduction in different Quantum Well/Dot channels based on the gate voltage. The change in the gate voltage makes the carriers move from one channel to others. This characteristic is not available in CMOS where conduction take place in one quantum well or wire channel. Furthermore, this feature can be exploited in many digital integrated circuits for multi-bit processing, thus reducing the count of transistors which translates to less die area.

SWS-FETs offers a new opportunity to implement logic gates and memories with fewer transistors than conventional logic gates. Modeling of SWS-FETs lays the groundwork for further investigation of the performance of logic functionality.

The objectives in this research include building dynamic models and designing different digital and analog circuits based on the switching properties of SWS-FETs. Moreover, the model is set as hierarchical block for use in Cadence-OrCAD CIS simulator. This permits investigation of SWS circuits. The overarching goal of this research is to explore SWS-FET circuit applications for various functionality.

1.2. Dissertation Outline

This dissertation research provides three different SWS-FETs models. They are based on integration between Berkeley Short-channel IGFET Model (BSIM) and the analog behavioral model (ABM). Additionally, this research shows the circuit simulations of different SWS-FET applications.

The organization of the dissertation is as follows. Chapter 1 shows the overview and the objectives of the research, and Chapter 2 explains SWS-FETs device structures, and electrical characterizations.

In Chapter 3, SWS-FET models are presented. Chapter 4 describes the novel SWS-FET circuits for universal logic gates, half-adder, differential encoder, memories (D-latch and SRAMs), and analog-to-digital converters (ADCs).

The simulation results and the truth Tables verifications are shown in Chapter 5. Finally, in Chapter 6 a comparison is made with CMOS technology and suggestions for future work are discussed.

2. SPATIAL WAVE SWITCHING FIELD EFFECT TRANSISTOR (SWS-FET)

2-1 SWS-FET Structure

SWS-FET device consists of multiple Quantum Well/Dot channels that allow the electron Wavefunction s switching from one channel to the other as a function of the gate voltage.

SWS-FET can be fabricated in same way as the conventional complementary metal-oxide-semiconductor (CMOS) FETs with modification of CMOS process [1]. The fabrication process of SWS-FET is explained in detail by Jain et al. [1]

Structures of n- and p- SWS-FET with two Si Quantum Well (2-QW) channel, the device has upper Si well (W1) and lower Si well (W2) sandwiched between SiGe barriers as shown in Figure 1. Figure 2A and 2B show n-SWS-FET energy band diagram of Type I heterostructure [2] and Type II heterostructure (strained Si/Si0.5Ge0.5), respectively. The conduction band offsets is equal to $\Delta Ec=Ec_{Si\text{-}well} - Ec_{SiGe\text{-}barrier} =1.04\text{-}0.89 = 0.15eV$ in strained Si/Si0.5Ge0.5 heterostructure.

The structure of 2-QW n-SWS-FET allows carriers (electros) to flow in different channels (Si wells) based on the applied gate voltage (V_{GS}). At a low gate voltage, the lower well has high carrier density while the carrier density in the upper well is smaller. When the gate voltage is increased the upper well has higher carrier density than the lower well. Figure 3 [1] shows the charge-densities simulation in lower well (called last well) and upper well (called first well).

In 2-QW p-SWS-FETs deceive, the carriers (holes) are confined in barriers which makes current flow in different channels (SiGe barriers) based on the applied gate voltage (V_{GS}). At a low magnitude vaule of gate voltage $|V_{GS}|$, the lower barrier has high carrier density while the carrier density in the upper barrier is smaller. When the gate voltage is increased toward negative side the upper well has higher hole density than the lower well.

Figure 4 presents quantum simulations showing the transfer of electron Wavefunction from W2 to W1 as the gate voltage is changed from 0.4 to 1.2 V. Figure 5

shows transfer of holes in a similar manner for gate voltage changed -0.2 to -0.8 V, Tables 1 and 2 give the parameter values used for quantum simulations in Figures 4 and 5 "The data in Figures 4&5, and Table 1 data is provided by Dr. Evan Hellec".

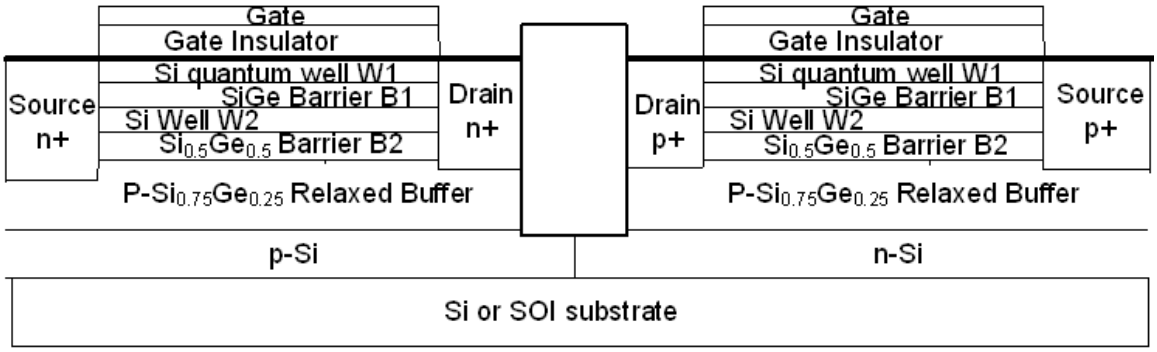


Figure 1. 2-QW n-and p- SWS-FET.

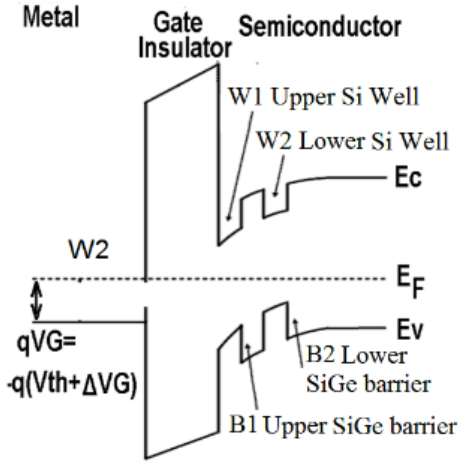


Figure 2A.Type I Heterostructure of n-SWS-FET energy band diagram [2].

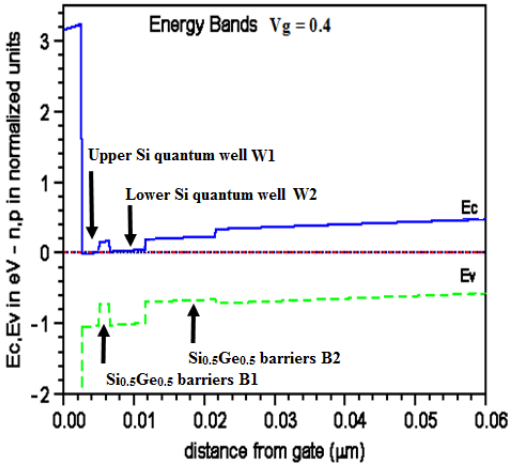


Figure 2B.Type II Heterostructure of n-SWS-FET energy band diagram.

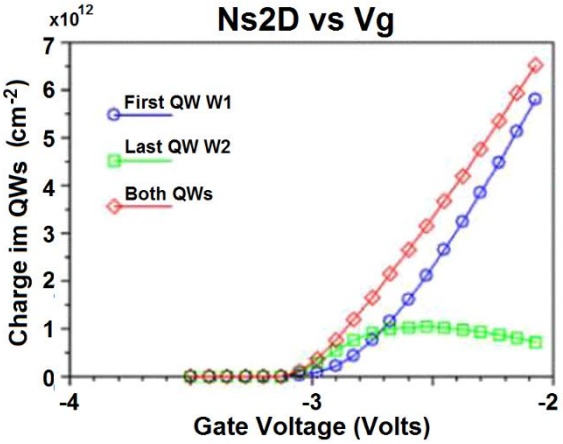


Figure 3. 2-QW n-SWS-FET charge.

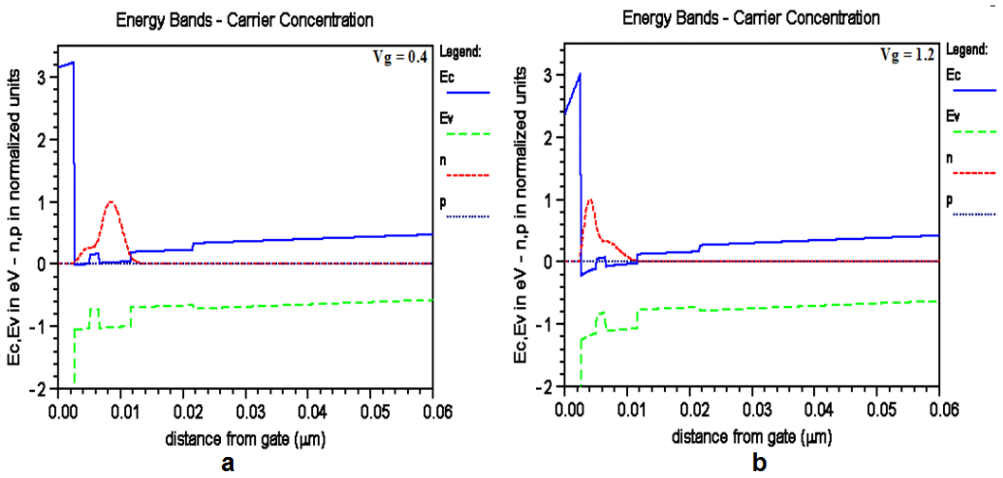


Figure 4. Electron Wavefunction in W2 at 0.4V (a) & W1 at 1.2V (b).

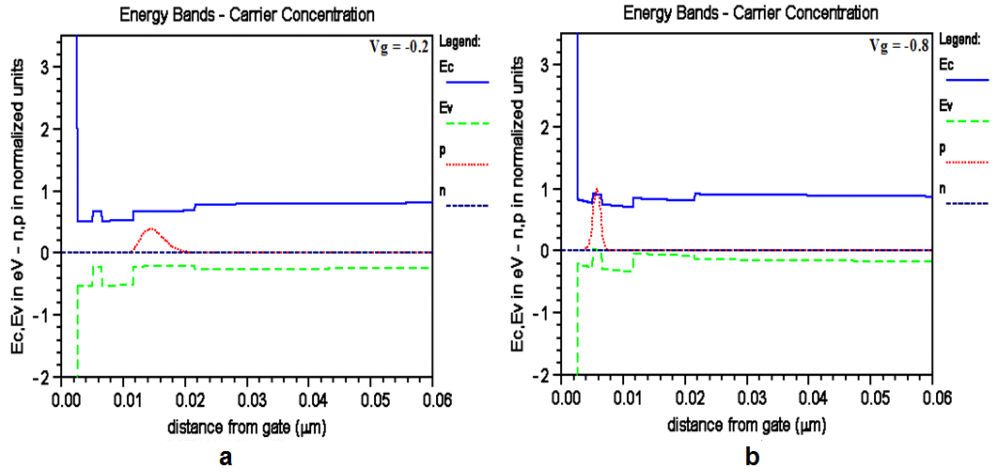


Figure 5. Hole Wavefunction in W2 at -0.2V (a) & W1 at -0.8V (b).

Table 1. Parameters used in the simulation of Wavefunctions for 2-QW SWS-FET

Layer	Thickness nm	χ- nSWS eV	χ- pSWS eV	Eg eV	me	mh	ε_r	N_d cm^{-3}	N_a cm^{-3}
SiO2	2.5	0.9	0.9	9	0.5	0.5	3.9	$0*10^0$	$0*10^0$
Si (QW1)	2.5	3.7	4.15	1.04	0.19	0.49	11.9	$0*10^0$	$0*10^0$
SiGe(.5)	1.5	4.0	4.0	0.89	0.13	0.38	14	$0*10^0$	$0*10^0$
Si (QW2)	5.0	3.7	4.15	1.04	0.19	0.49	11.9	$0*10^0$	$0*10^0$
SiGe(.5)	10	4.0	4.0	0.89	0.13	0.38	14	$0*10^0$	$0*10^0$
SiGe(.75)	50	3.95	3.9	1.05	0.13	0.38	14	$0*10^0$	$1*10^{16}$
Si	100	4.0	3.8	1.1	0.19	0.49	11.9	$0*10^0$	$1*10^{16}$

Where, QWs are tensile strained, χ is electron affinity, Eg the bandgap, me and mh are the electron and hole masses, εr the dielectric constant, N_d and N_a are donor and acceptor concentrations). For n-SWS-FET V_{GS}= 0.4 and 1.2V, p-SWS-FET V_{GS} =-0.2 and -0.8V.

Figure 6A shows 2-QW n-SWS-FET layout (twin drain configuration), where λ is a scale factor and the minimum technology geometry (this is different than the channel length modulation λ parameter). The Minimum n-SWS-FET area is 7λ*5λ. It follows that the area of n-SWS-FET is about same or slightly less than the area of n-MOSFET (4λ*10λ as shown in Figure 6B), this is due to wrap around insulation around lower well drain D2.

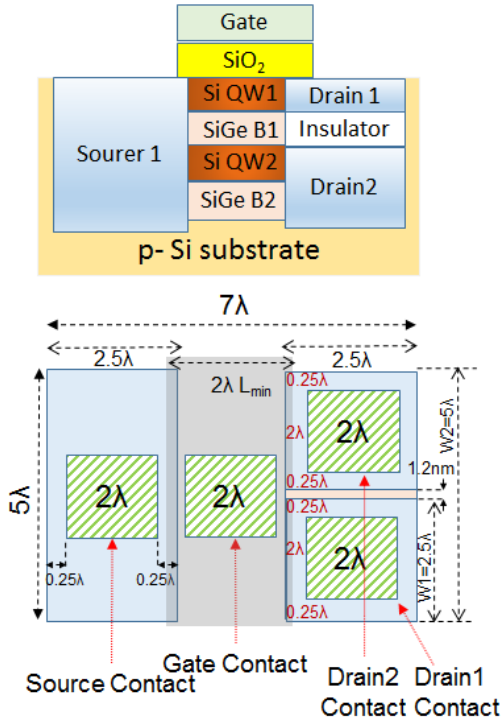


Figure 6A. Twin-drain n-SWS-FET layout.

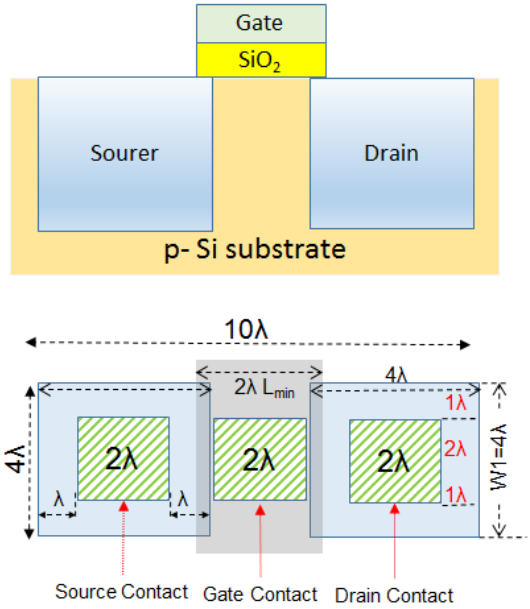


Figure 6B. Conventional n-MOSFET layout.

The three Quantum Well (3-QW) and four (4-QW) channel n-SWS-FET configuration with common source and drain is shown in Figure 7A.

Each channel in QW device has a different threshold voltage that makes the two QW n-SWS-FETs useful in the implementation of binary logic, the four QW n-SWS-FETs are valuable for quaternary logic. In this research, the models of QW SWS-FETs were created to verify the functionality of device in several circuits.

Figure. 7B shows the fabricated SiOx- cladded Si quantum dot n-SWS-FET structure. This device has four QD layers with two drain (D1-deep, D2-shallow). It shows the two lower QD layers conducting to D1 and upper QD layers to D2 [35]. While, Figure 8 presents ID-VD characteristics for gate voltage in the range of 1.8-2.0V whereas upper channel conducts from 2.2-2.4V [35].

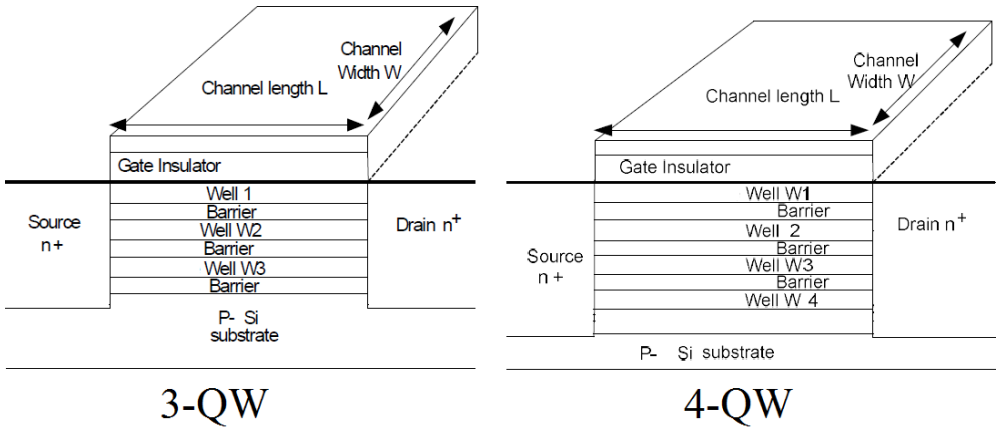


Figure 7A.Three and four QW n- SWS-FET.

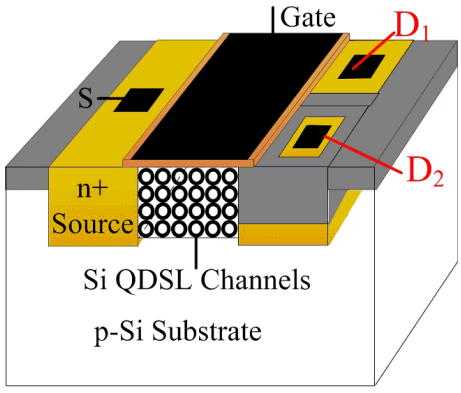


Figure 7B. QD n-SWS-FET.

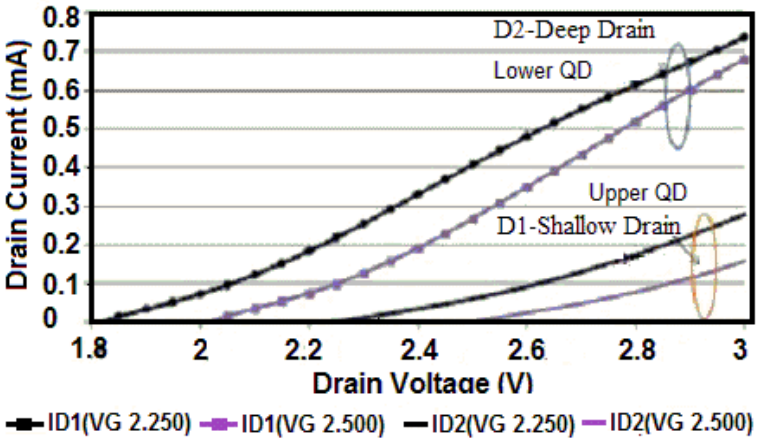


Figure 8. Four QD n-SWS-FET Experimental I_D-V_D

2-2 SWS-FET Theory

In 2-QW n-channel SWS-FET, when the gate to source voltage (V_{GS}) is applied between 0 and threshold voltage of lower well (V_{th2}), both wells W1 & W2 are in off sate and both currents in lower well ($I_{DS\text{-}W2}$) and upper well ($I_{DS\text{-}W1}$) are zero. As the gate voltage is set above V_{th2} the electrons are confined in well W2, resulting in drain current $I_{DS\text{-}W2}$. An increase in V_{GS} greater than the threshold voltage of upper well W1 (V_{th1}), the electrons transfer from W2 to W1, and drain current $I_{DS\text{-}W1}$ flows in W1, and $I_{DS\text{-}W2}$ drops off. At transition voltage (V_{UL}), the W2 is in an off mode [4-6]. The Tables 2, 3, 4 show operation mode of MOSFET, n-SWS-FET, and p-SWS-FET, respectively.

Table 2. The operations mode for MOSFET.

Mode	Cut Off	Saturation	linear
n-MOSFET	$V_{GS} < V_{th}$	$V_{DS} > V_{GS} - V_{th} > 0$	$V_{DS} < V_{GS} - V_{th} < 0$
	$I_{DS} \approx 0$	$I_{DS} > 0$	$I_{DS} >> 0$
p-MOSFET	$V_{GS} > V_{th}$	$V_{DS} < V_{GS} - V_{th} < 0$	$V_{DS} > V_{GS} - V_{th} < 0$
	$I_{SD} \approx 0$	$I_{SD} > 0$	$I_{SD} >> 0$

Table 3. The switching mode for 2-QW n-SWS-FET.

Gate voltage V_G	**$V_{GS} < V_{th2}$**	**$V_{GS} > V_{th2}$** **$V_{GS} < V_{UL}$** **$V_{GS} < V_{th1}$**	**$V_{GS} > V_{th2}$** **$V_{GS} > V_{UL}$** **$V_{GS} > V_{th1}$**	**$V_{GS} >> V_{th2}$** **$V_{GS} >> V_{UL}$** **$V_{GS} >> V_{th1}$**
Well-1	Off mode $I_{DS1} \approx 0$	Off mode $I_{DS1} \approx 0$	On mode $I_{DS1} > 0$	On mode $I_{DS1} >> 0$
Well-2	Off mode $I_{DS2} \approx 0$	On mode $I_{DS2} >> 0$	≈ Off mode $I_{DS2} \rightarrow 0$	Off mode $I_{DS2} \approx 0$

Table 4. The switching mode for 2-QW p-SWS-FET.

Gate voltage V_G	$V_{GS} << V_{th1}$ $V_{GS} << V_{UL}$ $V_{GS} << V_{th2}$	$V_{GS} < V_{th1}$ $V_{GS} < V_{UL}$ $V_{GS} < V_{th2}$	$V_{GS} > V_{th1}$ $V_{GS} > V_{UL}$ $V_{GS} < V_{th2}$	$V_{GS} > V_{th2}$
Well-1	On mode $I_{SD1}>>0$	On mode $I_{SD1}>0$	Off mode $I_{SD1}\approx 0$	Off mode $I_{SD1}\approx 0$
Well-2	Off mode $I_{SD2}\approx 0$	≈ Off mode $I_{SD2}\rightarrow 0$	On mode $I_{SD2}>>0$	Off mode $I_{SD2}\approx 0$

2-2-1 Computing SWS-FET Currents I_{DS1} and I_{DS2}.

In terms of the device switching mechanism, SWS-FETs behaves as a MOSFET. Equation 1 illustrates the drain current for MOSFET, the same equation was developed by Jain et al. [1] for SWSFET. Equation 2 represents the drain current for Well-1 ($I_{DS\text{-}W1}$), which is like the drain current in a regular n-MOSFET transistor. Equation 3 expresses the differential threshold voltage (V_{th2}) for W2. The drain current of W-2 ($I_{DS\text{-}W2}$) is defined in Equation 4, α is the voltage increment for threshold voltage V_{th2} [2-5].

$$I_{DS(Cutoff)} = 0, V_{GS} < V_{TH} \quad \textbf{(1a)}$$

$$I_{DS(Linear)} = \frac{W}{L} C_{OX} * \mu \left((V_{GS} - V_{TH}) - \frac{V_{DS}}{2} \right) V_{DS}, V_{DS} < V_{GS} - V_{TH} > 0 \quad \textbf{(1b)}$$

$$I_{DS(Saturation)} = \frac{W}{L} C_{OX} * \mu \frac{(V_{GS} - V_{TH})^2}{2}, V_{DS} > V_{GS} - V_{TH} > 0 \quad \textbf{(1c)}$$

$$I_{DS\text{-}W1(cutoff)} = 0, VGS1 < Vth1 \quad \textbf{(2a)}$$

$$I_{DS\text{-}W1(Linear)} = \frac{W_{w1}}{L} C_{OX} * \mu \left((V_{GS1} - V_{th1}) - \frac{V_{D1S1}}{2} \right) V_{D1S1}, V_{D1S1} < V_{GS1} - V_{th1} > \quad \textbf{(2a)}$$

$$I_{DS\text{-}W1(Saturation)} = \frac{W_{w1}}{L} C_{OX} * \mu \frac{(V_{GS1} - V_{th1})^2}{2}, V_{D1S1} > V_{GS1} - V_{TH1} > 0 \quad \textbf{(2c)}$$

$$V_{dth2} = \alpha + V_{th2} \quad \textbf{(3)}$$

$$I_{DS\text{-}W2(Cutoff)} = 0, V_{GS2} < V_{dth2} \quad \textbf{(4a)}$$

$$I_{DS\text{-}W2(Linear)} = \frac{W_{w2}}{L} C_{OX} * \mu \left((V_{GS2} - V_{dth2}) - \frac{V_{D2S2}}{2} \right) V_{D2S2}, V_{D2S2} < V_{GS2} - V_{dth2} > 0 \quad \textbf{(4b)}$$

$$I_{DS\text{-}W2(Saturation)} = \frac{W_{w2}}{L} C_{OX} * \mu \frac{(V_{GS2} - V_{dth2})^2}{2}, V_{D2S2} > V_{GS2} - V_{TH2} > 0 \quad \textbf{(4c)}$$

$$\alpha = \begin{cases} \frac{(V_{GS2} - V_{UL}) * (V_{GS2} - V_{UL})}{(V_{th1} - V_{UL})} & \text{When } V_{GS2} > V_{UL} \\ 0 & \text{When } V_{GS2} < V_{UL} \end{cases} \quad \textbf{(5)}$$

Where,

V_{GSx}	Gate-source voltage, x=1 for Well-1 and x=2 for Well-2,
V_{DxSx}	Drain -source voltage, x=1 for Well-1 and x=2 for Well-2,
V_{dth2}	Developed threshold voltage of Well-2,
V_{th2}	Threshold voltage of Well-2,
V_{th1}	Threshold voltage of Well-1,
V_{UL}	Transition voltage at which lower well W2 currents decreased,
α	Matching parameter for lower well W2,

Additional definition:

- C_{ox} is the capacitance per unit area $=\varepsilon_{ox}*\varepsilon_0/t_{ox}$, where ε_0 is the permittivity of the free space, ε_{ox} the relative permittivity of oxide, and t_{ox} the oxide thickness.
- V_{th1} and V_{th2} dependent on the thickness of gate oxide, thickness of wells of barriers, and barriers SiGe composition, for analytical expressions for the threshold voltages in a Si/SiGe/Si MOS structure see reference [34].
- Equation (6) is obtained by substituting V_{dth2} in Equation 3 to Equation 4.

$$I_{DS-W2(Linear)} = \left(\frac{W_2}{L}\right) C_{OX} * \mu \left(([V_{GS2} - \alpha] - V_{th2}) V_{D2S2} - \frac{{V_{D2S2}}^2}{2} \right) \quad \textbf{6}$$

Figure 9 represents I_{DS}-V_{GS} of 2-QW n-SWS-FET obtained from Equations 2-5, the device parameters are shown in Table 5, the modes of operation are shown in Table 6.

Table 5. 2-QW n- and p- SWS-FET 50nm device parameters

Parameter	Unit	n-SWS-FET	p-SWS-FET
V_G	V	From 0 to 1.2	From 0 to 1.2
$V_{DD}= V_{DS}$	V	1.2	-1.2
V_{TH1}	V	0.35	-0.4
V_{UL}	V	0.32	-0.35
V_{TH2}	V	0.18	-0.2
C_{ox}	f/m^2	24.7×10^{-3}	24.7×10^{-3}
U	$m^2/(Vs)$ BSIM4	0.032	0.0095
W1	nm	100	100
W2	nm	250	250

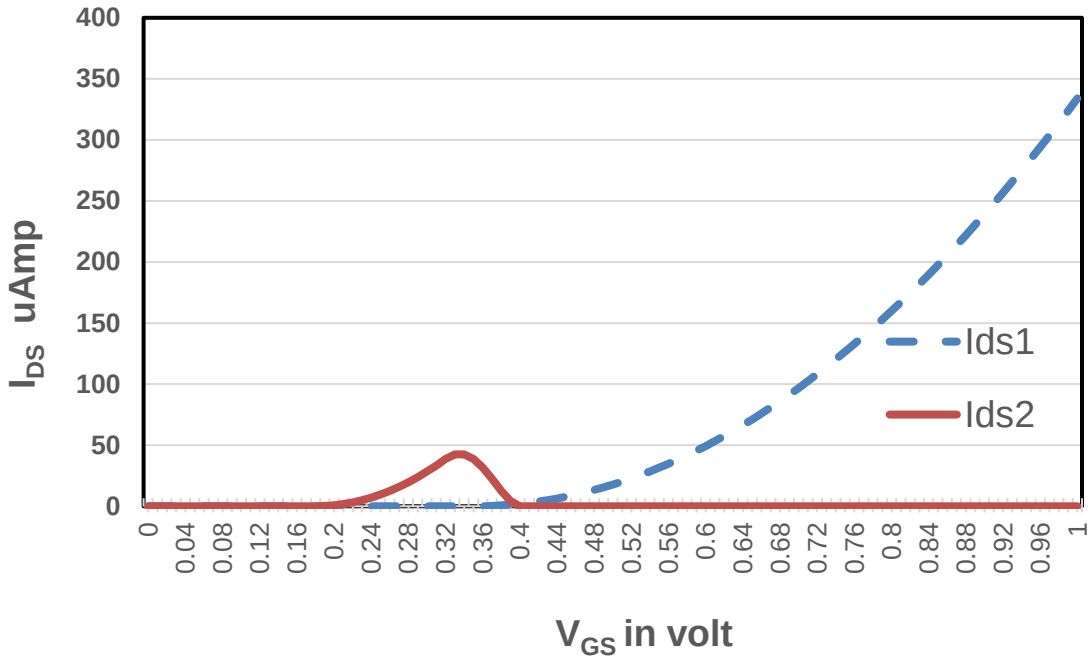


Figure 9. 2-QW n- SWS-FET I_{DS}-V_G for solving Equation 2 and 5.

Table 6. The plot data and switching mode for 2-QW n-SWS-FET

Data	$V_{GS} < V_{th2}=0.18$		$V_{GS}>V_{th2}=0.18$ $V_{GS}<V_{UL}=0.32$ $V_{GS}<V_{th1}=0.35$		$V_G >V_{th2}=0.18$ $V_{GS}>V_{UL}=0.32$ $V_{GS}>V_{th1}=0.35$		$V_{GS}>>V_{th2}=0.18$ $V_G >>V_{UL}=0.32$ $V_{GS}>>V_{th1}=0.35$		
V_{GS} V	0	0.1	0.2	0.3	0.37	0.4	0.5	from 0.6 to 0.9	1.0
I_{DS1} uA	0	0	0	0	0.32	1.98	17.7	from 49.4 to 239.1	333.9
I_{DS2} uA	0	0	0.79	28.4	22.4	0.09	0	0	0
Well-1	Off mode $I_{D1}\approx0$		Off mode $I_{D1}\approx0$		On mode $I_{D1}>0$		On mode $I_{D1}>>0$		
Well-2	Off mode $I_{D2}\approx0$		On mode $I_{D2}>>0$		$\approx$ Off mode $I_{D2}\rightarrow 0$		Off mode $I_{D2}\approx0$		

Figure 10 represents I_{DS}-V_{GS} of 2-QW p-SWS-FET obtained from Equations 2-5, the device parameters are shown in Table 5, the modes of operation are shown in Table 7.

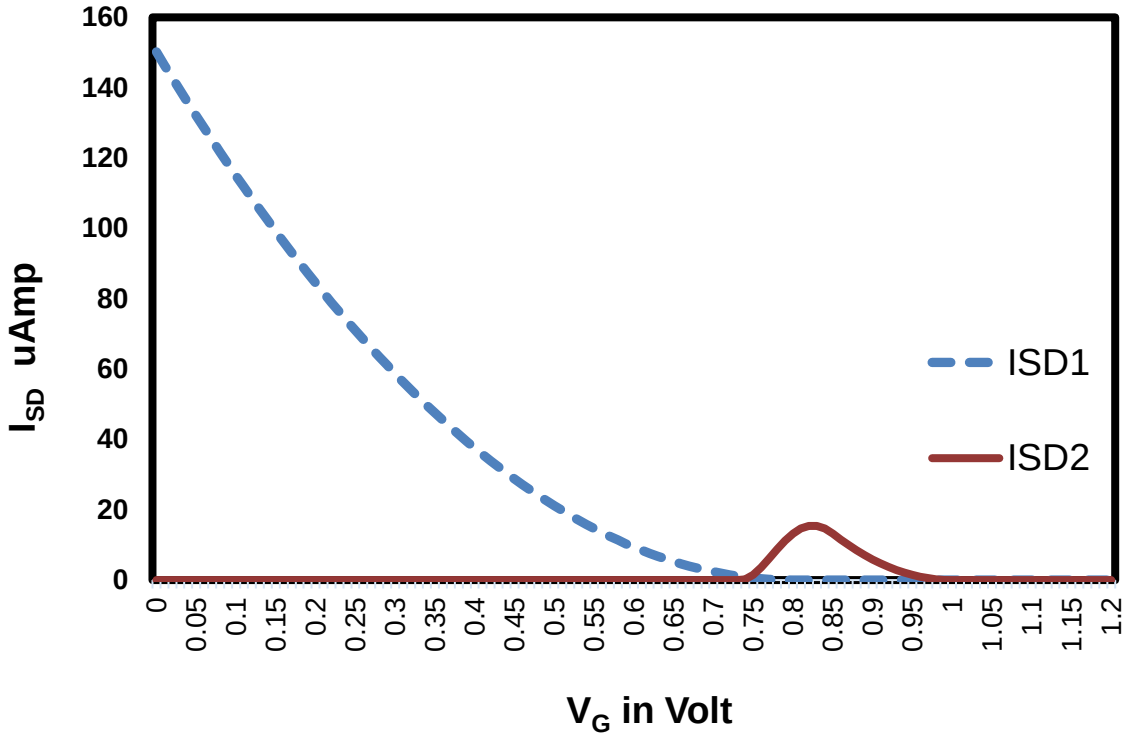


Figure 10. 2-QW p- SWS-FET I_{SD}-V_G for solving Equation 2 and 5

Table 7. The plot data and switching mode for 2-QW p-SWS-FET

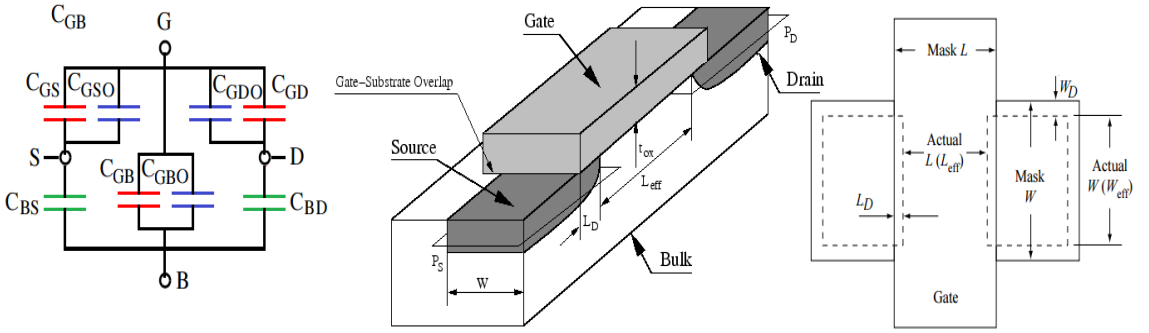
Data	**V_{GS}<<V_{th1}=-0.40 V_{GS}<<V_{UL}=-0.35 V_{GS}<<V_{th2}=-0.20**			**V_{GS}<V_{th1}=-0.40 V_{GS}<V_{UL}=-0.35 V_{GS}<V_{th2}=-0.20**		**V_{GS}>V_{th1}=-0.40 V_{GS}>V_{UL}=-0.35 V_{GS}<V_{th2}=-0.20**		**V_{GS}> V_{th2}=-0.2**	
V_G V	0	from 0.06 to 0.56	0.66	0.76	0.78	0.86	0.96	1.06	1.2
V_{GS} V	-1.2	from -1.14 to -0.64	-0.54	-0.44	-0.42	-0.34	-0.24	-0.14	0
I_{SD1} uA	150	128 to 13	4.60	0.38	0.09	0	0	0	0
I_{SD2} uA	0	0	0	3.57	8.73	11.50	0.94	0	0
Well-1	On mode I_{SD1}>>0			On mode I_{SD1}>0		Off mode I_{SD1}≈0		Off mode I_{SD1}≈0	
Well-2	Off mode I_{SD2}≈0			≈ Off mode I_{SD2}→ 0		On mode I_{SD2}>>0		Off mode I_{SD2}≈0	

2-2-3 SWS-FET Capacitances: C_G, C_S, and C_D.

It is well known that MOSFET has three regions of operation accumulation, depletion, and inversion. The accumulation happens when majority carriers accumulate of

at the surface, the depletion in which the surface is empty of any carriers leaving only a space charge or depletion layer, and the inversion occurs when the surface has the inverted charge. The two voltages that separate the three regions are Flat-band Voltage (V_{FB}) and Threshold Voltage (V_{TH}). Gate voltage below V_{FB} defines accumulation region and voltage above V_{FB} defines the depletion, V_{TH} makes onset of the inversion region.

For capacitance modeling, MOSFET's capacitances depend on the regions of operation. The capacitances are represented by nonlinear gate capacitors (C_{GB}, C_{GS}, C_{GD}), overlap capacitances (C_{GBO}, C_{GSO}, C_{GDO}), and two the junction capacitances (C_{BS}, C_{BD}) as shown in Figure 11. The overlap and junction capacitances are calculated from source and drain perimeters and area. Capacitances are shown in Equations 7 to 11.



L_{eff} :Effective channel length. | W_{eff} : Effective channel width. | A_S : Source diffusion area. | P_S :Source junction perimeter.
L_D :Lateral diffusion length. | W_D : Lateral diffusion width. | A_D: Drain diffusion area. | P_D:Drain junction perimeter.

Figure 11. n-MOSFET capacitors

$$C_{GBO} = Cox * L_{eff}\text{ ,where } L_{eff}=L-2*L_D \quad \textbf{(7)}$$

$$C_{GSO} = Cox * W_{eff} \quad \textbf{(8)}$$

$$C_{GDO} = Cox * W_{eff} \quad \textbf{(9)}$$

$$C_{SB} = \frac{C_J * AS}{(1+V_{SB}/PB)^{MJ}} + \frac{C_{JSW} * PS}{(1+V_{SB}/PB)^{MJSW}}, \quad \textbf{(10)}$$

$$C_{DB} = \frac{C_J * AD}{(1+V_{DB}/PB)^{MJ}} + \frac{C_{JSW} * PD}{(1+V_{DB}/PB)^{MJSW}} \text{ where} \quad \textbf{(11)}$$

Where, V_{SB} is source to body bias, V_{DB} is drain to body bias

Table 8 provides typical values for the model parameters of 1 µm, 0.5 µm, 50 nm, 20 nm channel CMOS technologies.

Table 8. The model parameters of 1 µm, 0.5 µm, 50 nm, 20 nm CMOS technologies.

Process	Note	L=1 µm		L=0.5 µm		L=50 nm BSIM4		L=20 nm BSIM4.6	
		n-	p-	n-	p-	n-	p-	n-	p-
$\|V_{DS}\|_{max}$ V	Max VDD voltage	5	5	3.3	3.3	1.2	1.2	1	1
T_{OX} nm	Oxide thickness	20	20	9.5	9.5	1.4	1.4	1	1
U $cm^2/V{\cdot}s$	Electron mobility	650	250	420	130	320	95	320	95
Na cm^{-3} $x10^{17}$	Substrate doping	1	0.6	1.4	1	8.2	2.4	12	4
Gamma γ $V^{1/2}$	Body-effect parameter	1.05	0.817	0.59	0.51	0.211	0.114	0.183	0.105
PHI $2\varphi_f$ V	Surface potential	0.82	0.79	0.83	0.82	0.92	0.86	0.94	0.89
V_{TO} V	V_{TH} at V_{SB}=0	0.858	-0.96	0.71	−0.92	0.25	-0.22	0.2	-0.12
VFB V	Flat-band voltage	-0.91	-2.47	-0.66	-2.18	-0.88	-1.19	-0.92	-1.11
L_D nm	length diffusion S/D (overlap)	50	50	38	38	1.2	1.2	1	1
W_D nm	Width diffusion	81	81	20.3	20.3	5	5	5	5
Xj nm	Junction depth	200	200	150	150	20	20	20	20
J_S uA/m^2	Body-junction reverse saturation current density	0.01	0.01	0.017	0.017	0.1	0.1	0.1	0.1
CJ mF/m^2	Zero bias junction capacitance	0.32	0.321	0.423	0.423	0.5	0.5	0.5	0.5
MJ	Grading coefficient for area	0.64	0.64	0.6	0.6	0.5	0.5	0.5	0.5
CJSW nF/m	Body-junction capacitance	0.25	0.25	0.38	0.38	0.5	0.5	0.5	0.5
MJSW	Body-junction capacitance	0.5	0.5	0.35	0.35	0.33	0.33	0.33	0.33
PB(V_0) V	Body-junction built-in potential	0.757	0.757	0.989	0.989	1	1	1	1
C_{GBO} nF/m	Gate-Body capacitance per unit channel length	0.45	0.45	0.38	0.38	0.025	0.025	0.025	0.025
C_{GDO} nF/m	Gate-Drain capacitance per unit channel width	0.354	0.354	0.3	0.3	0.623	0.623	0.623	0.623
C_{GSO} nF/m	Gat-Source capacitance per unit channel width	0.354	0.354	0.3	0.3	0.623	0.623	0.623	0.623
AS m	Source diffusion area	Length of Source *W = 2*L*W							
AD m	Drain diffusion area	Length of Drain *W = 2*L*W							
PS m	Source junction perimeter	2*(Length of Source) + W = 4*L + W							
PD m	Drain junction perimeter	2*(Length of Source or Drain) + W = 4*L + W							

Where: Gamma $= \gamma = \frac{\sqrt{2\times q\times \varepsilon_{Si}\cdot\varepsilon_0\cdot\times N_a}}{C_{ox}}$

$\mathrm{PHI} = 2\varphi f = 2 * 0.0259 * \ln\frac{N_a}{n_i}$

$V_{TH} = V_{T0} + \gamma * \left(\sqrt{\mathrm{PHI} + V_{SB}} - \sqrt{\mathrm{PHI}}\right)$

$V_{FB} = V_{T0} - \gamma * \sqrt{\mathrm{PHI} + V_{SB}} - \mathrm{PHI}$

The bias-dependent n-MOSFET gate capacitances distribute according to the Meyer model [21-22] as Table 9A.

Table 9A. The Meyer model for the n-MOSFET gate capacitances.

Mode	Accumulation $V_{dsat} < 2\varphi_f$	Depletion $V_{dsat} < 0$	Saturation $V_{dsat} < V_{DS}$	Linear $V_{dsat} > V_{DS}$
C_{GB}	C_{OX}	$C_{OX}\frac{V_{th}-V_{GS}}{\text{PHI}}$	0	0
C_{GS}	0	0	$\frac{2}{3}C_{OX}$	$\frac{2}{3}C_{OX}[1-\left(\frac{V_{GD}-V_{th}}{V_{GS}+V_{GD}-2V_{th}}\right)^2]$
C_{GD}	0	0	0	$\frac{2}{3}C_{OX}[1-\left(\frac{V_{GS}-V_{th}}{V_{GS}+V_{GD}-2V_{th}}\right)^2]$

NOTE: In the linear mode, As V_{GS} increased C_{GS} and C_{GD} become $=0.5C_{ox}$.

Where: V_{dsat} is the drain-source saturation voltage= V_{GS}-V_{th}.

Figure 12 represents gate capacitances (C_{GB}, C_{GS}, and C_{GD}) for the channel length (L) = 1 µm and the gate Width (W) =4 µm n-MOSFET, Figures 13 A, B, and C show the gate capacitances plus overlap capacitances (C_{GBO}, C_{GSO}, and C_{GDO}) for L=1 µm and W=4 µm channel length n-MOSFET. The plot is obtained using the parameters in Table 8 and the formulas in Table 9A.

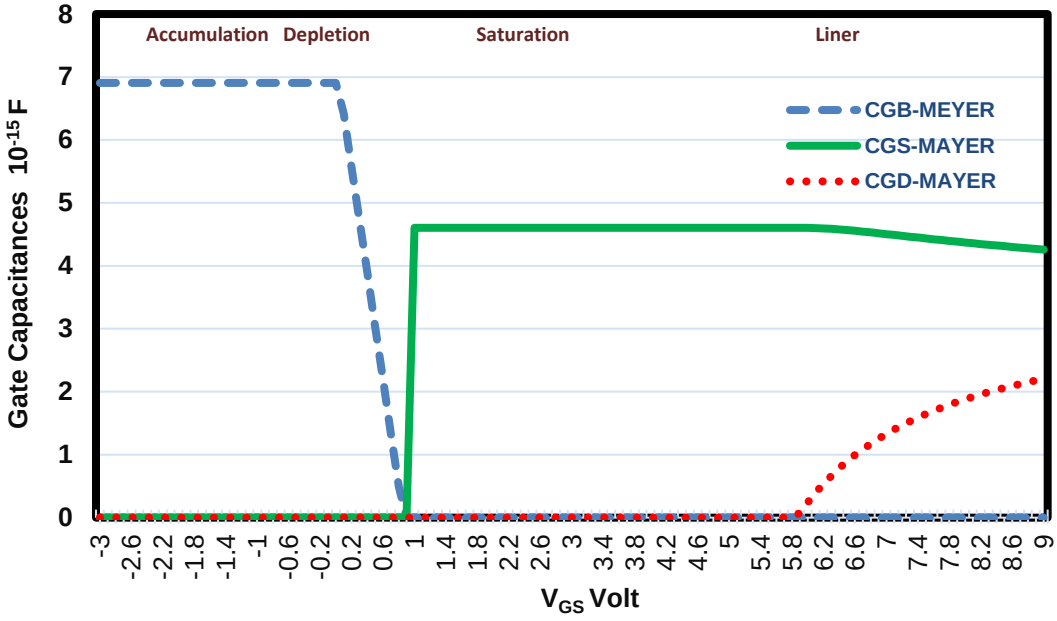


Figure 12. Meyer model for L=1µm n-MOSFET gate capacitances (C_{GB}, C_{GS}, C_{GD}).

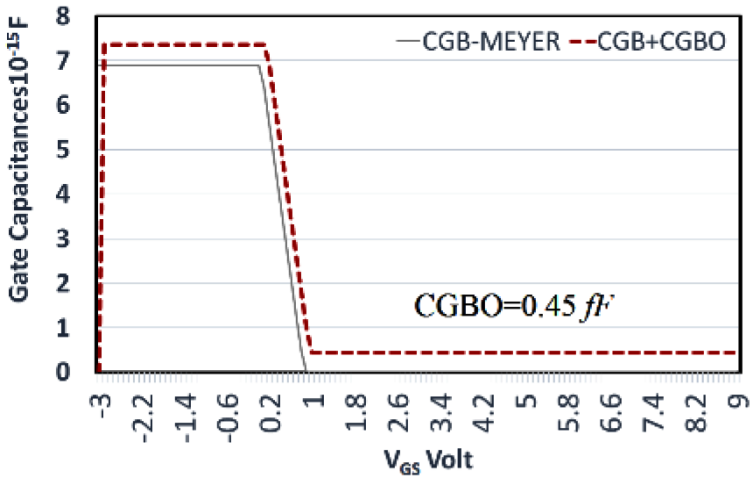


Figure 13A. Meyer model for L=1 µm n-MOSFET for $C_{GB}+C_{GBO0}$.

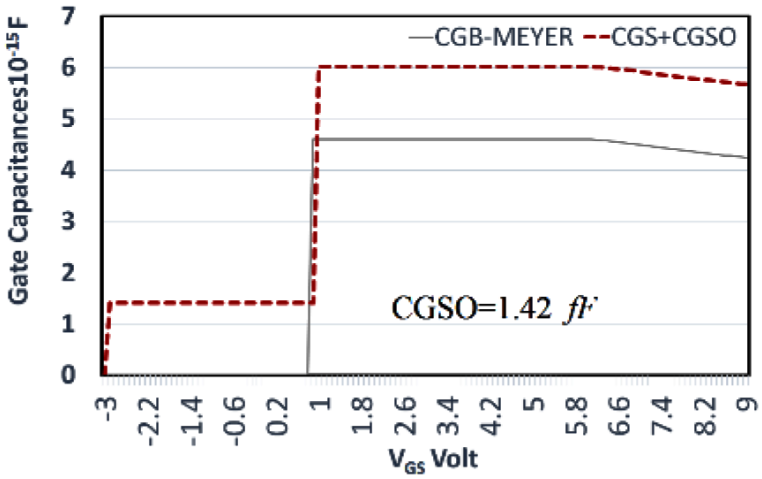


Figure 13B. Meyer model for L=1 µm n-MOSFET $C_{GS}+C_{GSO}$.

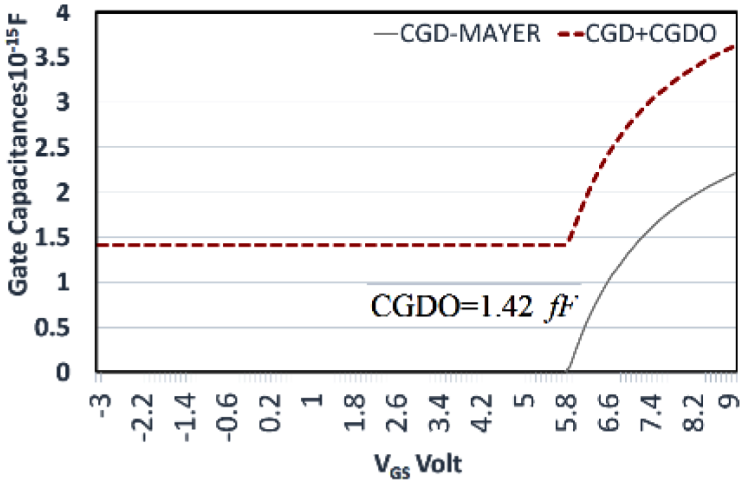


Figure 13C. Meyer model for L=1 µm n-MOSFET for $C_{GD}+C_{GDO}$.

Figure 14 shows all five capacitances (three capacitances for gate plus overlap capacitances, and two junction capacitances) for L=1 µm and W=4 µm n-MOSFET. Similarly, Figures 15 shows the plots of the five capacitances all for L=20 nm and W=80nm n-MOSFET.

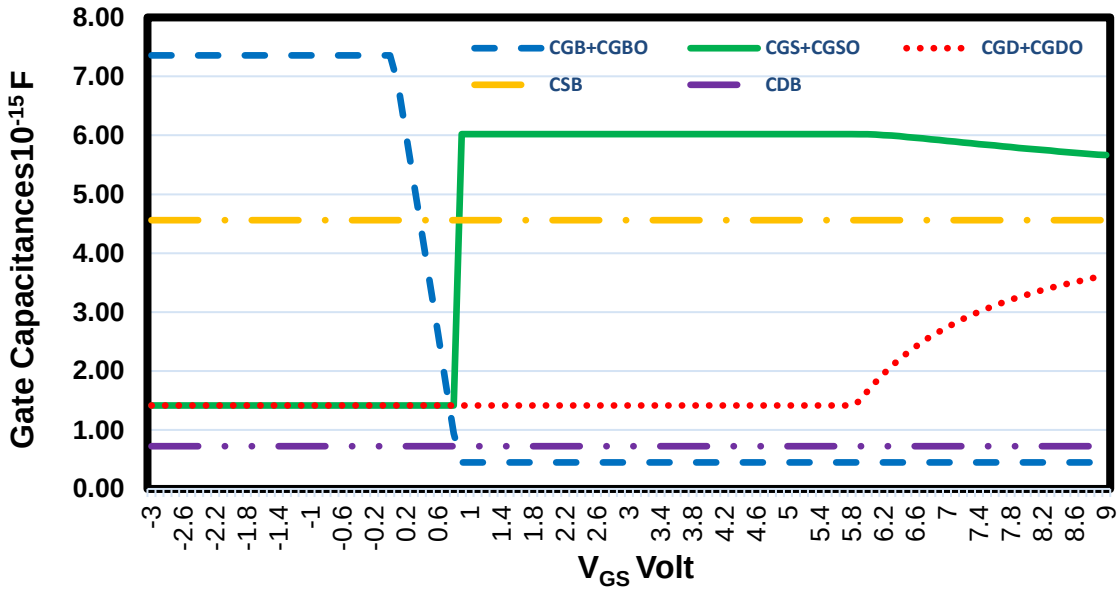


Figure 14. Meyer model for 1 µm n-MOSFET all five capacitances C_{GB}+C_{GBO0}, C_{GS}+C_{GSO}, C_{GD}+C_{GDO}, C_{BS}, and C_{BD}.

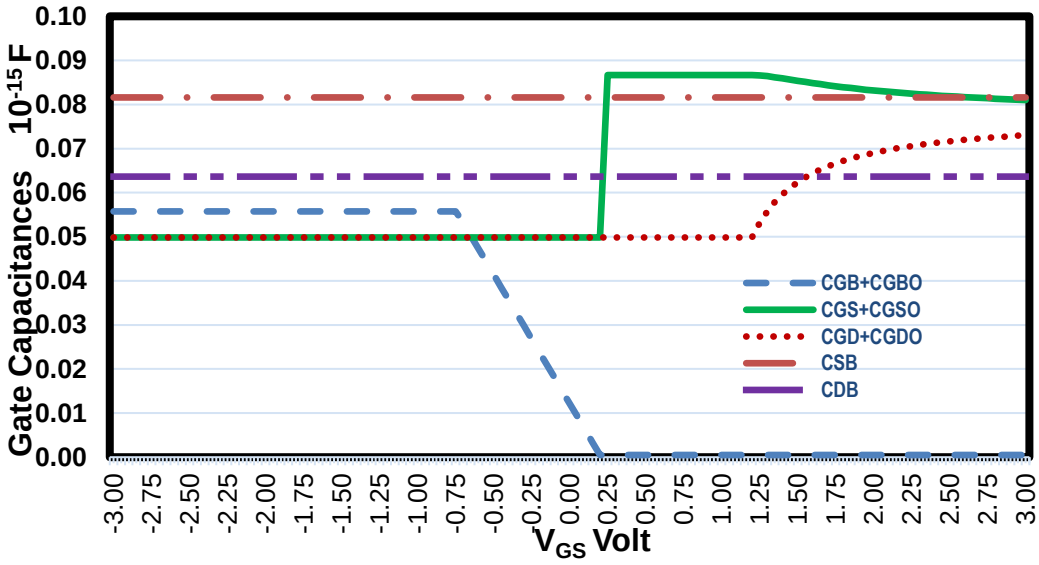


Figure 15. Meyer model for 20nm n-MOSFET all five capacitances C_{GB}+C_{GBO0}, C_{GS}+C_{GSO}, C_{GD}+C_{GDO}, C_{BS}, and C_{BD}.

The more accurate model for the gate capacitances is AMI-ASPEC [36, 40]. Appendix C shows the AMI code [36]. The capacitance formulas are shown in Table 9B. As AMI and Meyer model, give same value for C_{GS} and C_{GD}. In AMI model C_{GB} is combined with C_{ox} and depletion capacitance (C_d). However this improves accuracy of gate to body capacitance C_{GB} as shown in Figure 19.

Table 9B. AMI-ASPEC capacitances model.

Mode	Accumulation	Depletion	Saturation	Linear
C_{GS}	0	$0.75 * \frac{C_{ox} * V_{gst}}{V_{th} - V_{FB}}$	$\frac{2}{3}C_{OX}$	$V_{gst}\frac{V_{gst} - 2V_{DS}}{(V_{th} - V_{FB})^2} * \frac{2}{3}C_{OX}$
C_{GD}	0	0	0	$(3V_{gst} - V_{DS})\frac{V_{gst} - V_{DS}}{(2V_{gst} - V_{DS})^2} * \frac{2}{3}C_{OX}$
C_{GB}	$\frac{(C_{OX} - C_{GS} - C_{GD}) * C_d}{(C_{OX} - C_{GS} - C_{GD}) + C_d}$			

Where,

Effective Channel Length $L_{eff} = L - 2 * L_D$ and effective Width $W_{eff} = W - 2 * W_D$

$$V_{gst} = V_{GS}\frac{V_{th} - V_{FB}}{2}$$

The depletion width $W_d = \sqrt{\frac{2 * \varepsilon_{Si}.vc}{qNa}}$ and the Depletion capacitance $C_d = \frac{\varepsilon_{Si}}{W_d} W_{eff} * L_{eff}$

The effective voltage from channel to body $vc = \begin{cases} 0\ at\ \text{Accumulation} \\ V_{GS} + V_{SB} - V_{FB}\ \ Else\ where \end{cases}$

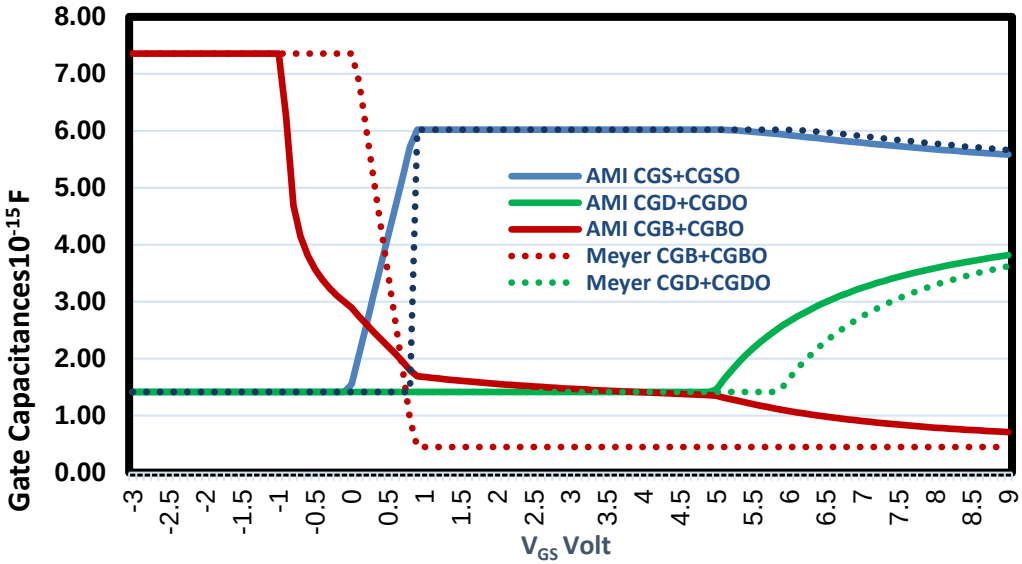


Figure 16. The capacitances of L=1 um n-MOSFET AMI (solid) and Meyer (doted).

The SWS-FET capacitance and regions of operation are same what related channel MOS-EFT. The capacitance in 2-QW n-SWS-FET can be simplified as circuit in Figure 17, it divided into five different parts:

1- Three overlap capacitances (C_{GBO}, C_{GSO}, C_{GDO})

2- Two junction capacitances (C_{BS}, C_{BD})

3- One gate to body capacitance (C_{GB})

4- Two gate to source capacitances (C_{GS1}, C_{GS1})

5- Two gate to drain capacitances (C_{GD1}, C_{GD2})

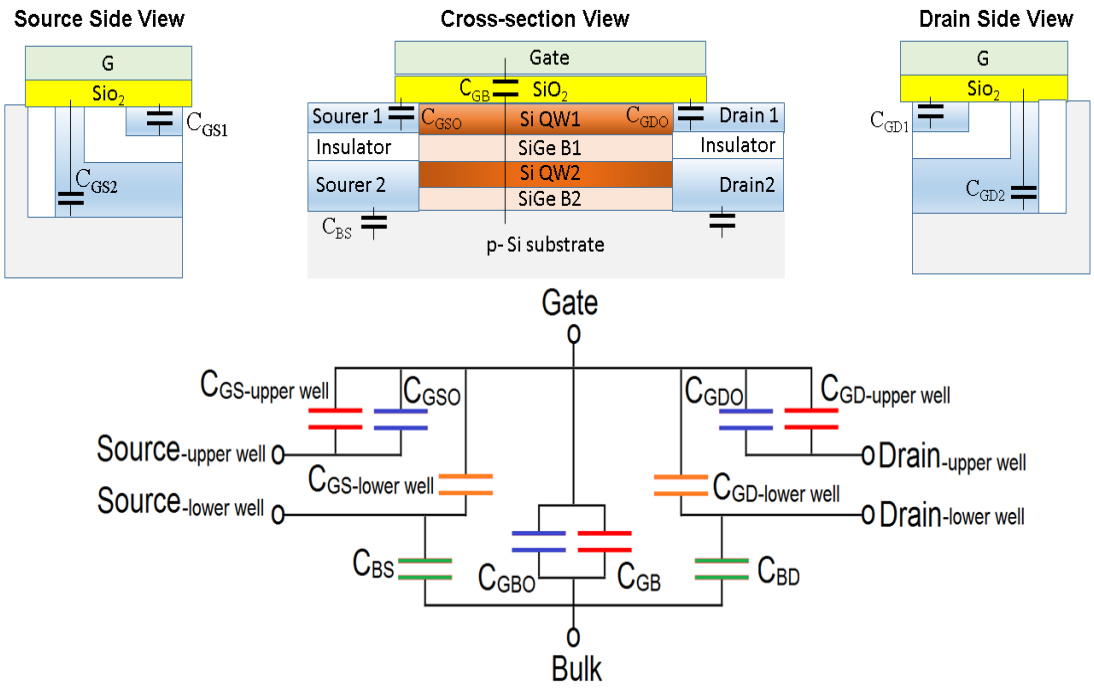


Figure 17. 2-QW -SWS-FET capacitances.

Figures 18 shows the twin-drain structure SWS-FET where the gate to source capacitance becomes similar to conventional n-MOSFET.

The overlap (C_{GBO}, C_{GSO}, C_{GDO}), and junction (C_{BS}, C_{BD}) capacitances are similar to a single drain/ single source FET and associated with the respective lower well W2 and upper well W1. The magnitude of gate capacitances C_{GB}, C_{GS1}, C_{GS2}, C_{GD1}, and C_{GD2} depend on gate voltage (regions of operation) as shown in Table10.

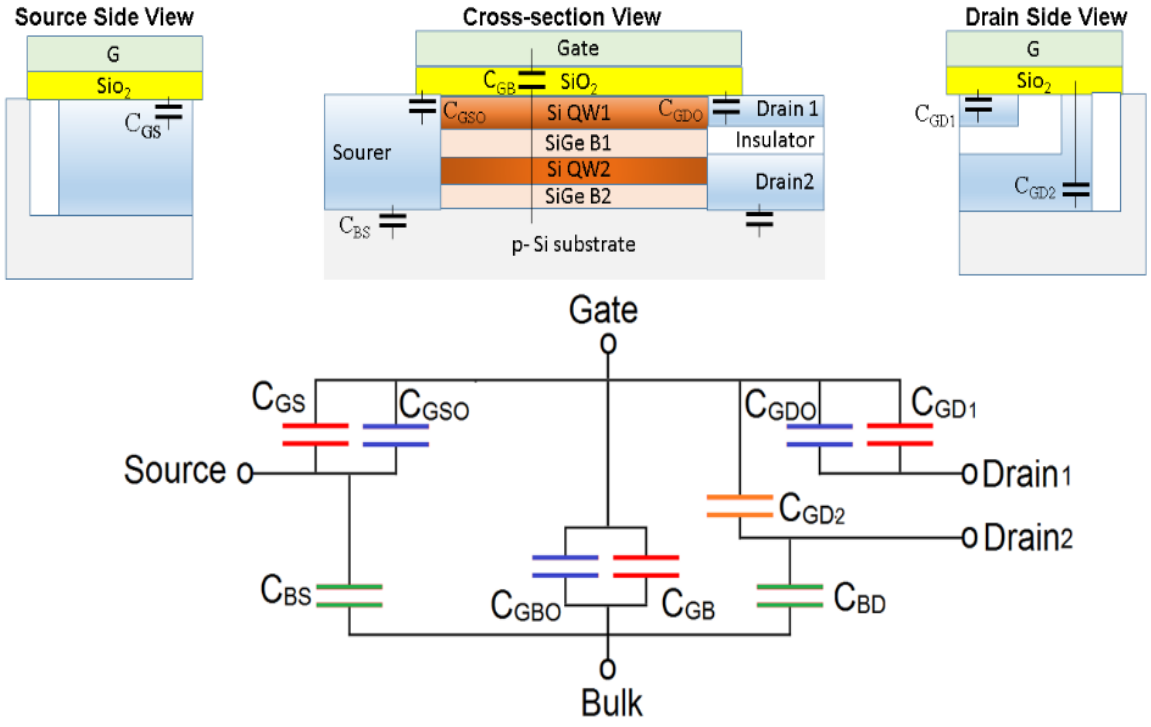


Figure 18. Twin-drain n-SWS-FET capacitances.

Table 10. The Meyer model for 2-QW n-SWS-FET gate capacitances.

Cap.	Accumulation	Depletion	Saturation	Linear
V_{GS1}	V_{GS1}-V_{th1}<PHI	V_{GS1}-V_{th1}<0	V_{GS1}-V_{th1}< V_{D1S1}	V_{GS1}-V_{th1}>V_{D1S1}
C_{GB1}	C_{OX}	$C_{OX}\frac{V_{th1}-V_{GS2}}{\text{PHI}}$	0	0
C_{GS1}	0	0	$\frac{2}{3}C_{OX}$	$\frac{2}{3}C_{OX}[1-\left(\frac{V_{GD2}-V_{dth2}}{V_{GS2}+V_{GD2}-2V_{dth2}}\right)^2]$
C_{GD1}	0	0	0	$\frac{2}{3}C_{OX}[1-\left(\frac{V_{GS}-V_{dth}}{V_{GS}+V_{GD}-2V_{dth}}\right)^2]$
V_{GS2}	V_{GS2}-V_{dth2}<PHI	V_{GS2}-V_{dth2}<0	V_{GS2}-V_{dth2}<V_{D2S2}	V_{GS2}-V_{dth2}>V_{D2S2}
C_{GB2}		$C_{OX}\frac{V_{dth2}-V_{GS2}}{\text{PHI}}$	0	0
C_{GS2}	0	0	$\frac{2}{3}C_{OX}$	$\frac{2}{3}C_{OX}[1-\left(\frac{V_{GD2}-V_{dth2}}{V_{GS2}+V_{GD2}-2V_{dth2}}\right)^2]$
C_{GD2}	0	0	0	$\frac{2}{3}C_{OX}[1-\left(\frac{V_{GS}-V_{dth}}{V_{GS}+V_{GD}-2V_{dth}}\right)^2]$
C_{GB}	is a parallel capacitor of C_{GB1} and C_{GB2}, C_{GB} =C_{GB1} +C_{GB2}			

Figure 19A represents 2-QW n-SWS-FET capacitances. The plot is obtained using the parameters listed in Table 8 and the formulas in Table 10. Here, we have used (V_{DD}=5V, Vth1=0.858, Vth2=0.56, L=1um, and W=4um).

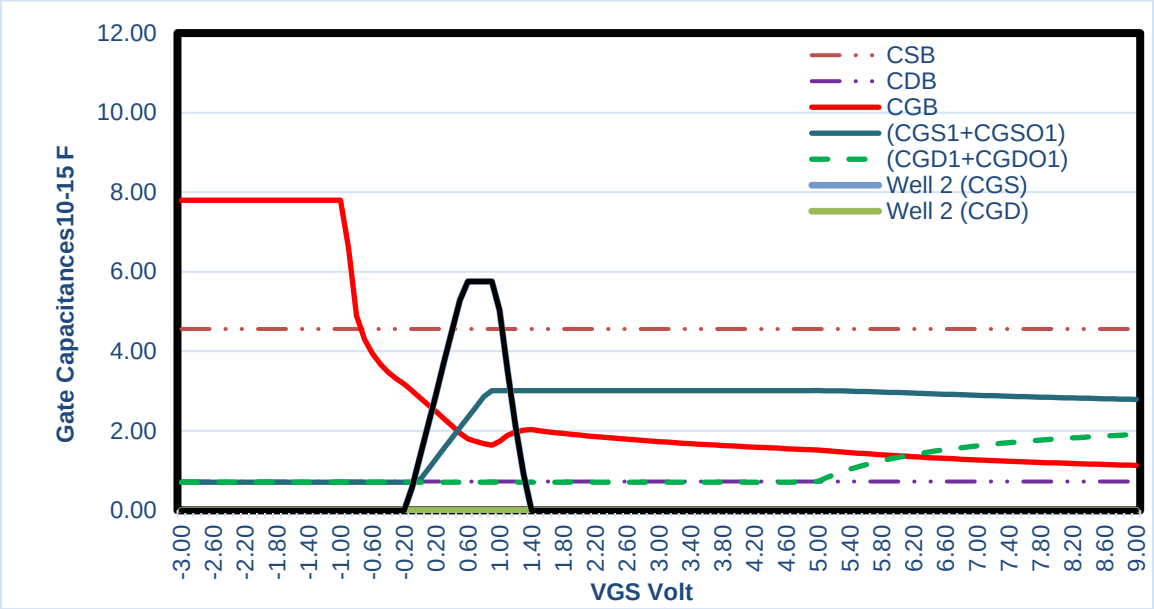


Figure 19A. The calculation of 2-QW n-SWS-FET AMI model capacitances L=1um.

Figure 19B shows the capacitances of 20 nm channel length 2-QW n-SWS-FET. The device parameters listed in Table 8.

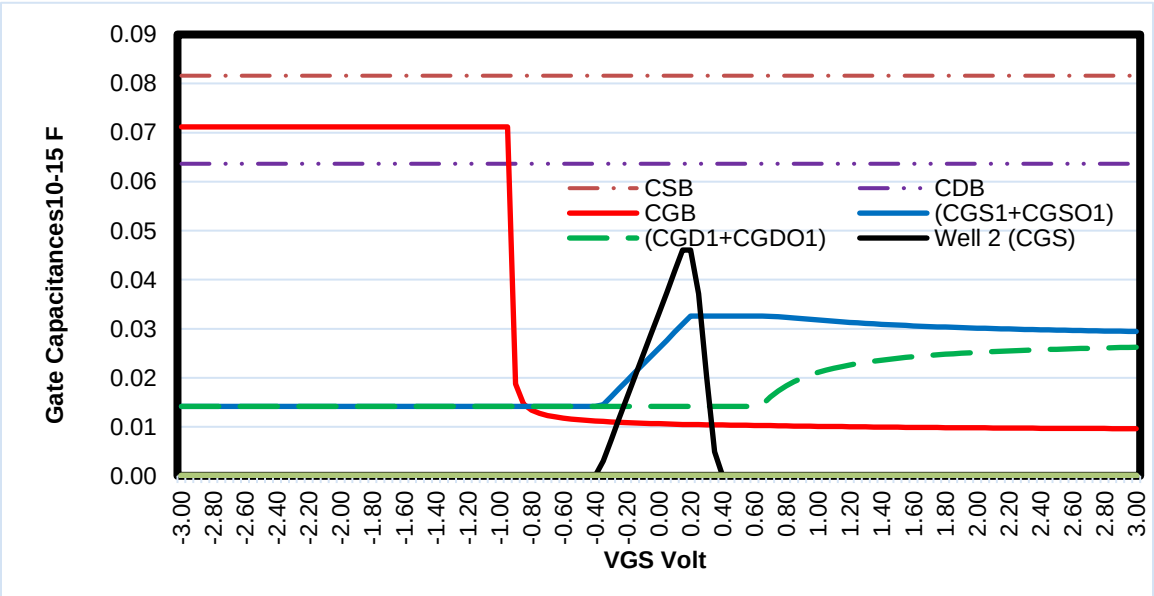


Figure 19B. The calculation of 2QW n-SWS-FET AMI model capacitances L=20nm.

Table 11A shows the compassion between n-MOS-FET and n-SWS-FET capacitance for 1 µm channel length device, where the width of n-MOS-FET is 2 µm and the width of n-SWS-FET wells are W1=1.25 µm and W2=2.5 µm, where the area of n-MOS-FET is 10λ*4λ and n-SWS-FET is 7λ*5λ as shown in figures 6A and 6B. Figure 20 shows the gate to body capacitance (C_{GB}) of n-MOSFET and n-SWS-FET. Table 11B shows the capacitances n-SWS-FET deceive which has the area = 10λ*8λ (L=1 µm , W1=2 µm, W2=4 µm).

Table 11 A. n-MOSFET and n-SWS-FET capacitances (10^{-15} Farad) for L=1µm.

Capacitance		Accumulation	Depletion	Saturation	Linear
		Vdsat <PHI	**Vdsat <0**	**Vdsat < VDS**	**Vdsat > VDS**
Equation	**C_{GB}**	$C_{OX} + C_{GB0}$	$C_{OX}\frac{V_{th} - V_{GS}}{\text{PHI}} + C_{GB0}$	$\approx C_{GB0}$	$= C_{GB0}$
	C_{GS}	$\approx C_{GS0}$	$\approx C_{GS0}$	$\approx \frac{2}{3}C_{OX} + C_{Gs0}$	$\approx \frac{1}{2}C_{OX} + C_{Gs0}$
	C_{GD}	$\approx C_{GD0}$	$\approx C_{GD0}$	$\approx C_{GD0}$	$\approx \frac{1}{2}C_{OX} + C_{Gs0}$
MOSFET	**C_{GB}**	3.903	3.903 to 1.003	1.003	0.58
	C_{GS}	0.708	0.708	3.010	2.658
	C_{GD}	0.708	0.708	0.708	2.434
SWS-FET	**C_{GB1}**	2.608	2.608 to 0.94	0.94	0.725
	C_{GB2}	2.608	2.608 to 0.84	0.84	0.5321
	C_{GB}	5.126	5.126 to 1.78	1.78	1.291
	C_{GS1}	0.4425	0.4425	1.881	1.192
	C_{GS2}	0.4425	0.4425	1.881	N.A*
	C_{GD1}	0.4425	0.4425	0.4425	1.192
	C_{GD2}	0.4425	0.4425	0.4425	N.A*

* The lower well W2 doesn't go to linear mode (the charges completely move to upper well and when $V_{dsat\text{-}W2} = V_{GS2} - V_{TH2} > V_{DS2}$).

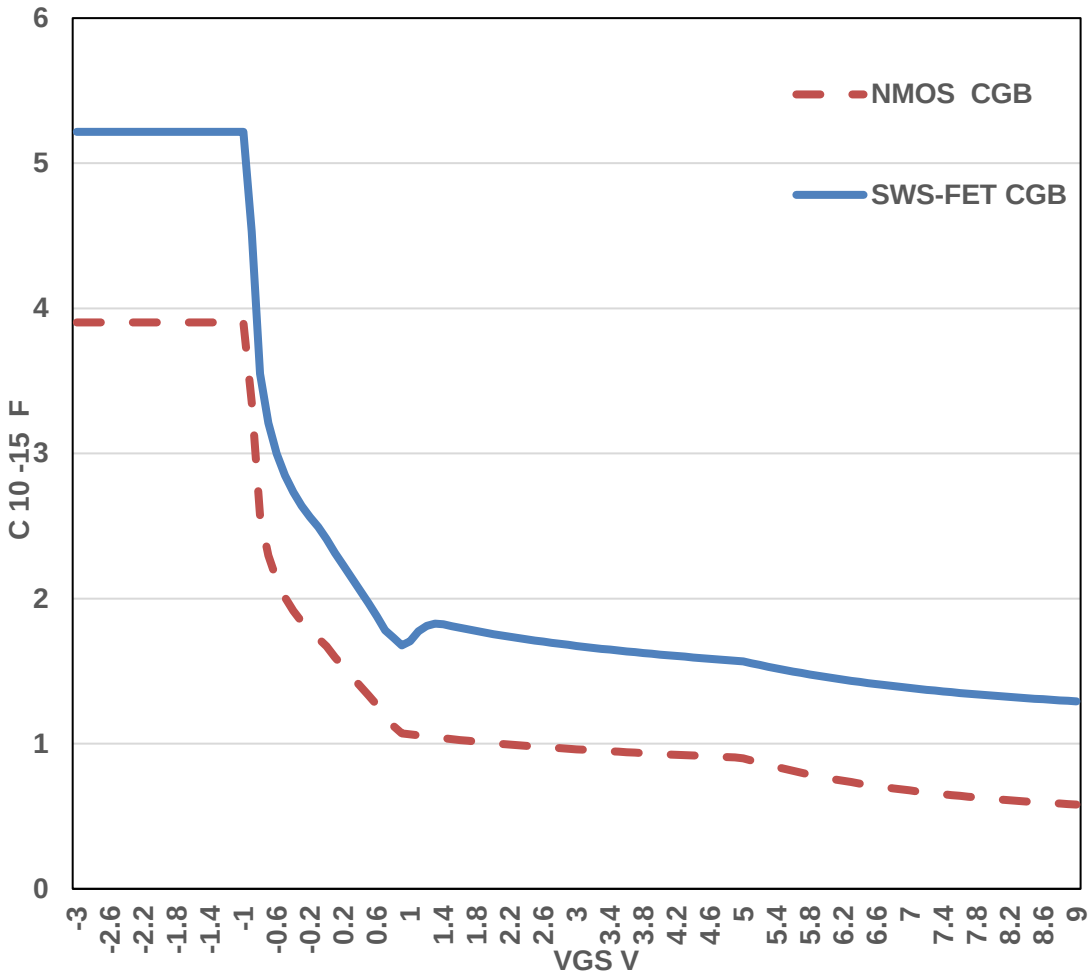


Figure 20. Gate-body capacitance C_{GB} of n-MOSFET and n-SWS-FET for L=1µm.

Table 11 B. The capacitances of n-SWS-FET (L=1 µm , W1=2 µm, W2=4 µm)

Capacitance		Accumulation	Depletion	Saturation	Linear
		Vdsat <PHI	Vdsat <0	Vdsat < VDS	Vdsat > VDS
WS-FET	C_{GB}	7.8	7.8 to 1.78	1.8	1.8
	C_{GS1}	0.69	0.69	2.99	2.145
	C_{GS2}	0.69	0.69	2.3	N.A*
	C_{GD1}	0.69	0.69	0.69	2.415
	C_{GD2}	0.69	0.69	0.69	N.A*

2-2-3 SWS-FET Transconductances (g_m, g_{mb},) and output conductance g_o

An important parameter characteristic for a transistor is transconductances g_m, g_{mb}, and g_o. g_m represents the change in the drain current (I_{DS}) as a function of change in the gate to source voltage (V_{GS}) with a constant drain-source voltage (V_{DS}). Similarly, g_{mb} denotes the backgate transconductance which describes how I_{DS} changes with voltage between body to source (V_{BS}) change. In addition, g_O is the output conductance or a reciprocal of output resistance ($r_o = g_o^{-1}$), g_o describes how is I_{DS} change with V_{DS}. Equations 12, 13, 14 define the transconductances g_m, g_{mb}, and conductance g_o.

$$g_m = \frac{dI_{DS}}{dV_{GS}} \quad \text{at fixed } V_{DS} \text{ and } V_{BS} \tag{12}$$

$$g_{mb} = \frac{dI_{DS}}{dV_{BS}} \quad \text{at fixed } V_{DS} \text{ and } V_{GS} \tag{13}$$

$$g_o = \frac{1}{r_o} = \frac{dI_{DS}}{dV_{DS}} \quad \text{at fixed } V_{GS} \text{ and } V_{BS} \tag{14}$$

As the value of V_{DS} increases, it causes the effective channel length (L) to decrease which causes I_{DS} to increase by factor of $(1+\lambda * V_{DS})$, where λ is called the channel length modulation (CLM). λ depends of channel doping (N_a). The calculation of λ from device structure is quite difficult, it can be obtained from I_{DS}-V_{DS} plot for V_{GS} - V_{th} >0 (i.e. the transistor is not in cutoff). At the saturation region, the voltage which corresponds to the intersection of a tangent line touching the bias point (I_{DS}=0) on I_{DS}-V_{DS} curve is called Early Voltage ($V_A = \lambda^{-1}$) as shown in Figure 21 and Equation 15, Appendix E has the calculation of n-MOSFET 1 µm (λ=0.018) and 20 nm (λ=0.05).

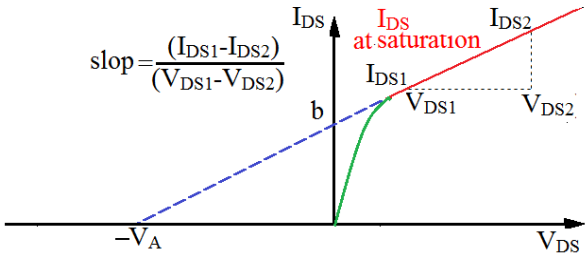


Figure 21. The simple graphical method to obtain an approximate value for lambda.

$$I_{DS-Saturation} \approx slop * V_{DS} + b = g_o * V_{DS} + b \tag{15}$$

$$I_{DS-Saturation} = I_{DS0-Saturation} * [1 + \lambda V_{DS}] = \frac{\beta}{2}(V_{GS} - V_{th})^2 * [1 + \lambda V_{DS}] \tag{16}$$

$$\beta = \mu * C_{OX} * \frac{W}{L} \tag{17}$$

Table 12 shows the transconductances (g_m, g_{mb}) and the output conductance g_o of n-MOSFET in different operation mode [37-38], Figures 22, 23, and 24 show plots of g_m , g_{mb}, and g_o as afunction of V_{GS} for 1µm-MOS using the parameters in Table 8 and the formulas in Table 13 (V_{DD}=5 V, V_{th}=0.858 V, λ =0.018 V^{-1}, L=1µm, and W=2µm).

Table 12. The transconductances and the output conductance of n-MOSFET.

Mode	**Cutoff** $V_{GS}-V_{th}<0$	**Saturation** $V_{GS}-V_{th}<V_{DS}$	**Linear** $V_{GS}-V_{th}>V_{DS}$
g_m	0	$\beta(V_{GS}-V_{th})$, Ignoring CLM $\beta(V_{GS}-V_{th})*(1+\lambda V_{DS})$	βV_{DS}
g_o	0	$I_{DS0-Saturation}*\lambda$	$\beta(V_{GS}-V_{th}-V_{DS})$
g_{mb}	$g_m * \frac{\gamma}{2*\sqrt{PHI+VSB}}$		

Where: γ (the body-effect parameter) & PHI (the surface potential) as defined in Table 9.

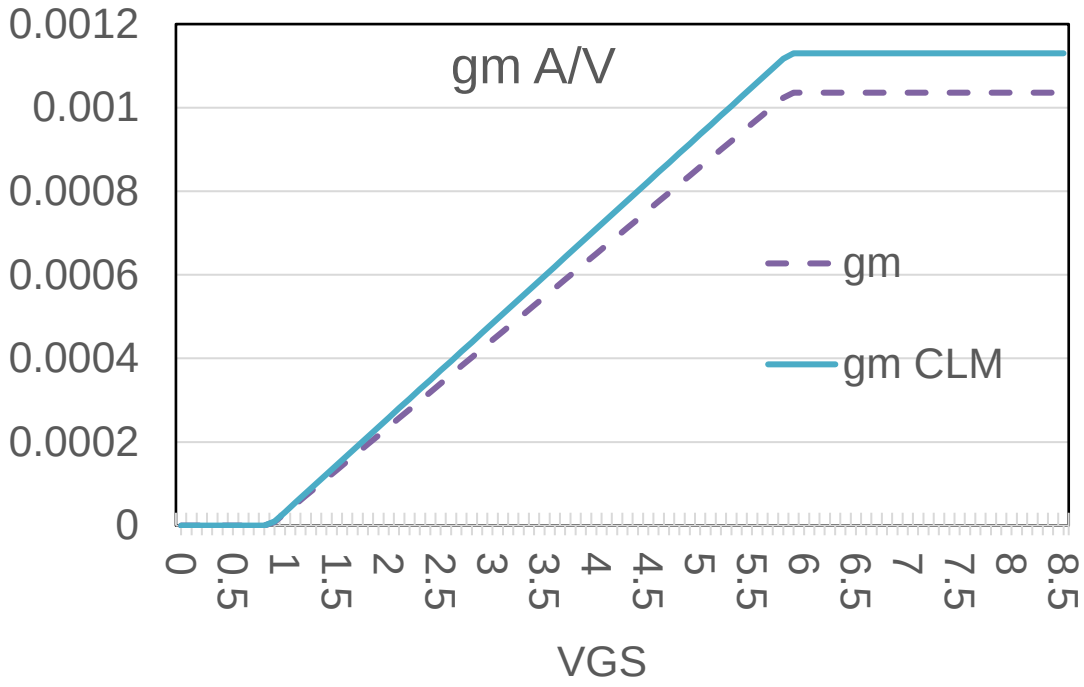


Figure 22. g_m vs VGS for 1µm n-MOSFET.

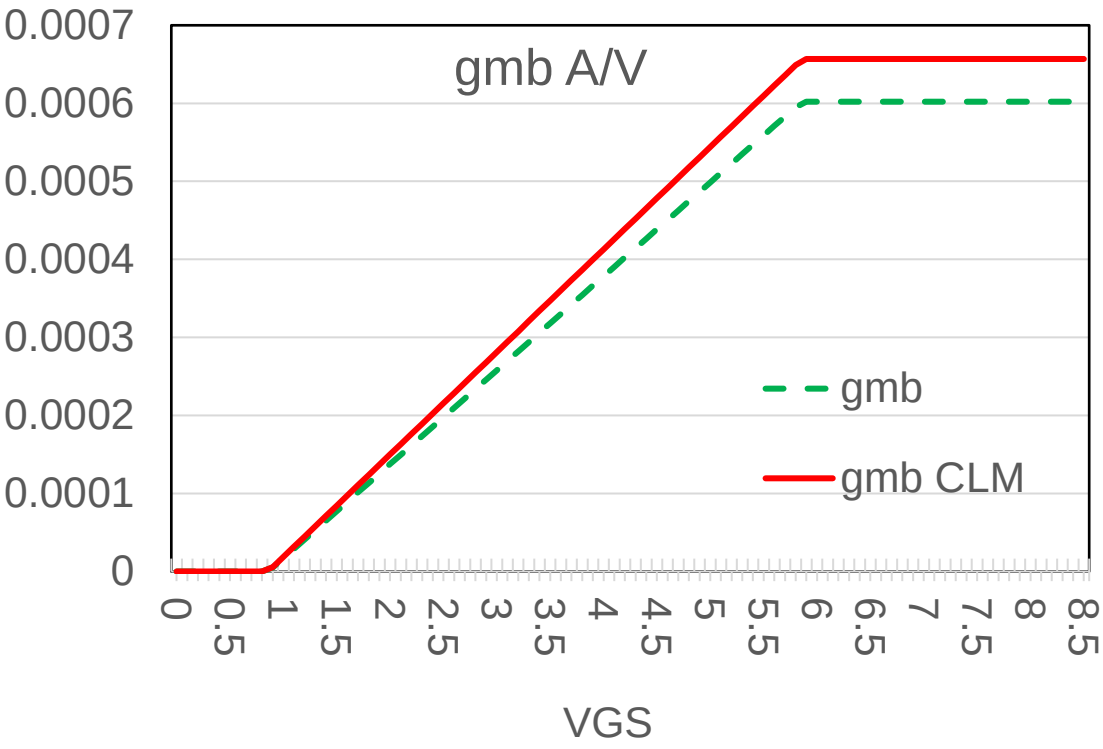


Figure 23. g_{mb} vs VGS for 1µm n-MOSFET.

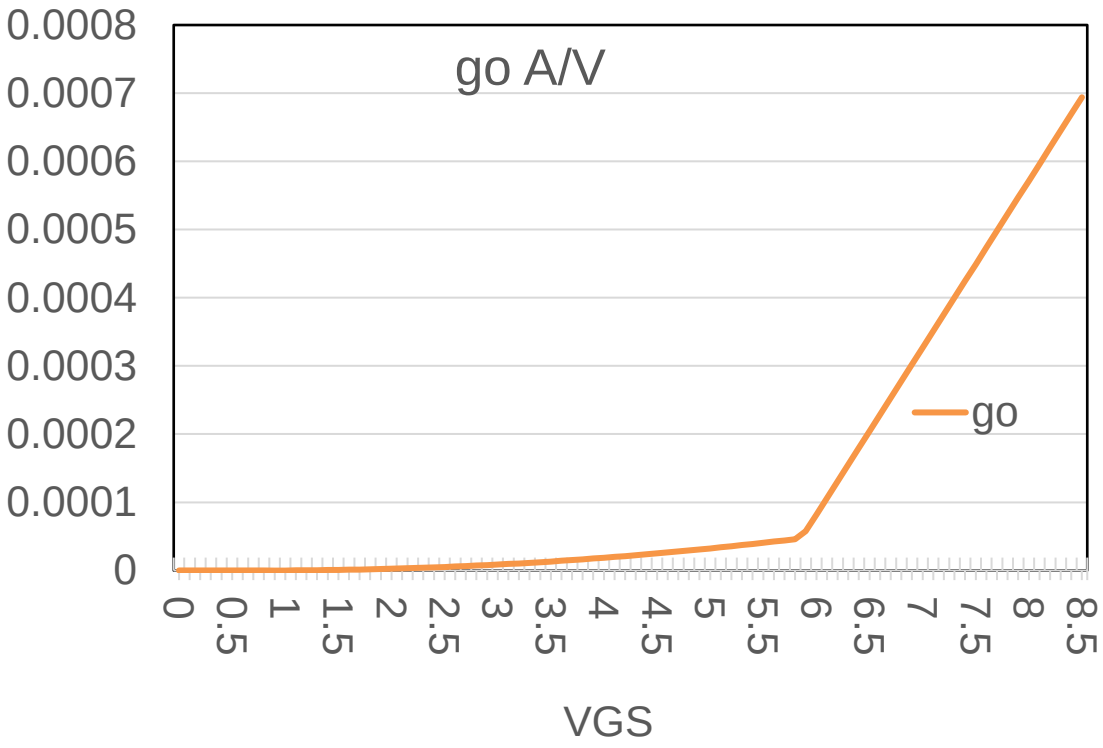


Figure 24. g_o vs VGS for 1µm n-MOSFET.

The transconductances and the output conductance g_o of 20 nm n-MOSFET are shown in Figures 25, 26, and 27 (V_{DD}=1V, V_{th}=0.20V, λ =0.05V^{-1}, L=20nm, and W=80nm).

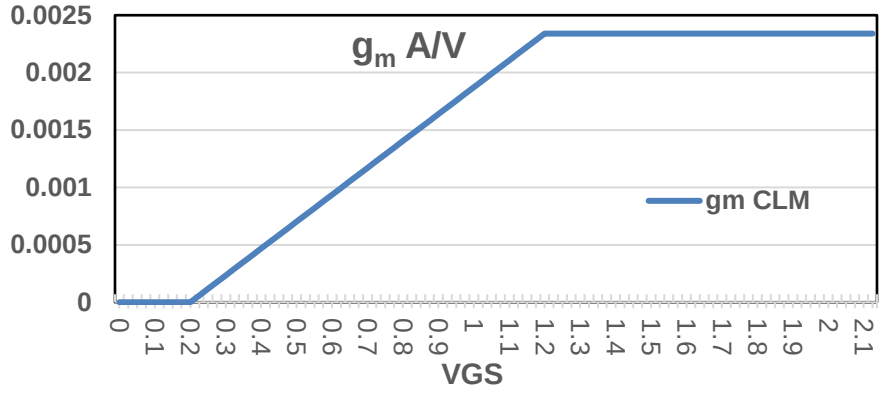


Figure 25. g_m vs VGS for 20nm n-MOSFET

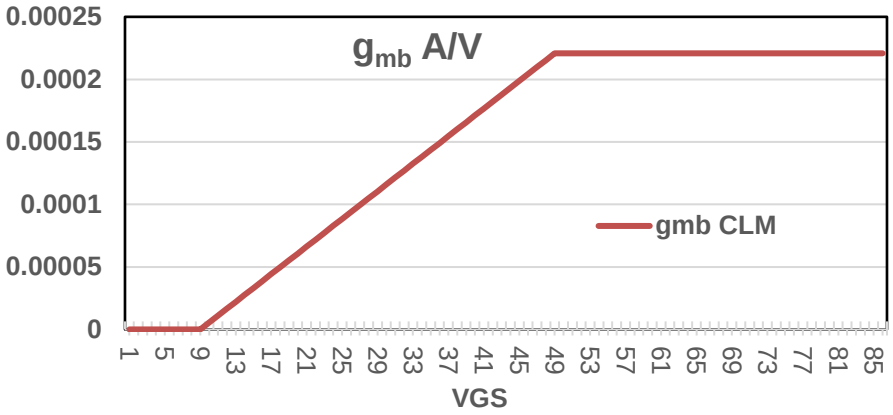


Figure 26. g_{mb} vs VGS for 20nm n-MOSFET

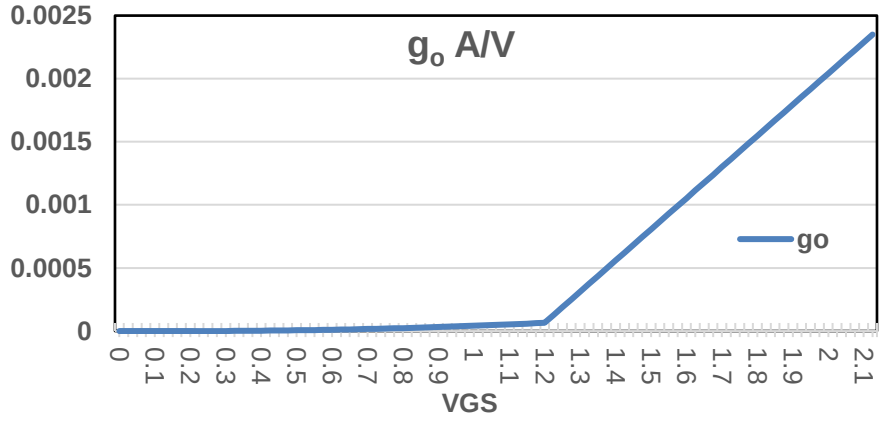


Figure 27. g_o vs VGS for 20nm n-MOSFET

For the twin-drain SWS-FET, the transconductances (g_m, g_{mb}) and the output conductance g_o are shown in Figure 28, 29 and 30. The transconductances and conductance for lower well W2 are shown in top right box in Figures 28, 29 and 30. g_m, g_{mb} , and g_o for W2 have the same switching functionality as the drain current in W2. Furthermore, the transconductances (g_m, g_{mb}) and the output conductance g_o for upper W1 are similar to a conventional n-MOSFET.

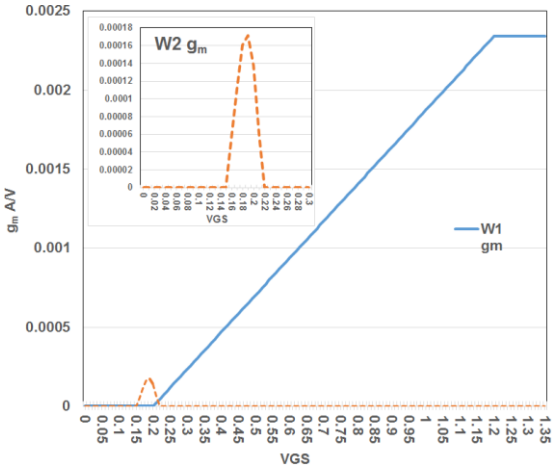


Figure 28. g_m for 20nm n-SWS-FET

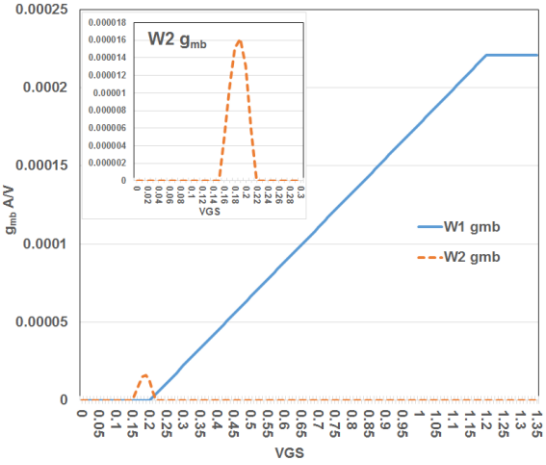


Figure 29. g_{mb} for 20nm n-SWS-FET

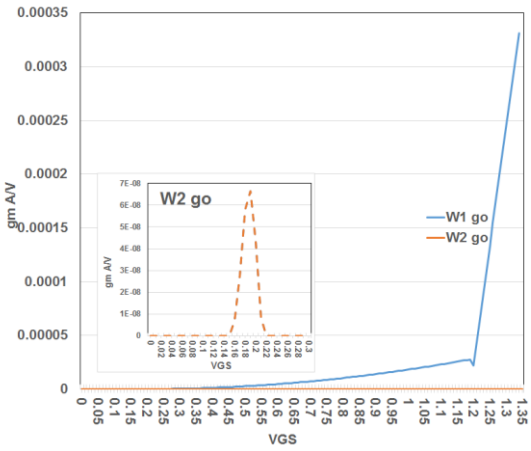


Figure 30. g_o for 20nm n-SWS-FET

2-2-4 SWS-FET as a Switch.

A MOSFET can be used as a switch as shown in Table13A as well as Figure 31A. The switch in the n-MOSFET is closed (conducting D with S) when V_{GS} =0 and opened (non-conducting) when V_{GS} = 0 or ground, the switch sequence is as OFF-ON. In the case of p-MOSFET, the switch is closed when V_{GS} = 0 or ground and Open when V_{GS} = V_{DD}, the switch sequence is as ON-OFF as shown in Table13A and Figure 31A.

The switching for the upper well W1 in n-SWS-FET is to NMOS, unlike conventional FETs, the lower well W2 in n-SWS-FET has OFF-ON-OFF switching sequence as shown in Table13B and Figure 31B. This results in SWS-FET to be used as a four-state switch which. A four state such place to a conventional CMOS in order to three NMOS and one PMOS.

Table 13A. The switching mode for n-MOSFET and n-SWS-FET

n-MOSFET	$V_{GS} < V_{thn,}$ or V_{GS}=0	$V_{GS} > V_{thn}$ or V_{GS}=V_{DD}
	OFF	ON
p-MOSFET	$V_{GS} < V_{thp}$ or V_{GS}= 0	$V_{GS} > V_{thp}$ or V_{GS}= V_{DD}
	ON	OFF

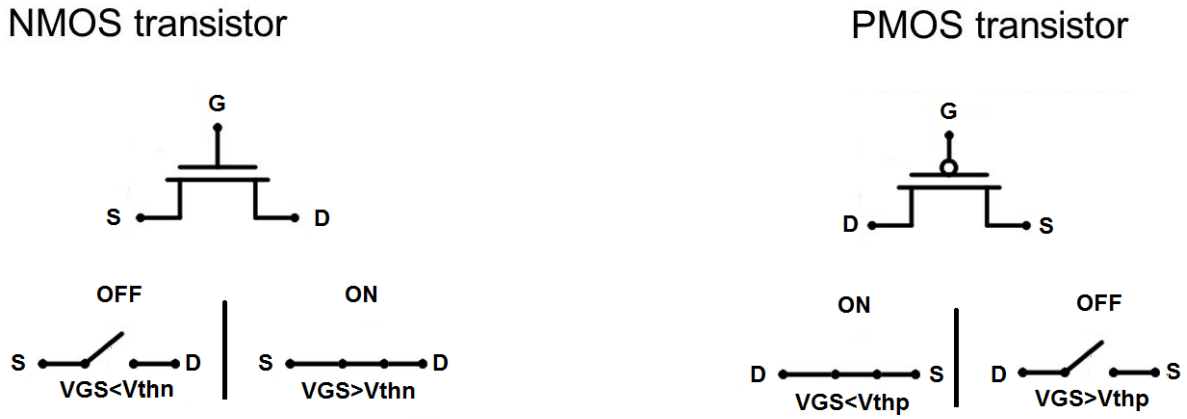


Figure 31A. SWS-FET switch

Table 13B. The switching mode for n-SWS-FET

Upper well n-SWS-FET	$V_{GS} < V_{thn1,}$ or V_{GS}=0	$V_{GS} > V_{thn1}$ or V_G=V_{DD}	
	OFF	ON	
Lower well n-SWS-FET	$V_{GS} < V_{thn2}$	$V_{GS} > V_{thn2}$	$V_{GS} < V_{dthn}$= V_{th2}+ α
	OFF	ON	OFF

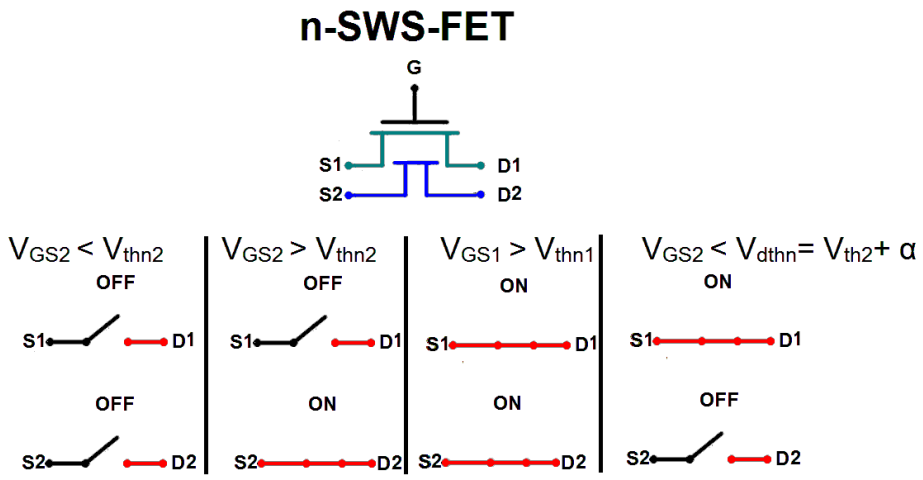


Figure 13B. n-SWS-FET switch

Table 13C and figure 31C shows the switching for the upper well W1 and lower well W2 in p-SWS-FET.

Table 13C. The switching mode for p-SWS-FET

Upper well p-SWS-FET	$V_{GS} < V_{thp1}$, or $V_G=0$	$V_{GS} > V_{thp1}$ or $V_{GS}=V_{DD}$	
	ON	OFF	
Lower well p-SWS-FET	$V_{GS} < V_{dthP} = V_{thP2} + \alpha$	$V_{GS} < V_{thn2}$	$V_{GS} > V_{thp2}$ or $V_G=V_{DD}$
	OFF	ON	OFF

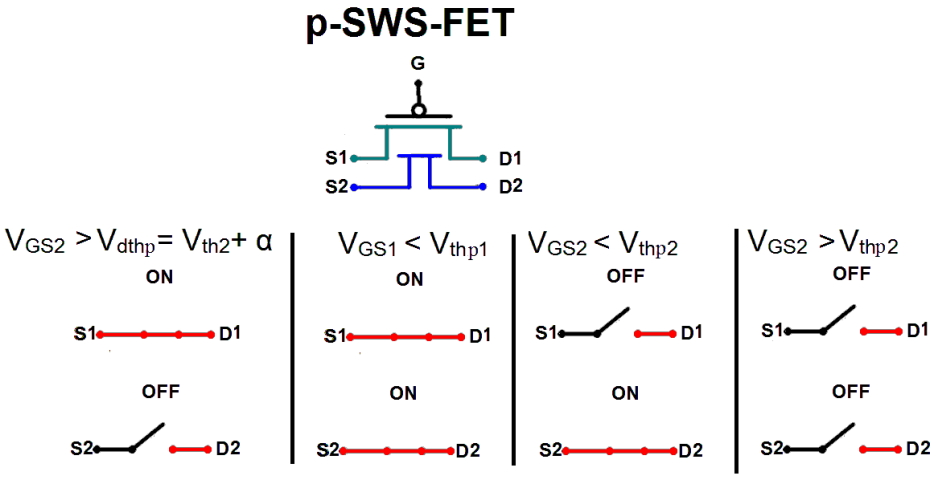


Figure 13C. p-SWS-FET switch

3- Circuit Model for SWS-FETs

SWS-FET has two or more quantum wells (2-QW) separated by barriers. Each well conducts in certain voltage range as the transport channel as discussed in chapter 2 (Equations 2-5). The threshold voltage V_{th2} for the lower well W2 is adjusted by a parameter α which simulates the decreases of drain current in well 2 due to transfer of carriers to well 1, α may depend on V_{DS}. The transistor model like BSIM cannot adjust the threshold voltage while the simulation is running.

This work shows two circuits which are capable of adjusting the changing of the threshold voltage during the simulation. The model represents a SWS-FET by two transistors, one n-MOSFET for the upper well (W1) and other for the lower well (W2), the model use two BSIM equivalent circuits for two transistors representing each quantum well channel.

3-1 BSIM level 7 Model for SWS-FET

Generally, CMOS models are divided into three classes: First Generation Models (Level 1, Level 2, and Level 3), Second Generation Models (BSIM Level 5, HSPICE Level 28) and Third Generation Models (BSIM Level 7, Level 8). The level is set for different channel length values and accounts for various effect. These effects are short channel effects, gate leakage (tunneling), noise calculations, and temperature. The current express by Equations 1, 2, and 4 in chapter 2. These are recommended for MOSFETs with gate lengths of 10 µm or more. For example Equation 18 shows Level 6 I_{DS} equation.

$$\mathrm{Ids} = \beta\left\{\left(\mathrm{Vgs} - \mathrm{Vbi} - \frac{\eta * \mathrm{Vde}}{2}\right)\mathrm{Vde} - \frac{2}{3}\gamma[(\mathrm{PHI} + \mathrm{Vde} + \mathrm{Vsb})^{\frac{2}{3}} - (\mathrm{PHI} + \mathrm{Vsb})^{\frac{2}{3}}]\right\} \quad \textbf{18}$$

Where :

W_{eff} , $L_{eff.}$, μ, and γ are as defined in chapter 2, and $\beta = C_{OX} * \mu_{eff}\frac{W_{eff}}{L_{eff}}$

Vbi is built-in voltage and defined as: $Vbi = V_{fb} + PHI$.

Vde = min(Vds,Vdsat).

η= 1+ Narrow-Width-Effect(NWE) /W_{eff} , (W_{eff} inµm)

The Level 1 (First Generation Model) can be used for n-SWS-FET for 1-10 µm channel length by adding a correction function f(V_{GS}), Table 14 shows the correction function f(V_{GS}) which is obtained by plotting the ratio of $I_{DS\text{-}LEVEL7}$/ $I_{DS\text{-}LEVEL1}$ and then

using the best fitting polynomial. I_{DS} equations are modified using correction function $f(V_{GS})$ as I_{DS} modified for n-MOSFET and n-SWS-FETs. This appropriate has provided a good results to develop SWS-FET to Level 7 (Third Generation Model) equation.

$$I_{DS-Modified(Linear)} = I_{DS(Linear)} * f(V_{GS})_{Linear}$$
$$I_{DS-Modified(Saturation)} = I_{DS(Saturation)} * f(V_{GS})_{Saturation} \quad \text{FET} \quad \textbf{(19)}$$

$$I_{DS-W1-Modified(Linear)} = I_{DS-W1(Linear)} * f(V_{GS})_{Linear}$$
$$I_{DS-W1-Modified(Saturation)} = I_{DS-W1(Saturation)} * f(V_{GS})_{Saturation} \quad \text{Well-1 SWS} \quad \textbf{(20)}$$

$$I_{DS-W2-Modified(Linear)} = I_{DS-W2(Linear)} * f(V_{GS})_{Linear}$$
$$I_{DS-W2-Modified(Saturation)} = I_{DS-W2(Saturation)} * f(V_{GS})_{Saturation} \quad \text{Well-2 SWS} \quad \textbf{(21)}$$

Table 14. The correction function $f(V_{GS})$ for the different channel length. X=V_{GS}

Length	$f(V_{GS})$ Weak inversion	$f(V_{GS})$ Saturation	$f(V_{GS})$ Linear
20 nm	0.0006x-6e-6	$-0.256x^3+0.533x^2-0.32x+0.06$	$-0.012x^2+0.028x+0.001$
50 nm	0.0005x – 5e-5	$-0.13x^3+0.281x^2-0.17x+0.033$	$-0.099x^2+ 0.02x\ \ 0.003$
0.5 µm	0.0349x - 0.0074	$+0.368x^3-2.224x^2+4.29x- 2.28$	$+0.01x^2-0.130x+ 0.557$
1 µm	0.0037x - 0.0011	$+0.063x^3-0.56x^2+1.59x-1.175$	$+0.004x^2- 0.069x+ 0.46$

The compression between I_{DS} Level 1 & 7 (by Cadence) is shown in Figures 32 A and B. The same current compression after adding the correction function $f(V_{GS})$ is shown Figure 33 A and B.

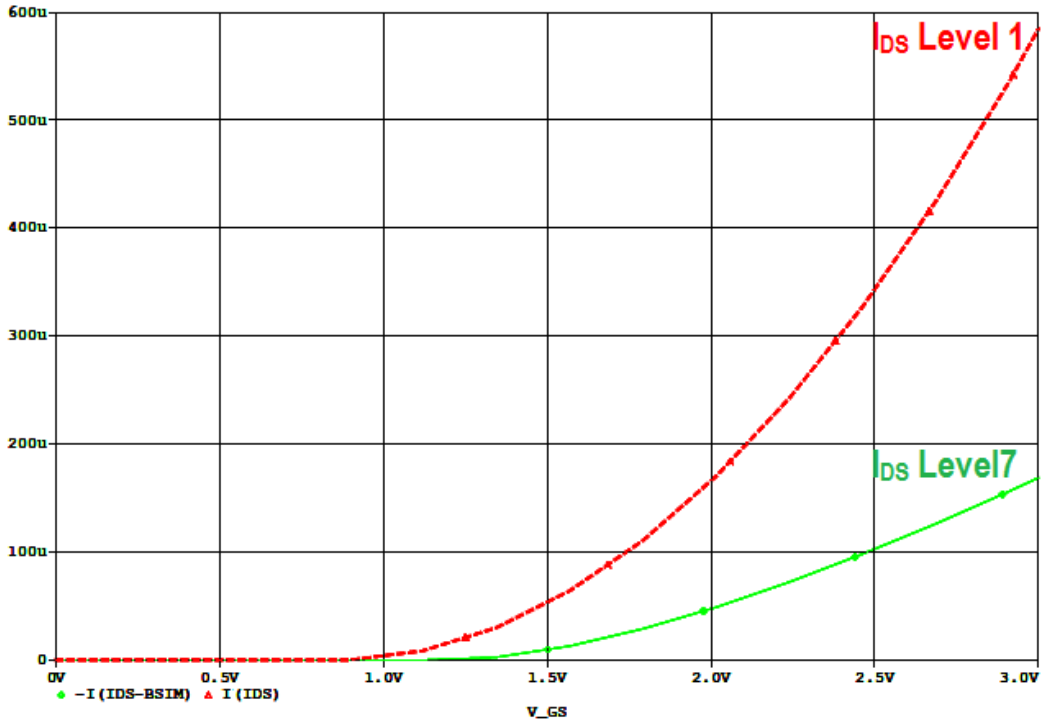


Figure 32A. I_{DS} Level 1(- -) and Level 7(—) for L=1µm n-MOSFET.

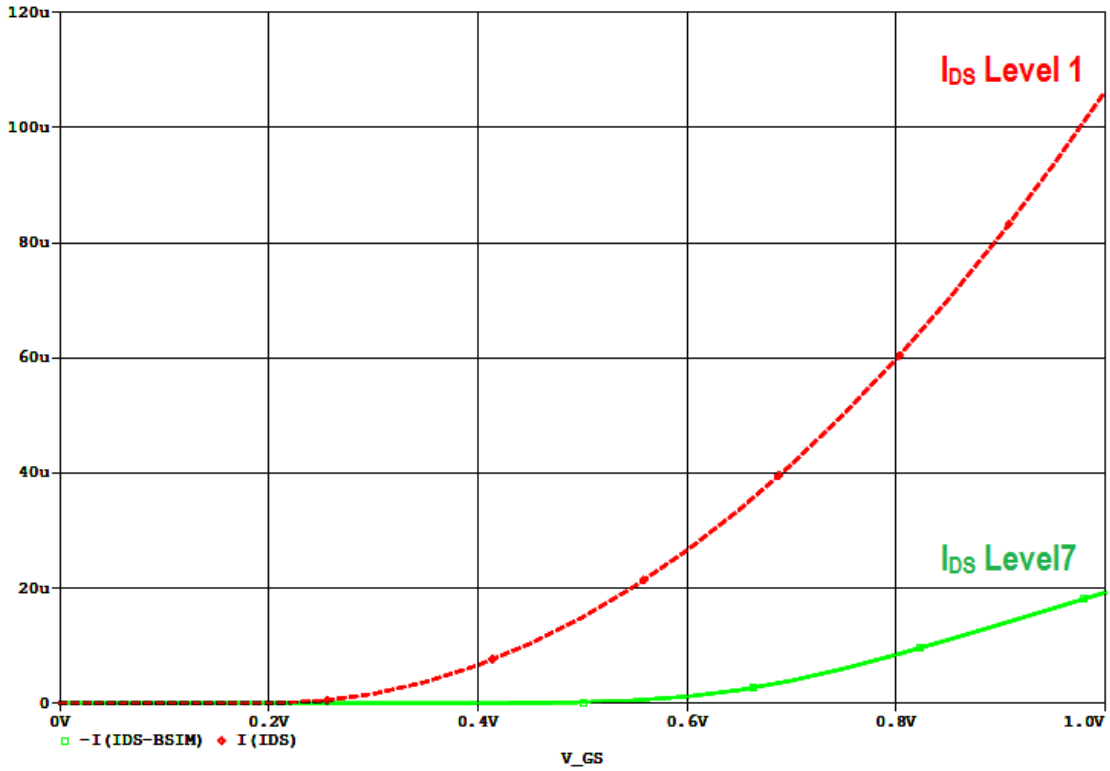


Figure 32B. I_{DS} Level 1(- -) and Level 7(—) for L=20 nm n-MOSFET.

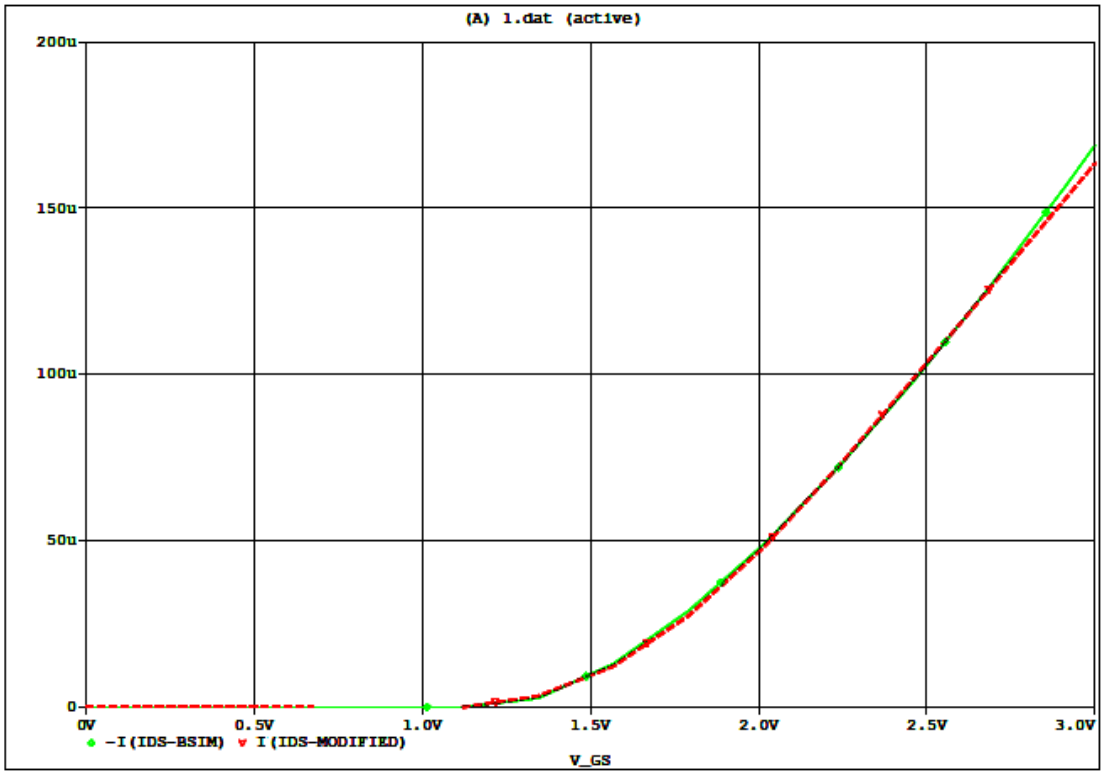


Figure 33A. I_{DS} modified level 1(- -) and level 7(—) for L=1 µm n-MOSFET.

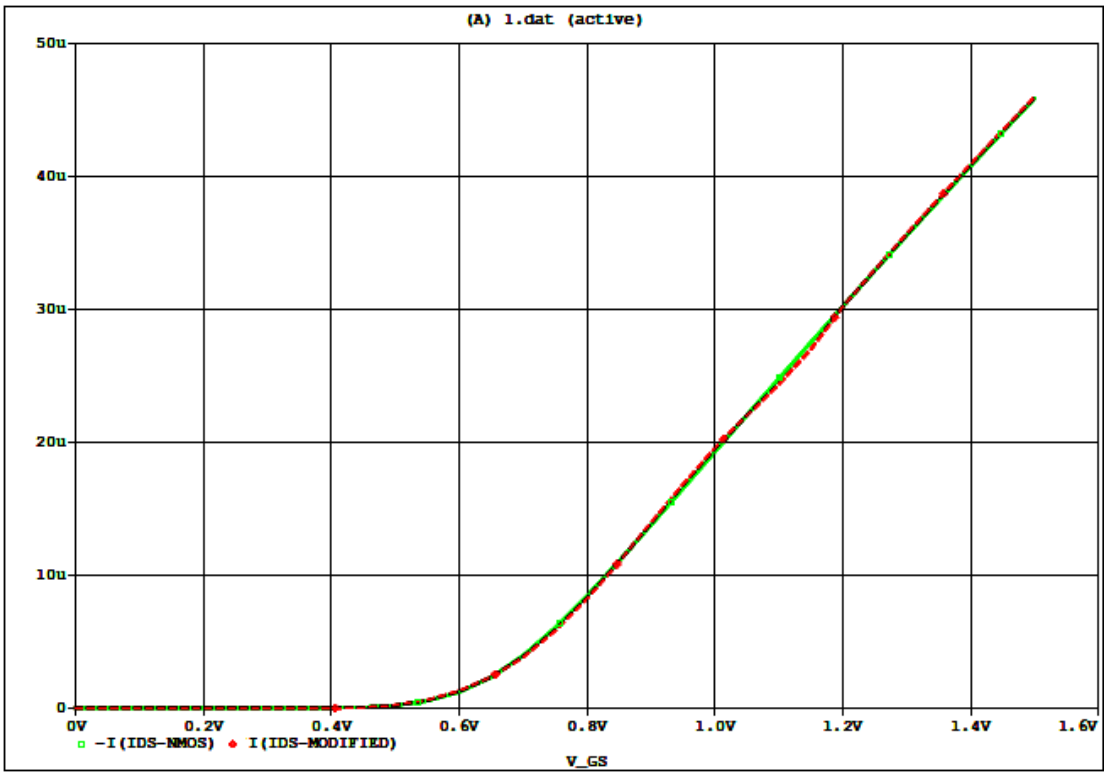


Figure 33B. I_{DS} modified level 1(- -) and level 7(—) for L=20 nm n-MOSFET.

3-2 Transistors Model of BSIM SWS-FET

Figure 34 shows Two Transistors (2-T) model of twin-drain n-SWS-FET. This circuit has two BSIM transistors T1 and T2, simulating Well-1 and Well-2 by two transistors respectively.

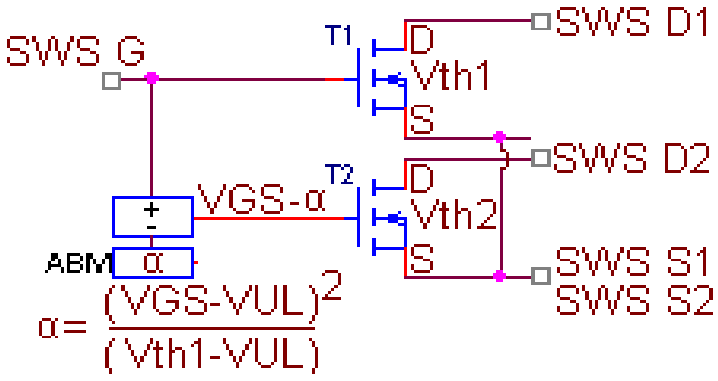


Figure 34. BSIM twin-drain SWS-FET model circuit.

The transistors T1 and T2 have of values of threshold voltages V_{th1} and V_{th2}. However, the threshold voltage of lower well (W2) transistor (T2) is adjust by α ($V_{dth2=}$ α + V_{th2}).

The matching parameter (α) changes as a function of gate voltage. This can be done by using the analog behavioral model (ABM), which first computes the matching parameter (α) and subtracts it from the value of V_{GS2}. The equivalent gate voltage is (V_{GS2} -α) for T2.

Figure 35A shows the simulation of the equivalent gate (V_{GS2} – α) as a function of the gate (V_{GS2}), this is an approximation to model SWS-FET with the following consideration:

- As the two transistors are connected in parallel, this results in the total gate oxide capacitance to be doubled. The actual SWS-FET gate capacitance is obtained by divided the 2-T capacitance by 2.
- The gate oxide capacitance for upper well W1 need to be modified as

$$C_{OX-W1}=(\frac{\varepsilon_{ox}}{tox}+\frac{\varepsilon_{well-1}}{t_{well-1}}+\frac{\varepsilon_{barrier-1}}{t_{barrierl-1}}+\frac{\varepsilon_{well-2}}{t_{well-2}}+\frac{\varepsilon_{barrier-2}}{t_{barrierl-2}})^{-1}$$ [8-10].

- The effective gate to source voltage of T2 is adjusted by α instead of the threshold voltage ($V_{dth2=}V_{th2}$ + α).

The advantage of using BSIM models is that they can scale to 45 nm and 25 nm with capturing the latest technology advances [11-12]. This approach can capture the basic SWS-FET behavior.

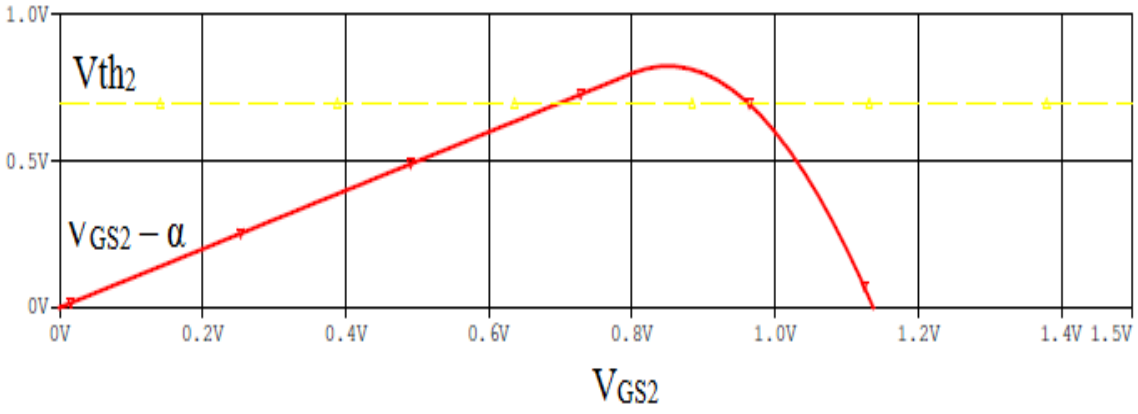


Figure 35A. The simulation of L=1um twin-drain n-SWS-FET (V_{GS2} – α) of W_2.

Figure 35B shows Cadence simulation of the lower well is on (I_{DS-W2} >0) if $V_{GS} - \alpha > V_{th2}$ or $V_{GS} > V_{th2} + \alpha$, this occurs when $V_{GS} - \alpha = V_{TH2}$. And upper well is no ($I_{DS-W2}$ >0) when $V_{GS} > V_{th1}$ as conventional n-MOSFET. The model parameters are same as Table 9 with V_{DD}=5V, V_{TH1}=0.9V, V_{UL}=0.85V, V_{TH2}=0.8V, L=1, W_1=2um, and W_2=5um.

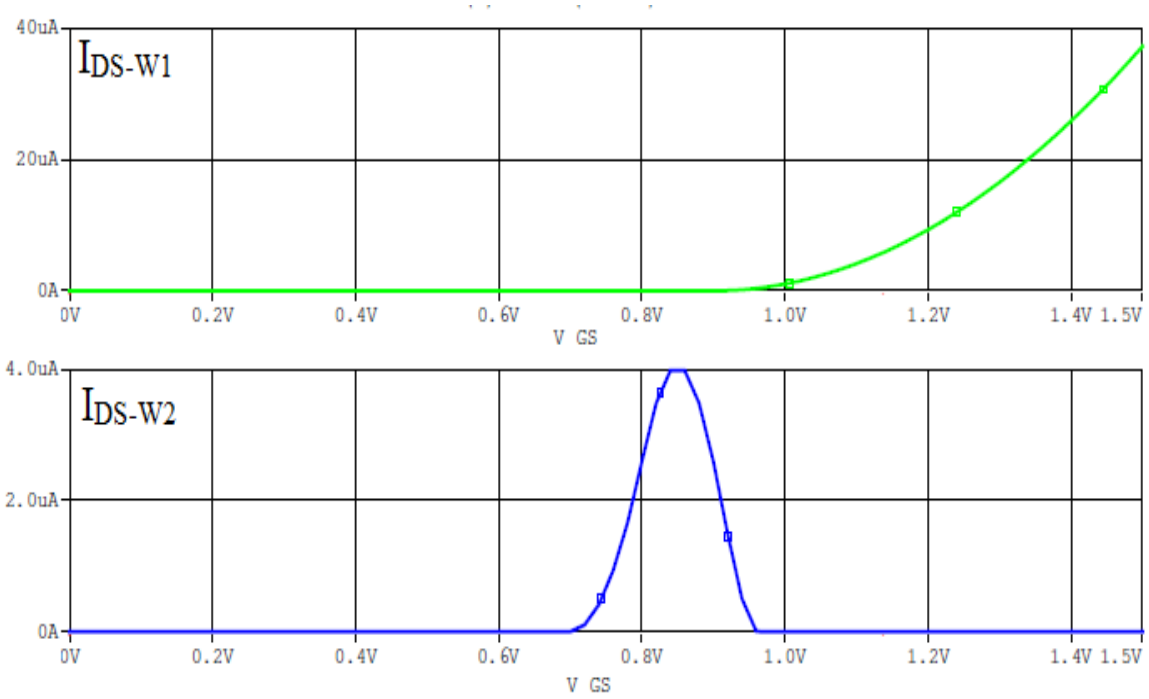


Figure 35B. The simulation of L=1 µm twin-drain n-SWS-FET I_{DS} W_1 (top) and W2 (bottom).

Figures 36 and 37 show Cadence simulation of $I_{DS-W1\&2}$ versus V_{GS} of 1um and 20nm twin-drain n-SWS-FET, respectively.

The twin-drain 20 nm channel length n-SWS-FET model have 230-parameters obtained using modeled BSIM4.6.0 level 7 Third Generation Model. The major parameters are (V_{DD}=1 V, V_{TH1}=0.3 V, V_{UL}=0.25 V, V_{TH2}=0.2 V, L=20 nm, W_1=40nm, and W_2=100nm) the full model parameters are shown in Appendix A. This 20 nm devices deliver small drain currents as the width for the upper and lower wells are set to minimum (2L and 5L). Increasing the wells width will enhance the current value.

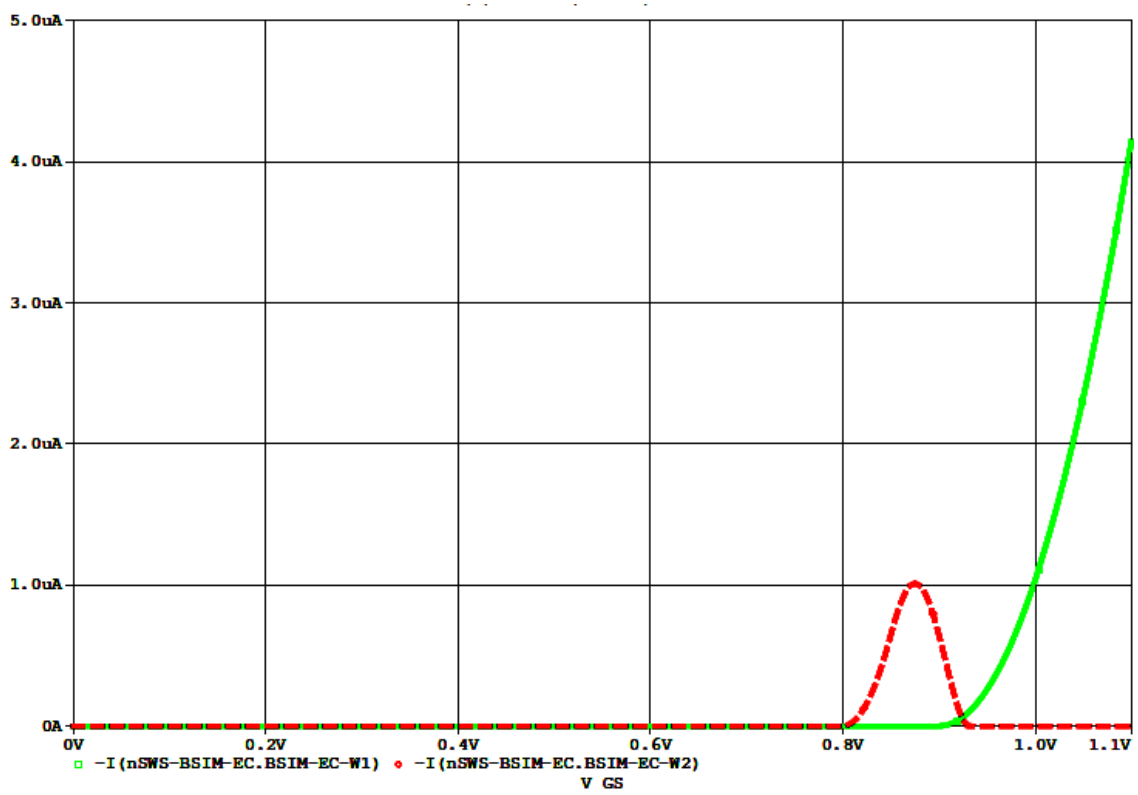


Figure 36. BSIM-2T twin-drain 1µm n-SWS-FET modeled $I_{DS\text{-}W2}$(- -) & $I_{DS\text{-}W1}$(—).

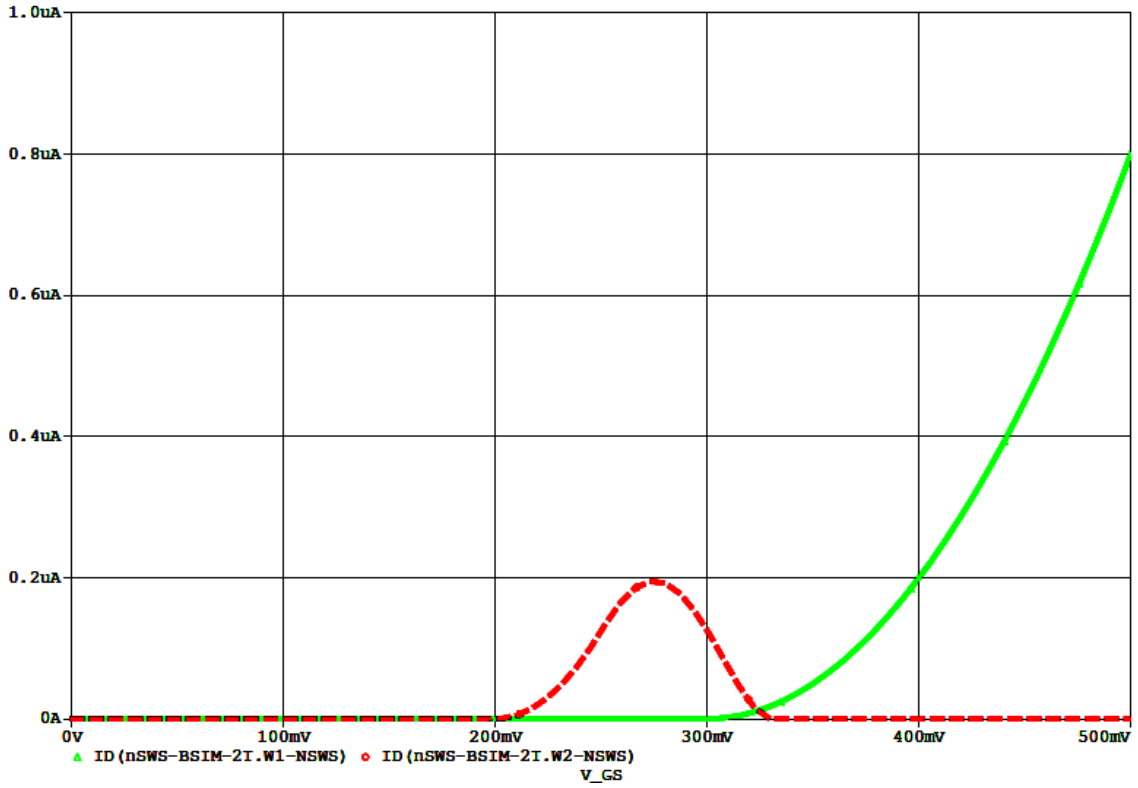


Figure 37. BSIM-2T twin-drain 20nm n-SWS-FET modeled $I_{DS\text{-}W2}$(- -)& $I_{DS\text{-}W1}$(—).

3-3 BSIM -Equivalent Circuit (BSIM-EC) for SWS-FET

The switching of n-MOSFET can be performed using the small and large -signal π models equivalent circuit at high frequencies. This is shown in Figure 38 [14-17]. The same is used for low frequency without account for terminal capacitances [18-19].

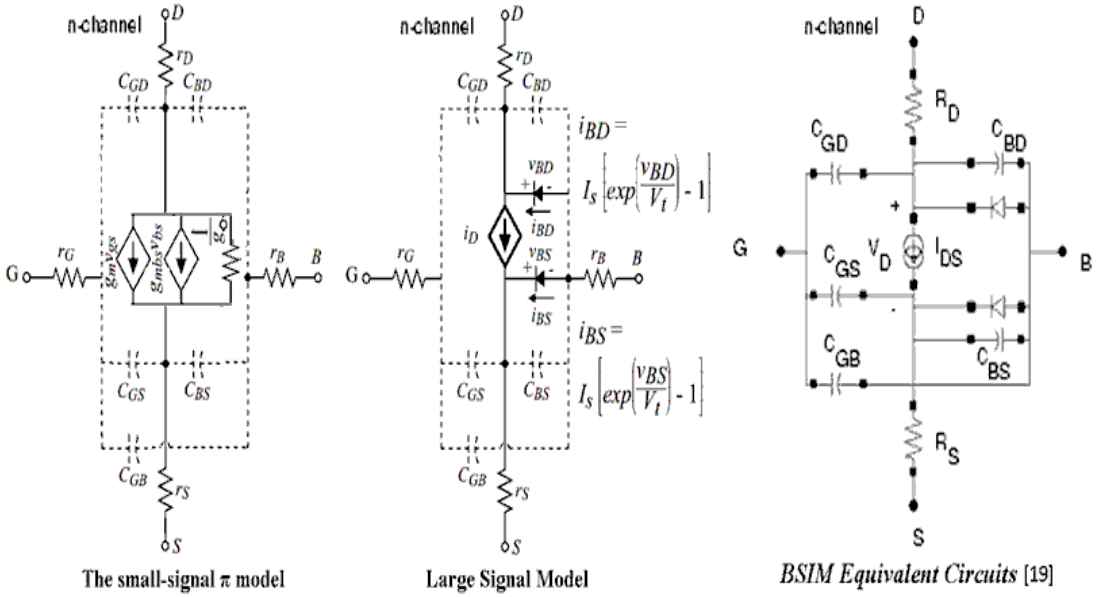


Figure 38. MOSFET Small and Large Signal Model.

The twin-drain n-SWS-FET can be modeled by using two BSIM equivalent circuits (BSIM-EC) as shown in Figure 39. ABM blocks are used to obtain the currents in different wells and nonlinear capacitances. The resistances (R_G, R_D, and R_S) will be calculated based on device geometry [11, 17, 19-20], I_{DS1} and I_{DS2} are obtained by extracting from BSIM Level 7 transistor models (using Equations 20 and 21), the currents model use nonlinear independent current sources. The capacitances (C_{GB}, C_{GD1}, C_{GS1}, C_{GD2}, C_{GS2}, C_{BD} and C_{BS}) are obtained from Meyer's capacitance model [21-22]. These are nonlinear capacitors [23], where C_{GDO} and C_{GSO} are the overlap capacitors.

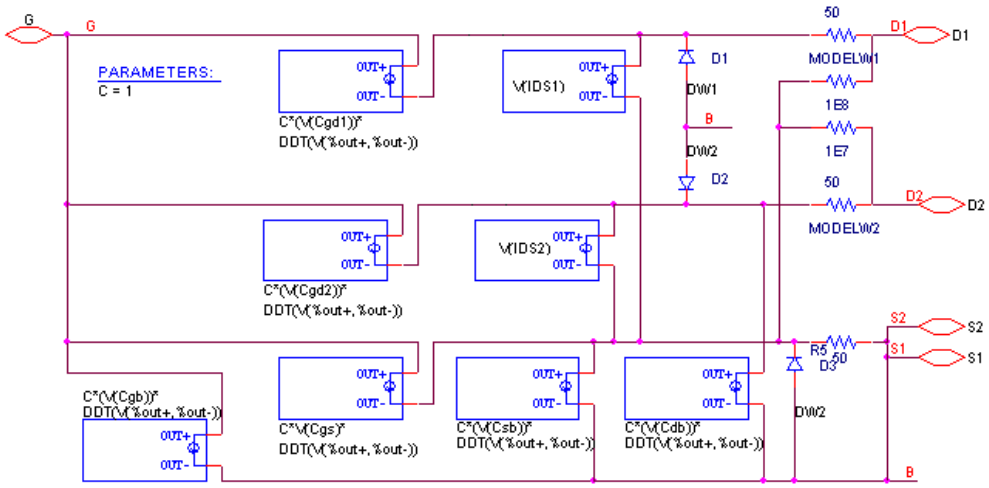


Figure 39. The model of the twin-drain SWS-FET by BSIM-EC.

Figures 40 and 41 show Cadence simulation of $I_{DS\text{-}W1\&2}$ versus V_{GS} of 1μm and 20nm twin-drain n-SWS-FET, respectively. The model capacitors are listed in Table 15 and Figures 42 and 43.

Table 15. The twin-drain n-SWS-FET capacitors (10^{-15} Farad) model.

L	W1	OFF	OFF	Sat.	Sat.	linear
	W2	OFF	Sat		OFF	
	C_{GB}	$C_{OX}L*W_2 + C_{GBOV}$	$C_{GBOV}= C_{OX}*W_d*L$			
	C_{GS}	$C_{GSOV} = C_{OX}*L_d*W_1$	$0.6C_{OX}L*W_2 + C_{GSOV}$	$0.6C_{OX}L*W_1 + 0.6C_{OX}L*W_2+C_{GSOV}$	$0.6C_{OX}L*W_1 + C_{GSOV}$	$0.5C_{OX}L*W_1 + C_{GSOV}$
	C_{GD1}	$C_{GDOV} = C_{OX}*L_d*W_1$				$0.5C_{OX}L*W_1 + C_{GDOV}$
	C_{GD2}	0				
	C_{SB}	$\frac{C_J * AS}{(1+V_{SB}/PB)^{MJ}} + \frac{C_{JSW} * PS}{(1+V_{SB}/PB)^{MJSW}}$, Note $V_{SB} = 0V$				
	C_{DB}	$\frac{C_J * AS}{(1+V_{D1B}/PB)^{MJ}} + \frac{C_{JSW} * PS}{(1+V_{D1B}/PB)^{MJSW}}$, Note $V_{D1B} = V_{DD}$				
1um	C_{GB}	6.875	0.74			
	C_{GS}	0.650	5.662	7.57	2.554	0.650
	C_{GD1}	0.650				2.08
	C_{GD2}	0				
	C_{SB}	4.89 ,Note V_{SB}=0V				
	C_{DB}	1.525 ,Note V_{D1B}=V_{DD}=5V				
20nm	C_{GB}	21.17E-3	0.450E-3			
	C_{GS}	18.69E-3	39.41E-3	46.31E-3	25.60E-3	23.87E-3
	C_{GD1}	18.69E-3				23.87E-3
	C_{GD2}	0				
	C_{SB}	82.62E-3,Note V_{SB}=0V				
	C_{DB}	065.58E-3 ,Note V_{D1B}=V_{DD}=1V				

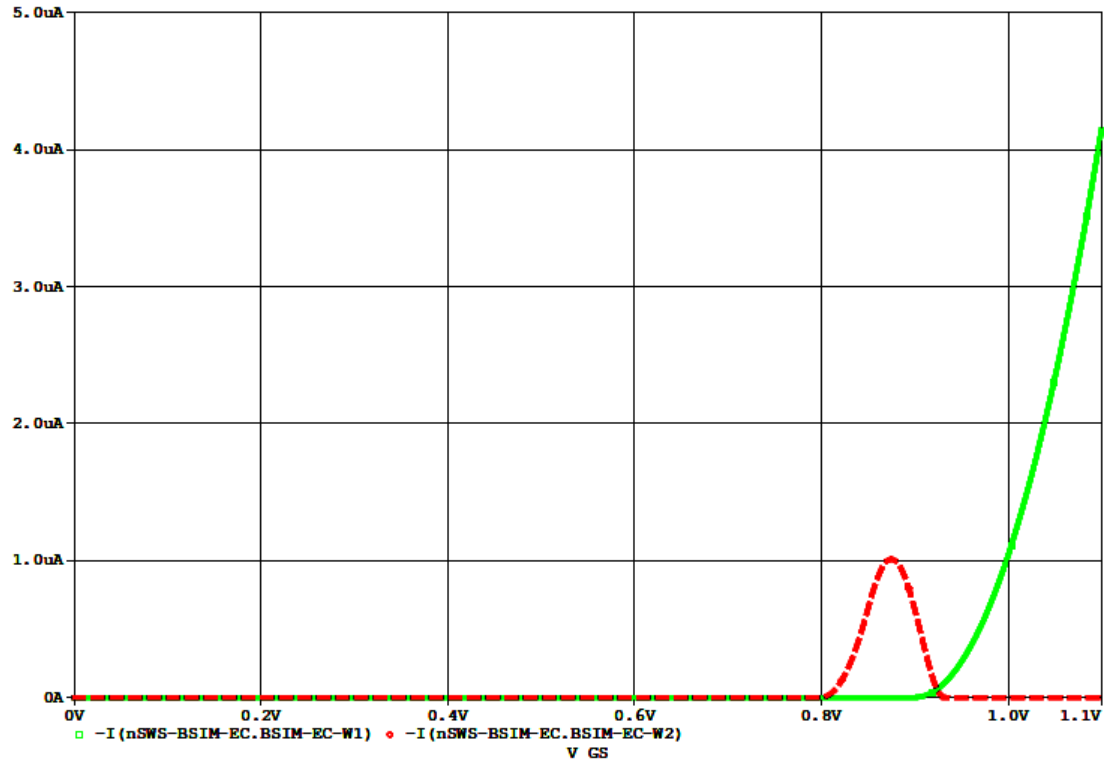


Figure 40. BSIM-EC twin-drain 1um n-SWS-FET modeled $I_{DS\text{-}W2}$(- -) & $I_{DS\text{-}W1}$(—).

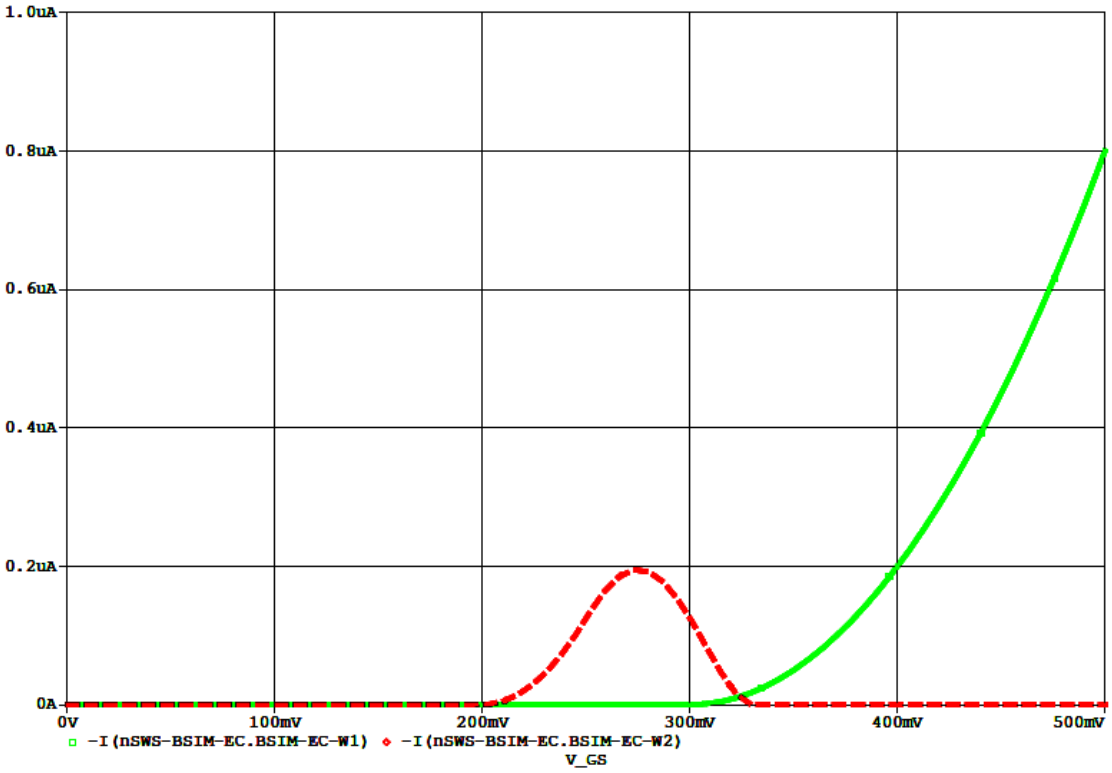


Figure 41.BSIM-EC twin-drain 20nm n-SWS-FET modeled $I_{DS\text{-}W2}$(- -)&$I_{DS\text{-}W1}$(—).

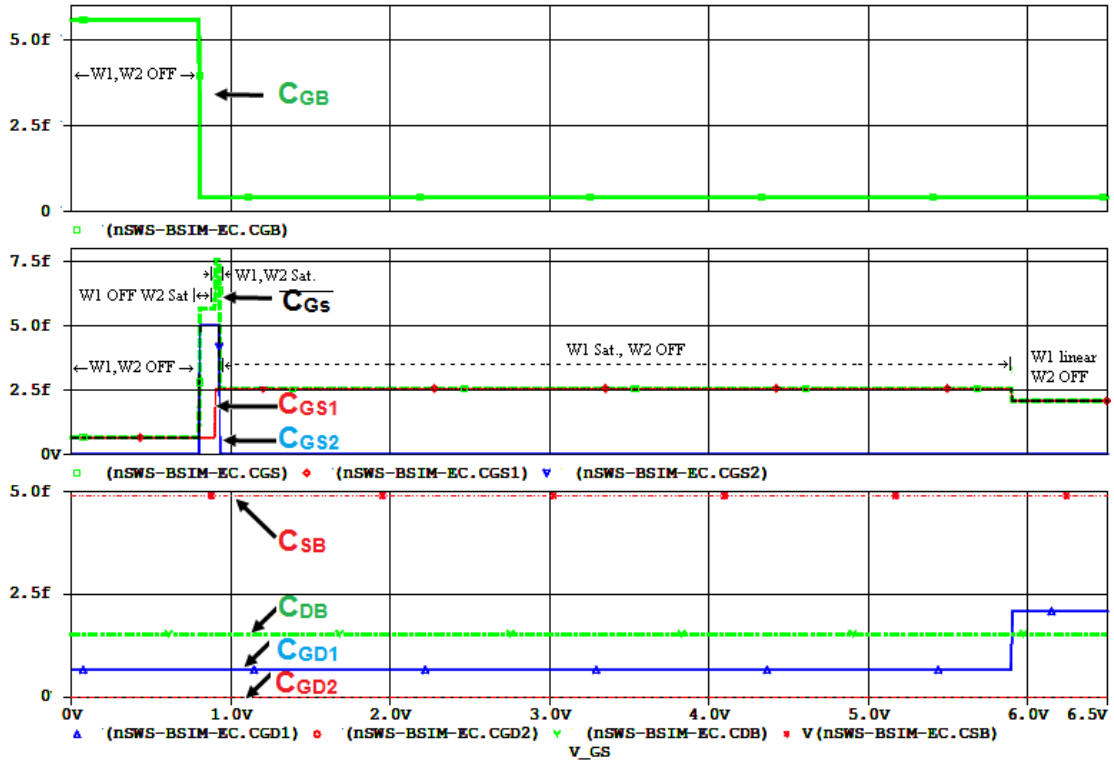


Figure 42. BSIM-EC twin-drain 1 µm n-SWS-FET capacitors (Farad) model.

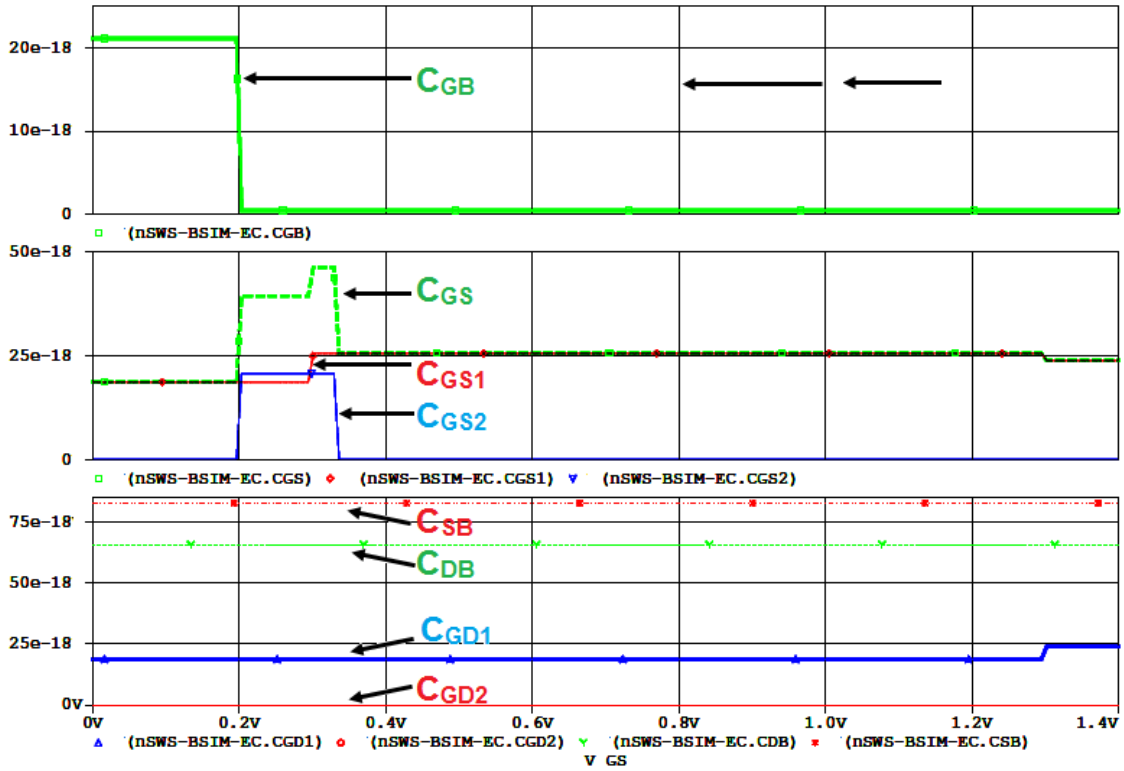


Figure 43. BSIM-EC twin-drain 20nm n-SWS-FET capacitors (Farad) model.

3-4 Integration between BSIM Transistor and BSIM Equivalent Circuit for SWS-FET

The circuit is an integration between both circuit BSIM Transistor and HF Small Signal Model, the Well-1 is represented by BSIM transistor T1 and Well-2is implemented by the BSIM HF Small Signal model as shown in Figure 44. This circuit provides the accurate modeling of SRAM SWS-FET (showing in Figure xxx chapter 4). Figure 45 A and B show 1 µm and 20 nm channel length n-SWS-FET device, respectively

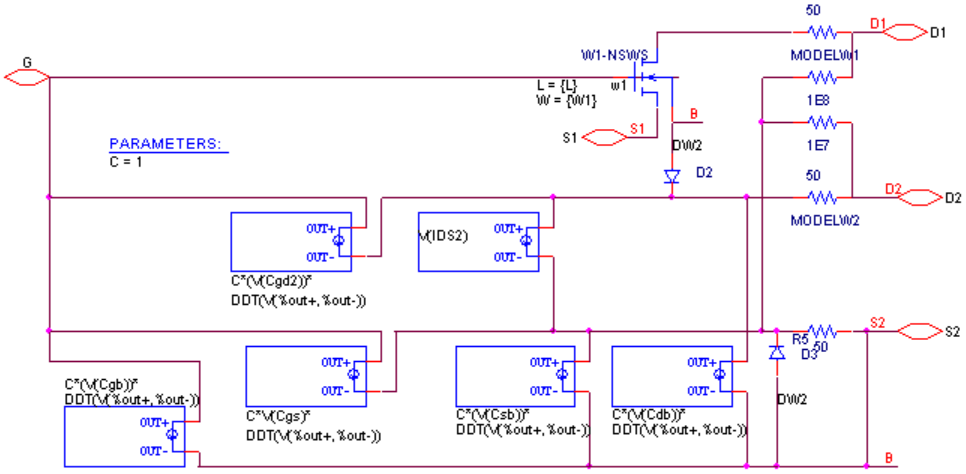


Figure 44. n-SWS model by BSIM transistor & equivalent circuit (BSIM 1T&EC).

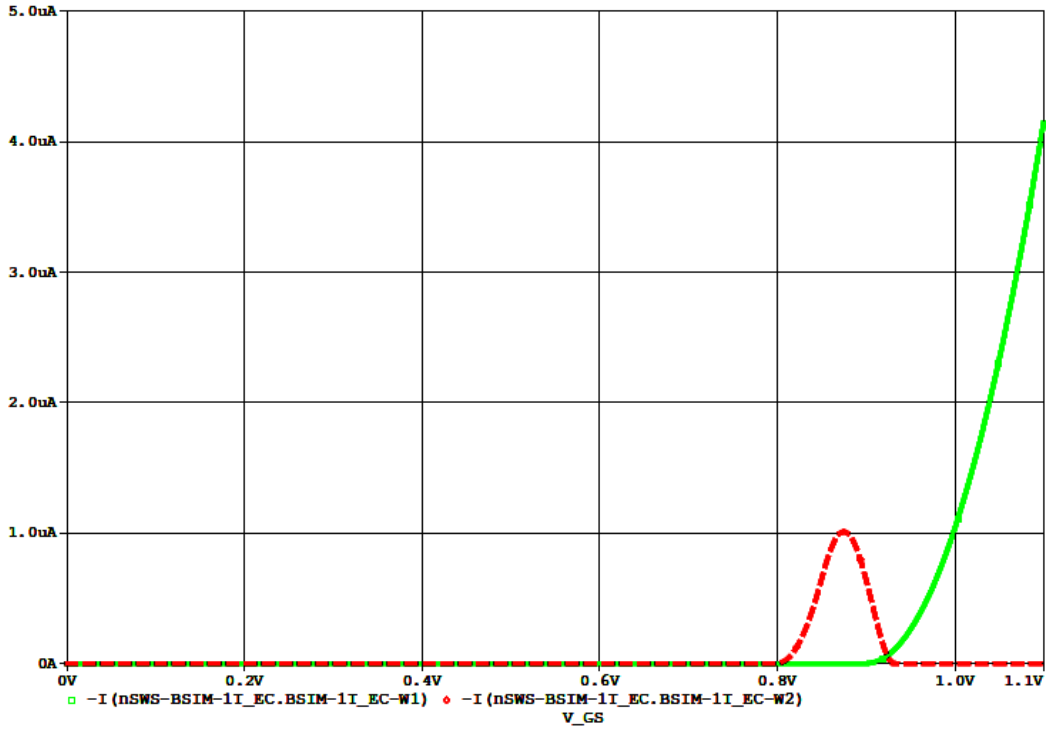


Figure 45A. BSIM-1T&EC L=1µm n-SWS-FE [I_{DS-W2} (- -),I_{DS-W1}(—)].

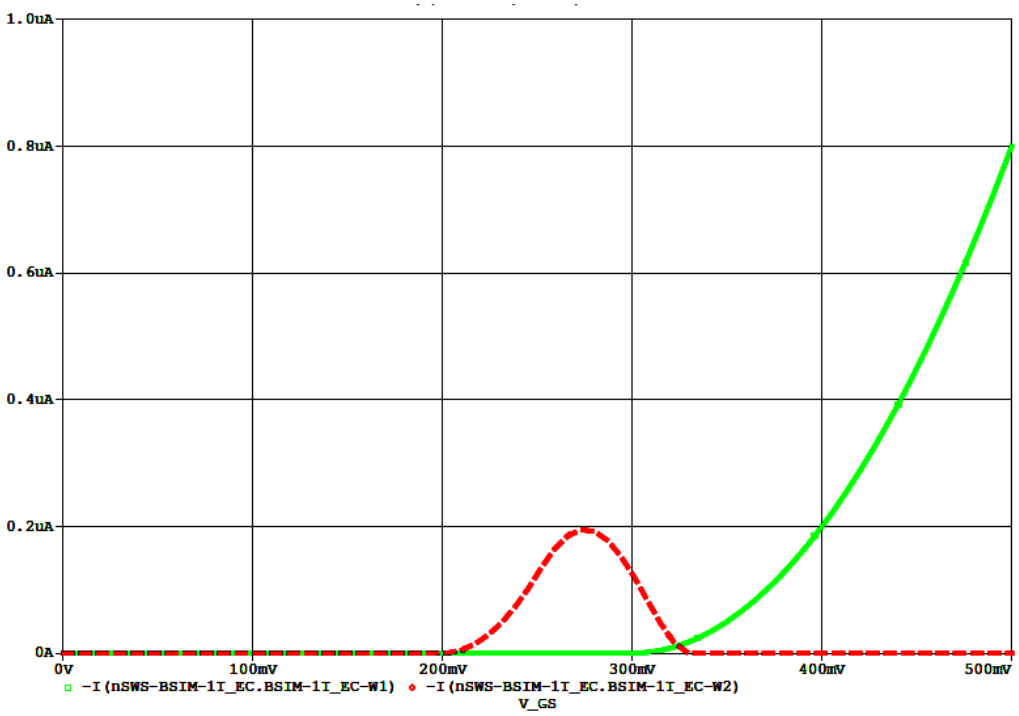


Figure 45B. BSIM-1T&EC L=20nm n-SWS-FE [$I_{DS\text{-}W2}$ (- -),$I_{DS\text{-}W1}$(—)].

3-5 The Transconductances (g_m) Simulations.

The circuit in Figure 46 is used to measure g_m in SWS-FET model. The calculations of g_m are performed for Well-1 and 2 as shown in Figure 47 (1um n-SWS-FET) and Figure 48 (20m n-SWS-FET). The figures show g_m for W2 have the same switching functionality as the drain current in W2 and g_m for upper W1 are similar to a conventional n-MOSFET.

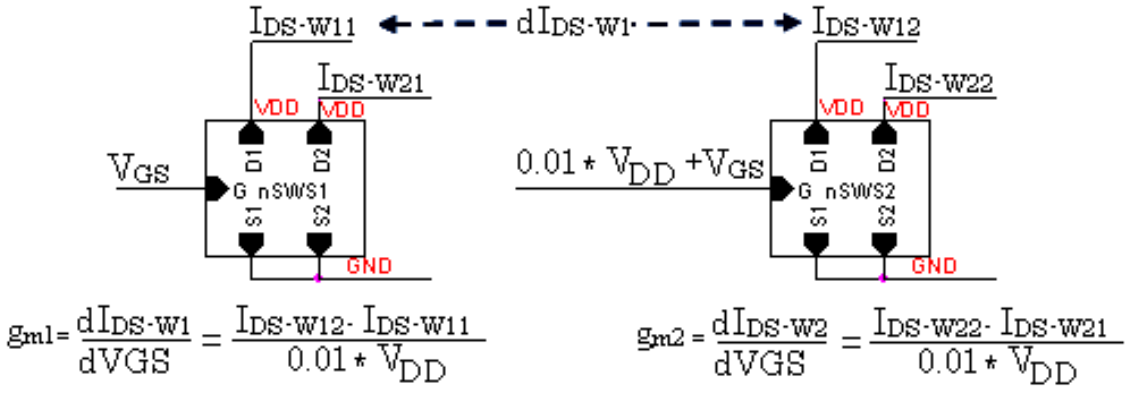


Figure 46. The circuit for evaluating gm for the twin-drain n-SWS-FET.

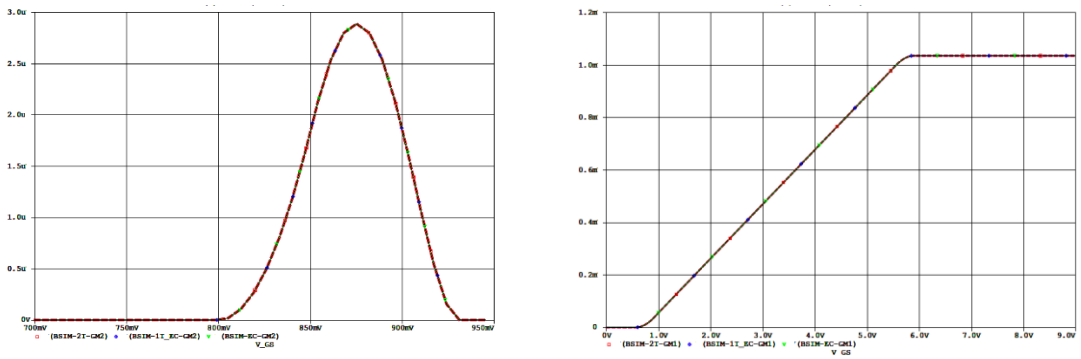


Figure 47. The twin-drain 1 μm n-WS-FET,
$g_{m\text{-}W2}$ (left) and $g_{m\text{-}W1}$ (right).[Unit A/V].

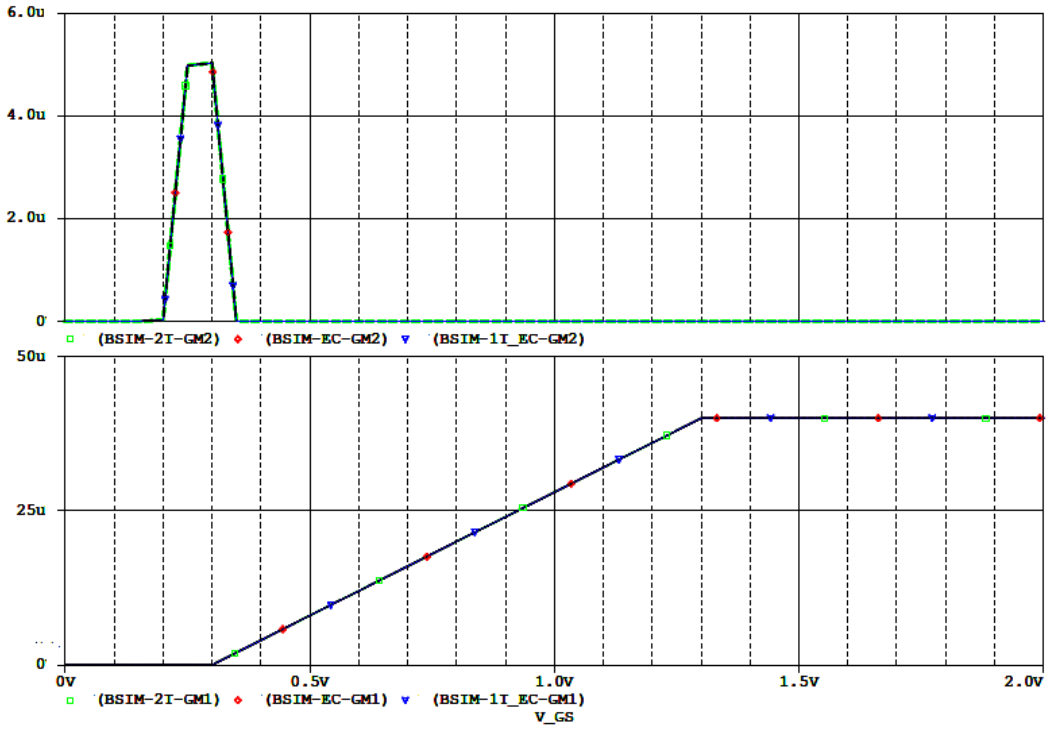


Figure 48. The twin-drain 20nm n-WS-FET,
$g_{m\text{-}W2}$ (top) and $g_{m\text{-}W1}$ (bottom).[Unit A/V].

4 SWS-FET APPLICATIONS

4-1 Logic Gates Circuit Using n-SWS-FET

Complementary MOS (CMOS) uses PMOS and NMOS transistors to implement any Boolean functions [14]. This section shows the design possibilities of logic gates using only n-SWS-FETs. The truth table for the various logic gates is presented in Table 16.

The Inverter design uses two n-SWS-FETs [1] is shown in Figure 49A. When the input V_{IN} is 0, the lower wells SWS 1 and 2 are in the conducting mode whereas D2 of SWS1 connects the output to V_{DD} (logic 1). As V_{IN} is changed to 1, the upper wells of SWS 1 and 2 are in the conducting mode where D1 of SWS 2 connects the output to ground (logic 0). Figure 49B shows the conducting paths (green lines) of each gate input [24].

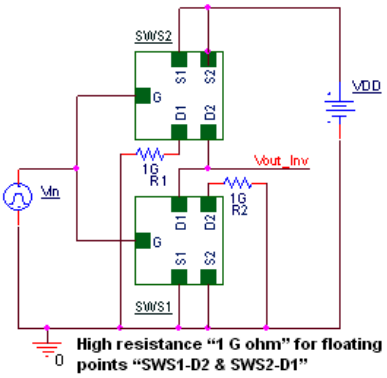


Figure 49A. n-SWS-FET Inverter.

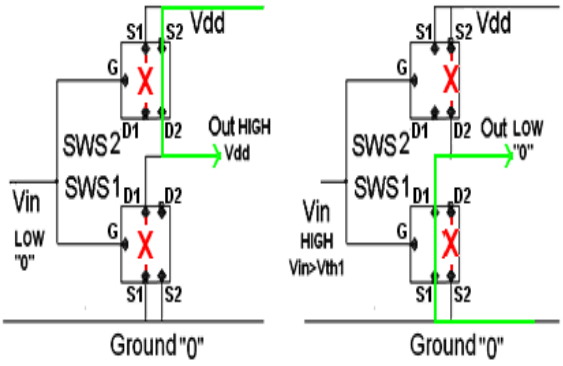


Figure 49B. Operation in n- SWS-FET Inverter

Table 16. The truth table for the implemented logic gates.

INPUT1 A	INPUT2 B	INVERTER $\bar{A}$	NAND $\overline{A.B}$	NOR $\overline{A+B}$	XOR $A \oplus B = \bar{A}.B + A.\bar{B}$	XNOR $A \odot B = \overline{A.B} + A.B$
0	0	1	1	1	0	1
0	1	1	1	0	1	0
1	0	0	1	0	1	0
1	1	0	0	0	0	1
No. of CMOS transistors needed		1-PMOS 1-NMOS	2-PMOS 2-NMOS	2-PMOS 2-NMOS	16T By 4-NAND	16T By 4-NOR
					8T by Transmission Gate [25],[26]	
No. of SWS-FET transistors		2	3	3	6	4

n-SWS-FET NAND logic gates can be realized simply by inverting one input and supply it to n-SWS-FET well 1, the well 2 is connected to V_{DD}. Figure 49C shows the NAND circuit and simulation result. Also, n-SWS-FET AND are made by adding other inverter to n-SWS-FET NAND [24].

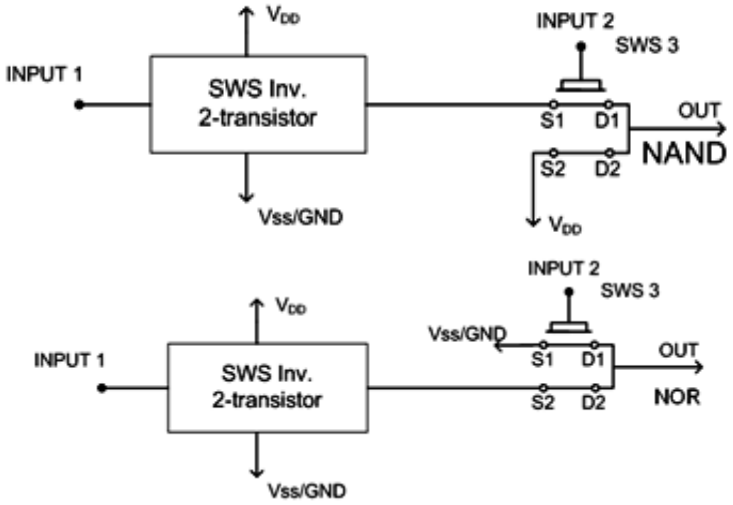


Figure 49C. Two input n-SWS-FET NAND (top) and NOR (bottom) circuit

n-SWS-FET NOR gate design includes one SWS inverter and one n-SWS-FET in twin-source configuration shown in Figure 49C, meanwhile OR circuit is inverted of NOR.

Figure 49D shows the XNOR circuit has four n-SWS-FETs that perform the function of XNOR and XOR performs by XNOR with one more SWS- Inverter [24]. [24].

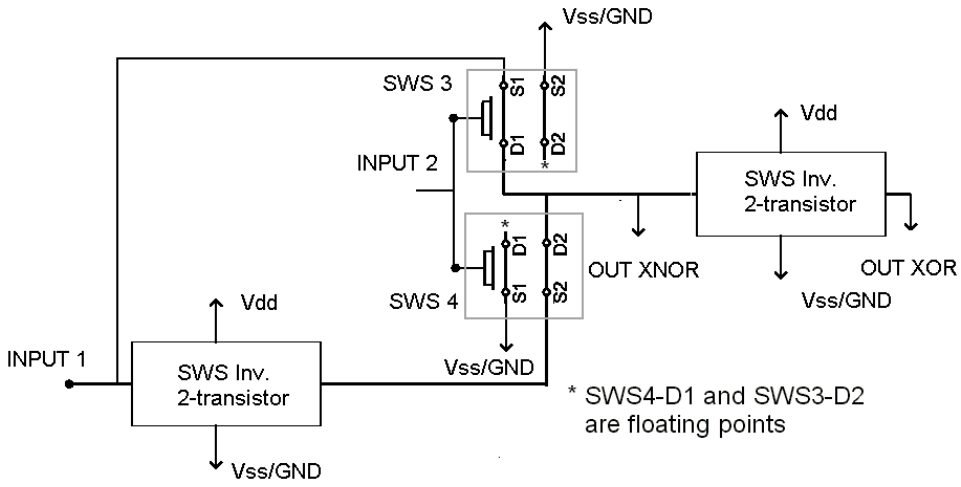


Figure 49D. Two input n-SWS-FET XNOR and XOR circuits

Figure 50 shows the circuit designs of inverter, NAND, NOR and XNOR gates using SWS-FETs. Based on truth table the conducting paths of each gate are marked in red dotted lines

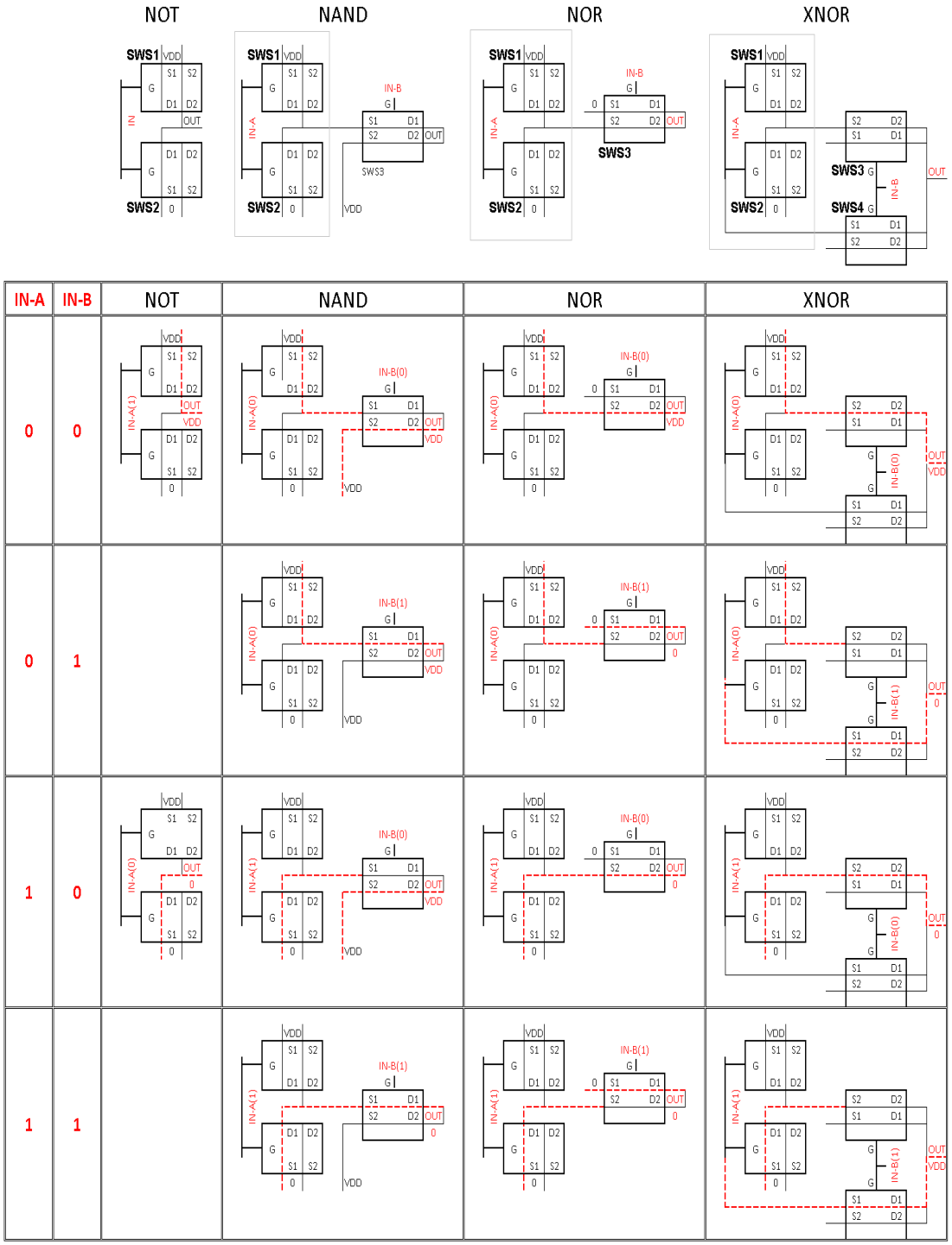


Figure 50. n-SWS-FET logics circuits.

* The circuits of NOT, NAND and NOR established by Jain et al. [1,24].

4-2 Memories Circuit Using n-*SWS*-FET

4-2-1 D Latch Flip Flop (One Bit Delay) Using n-SWS-FET

Four SWS-NAND gates are used to perform function of D Latch Flip flop which is also called One Bit Delay. Figure 51 presents the schematic circuit of the D Latch flip flop and Table 17 shows the truth Table [27].

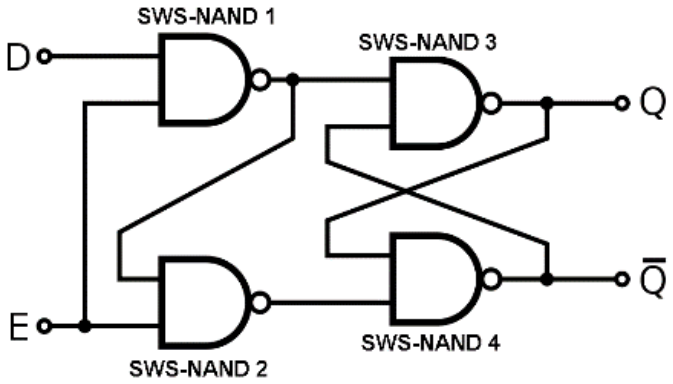


Figure 51. SWS-D Latch Flip Flop circuit.

Table 17. The D Latch flip flop truth table.

INPUT CK	INPUT D	OUTPUT Q	OUTPUT Q-BAR
0	0	keep state	keep state
0	1	keep state	keep state
1	0	0	1
1	1	1	0
No. of CMOS transistors are needed		4*2 PMOS + 4*2 NMOS= 8 PMOS + 8 NMOS =16 CMOS	
No. of SWS-FET transistors are needed		4*3 n-channel SWS-FET = 12 n-channel SWS-FET	

4-2-2 SWS-FET SRAM Circuits

Conventional SRAM consists of two Conventional-Coupled COMS Inverter for the memory implementation. The 6T circuit has two coupled inverter and two n-MOSFET access transistors as shown in Figure 52A [28]. M1, M2, M3 and M4 transistors make a pair of inverters, connected in a loop. The other transistors M5 and M6 are used to control read and write. The 8T circuit of Figure 52B has two more n-MOSFET to prevent the data from being disturbed during a read operation [28], the truth table of the SRAM shown in Table 18.

Table 18. Standard SRAM truth Table.

Write signal	Data signal	Stored Data
0	0	Same State
0	1	Same State
1	0	0
1	1	1

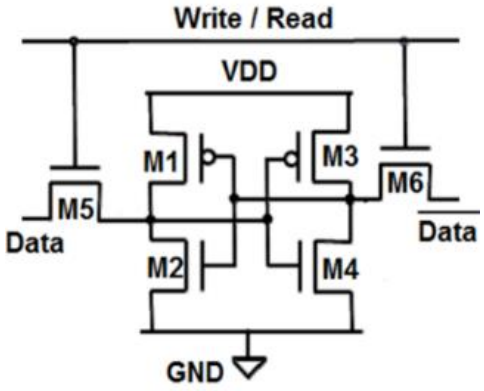


Figure 52A. CMOS SRAM 6T cell.

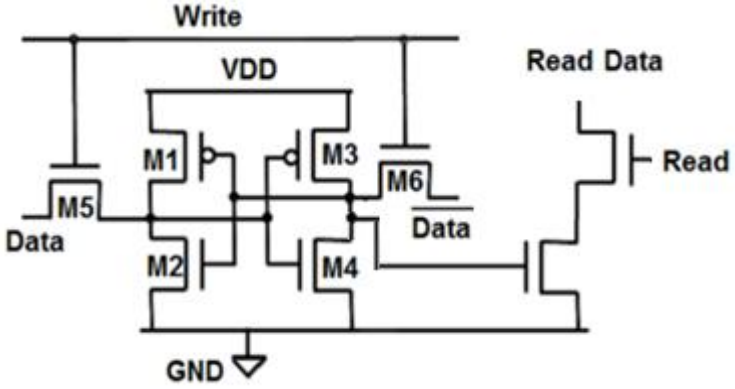
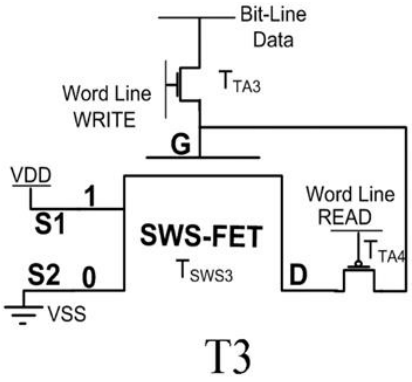


Figure 52B. CMOS SRAM 8T cell.

SRAM circuits using a signal SWS-FET (T3 in Figure 53A, T4 in Figure 53B) that were first developed by Jain et al [29-32]. The circuit of Figure 53A works like a conventional 6T circuit. The circuit of Figure 53B has two conventional access transistors n-MOSFET (T_{A5}) and p-MOSFET (T_{A6}) for the write operation and one n-MOSFET (T_{A7}) for the read operation. This circuit is similar to CMOS using T8. In this circuit, SWS-FET (T_{SWS4}) works as memory cell and the source S1 and S2 are connected to the power supply (V_{DD}) and ground (GND) respectively.

For the write operation, cell is accessed by turning ON T_{A5} and turning OFF T_{A6}. In this case the data is passed to gate of T_{SWS4} then to drain of T_{SWS4}. When the write signal became low (disappear) T_{A5} turns OFF and T_{A6} turns ON, and this conduction provides a loop between T_{SWS4} drain, T_{A6} and T_{SWS4} gate. The loop lets the data to store.

For the read operation T_{A7} turns ON and the stored data passes to the data line.



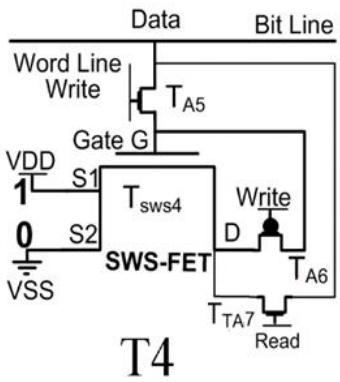
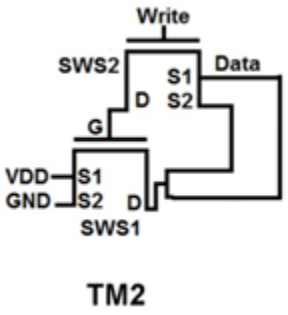


Figure 53A. T3 SWS-FET SRAM [32]. **Figure 53B. T4 SWS-FET SRAM [32].**

Figures 54A and 54B show a modification of SRAM in Figures 53A and 53B respectively. The modification reduces the number of transistors by one in each circuit. Here, the access transistors T_{A5} and T_{A6} are replaced by one SWS-FET (T_{SWS2}) to perform the writing operation [33].



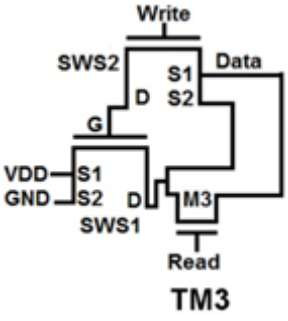
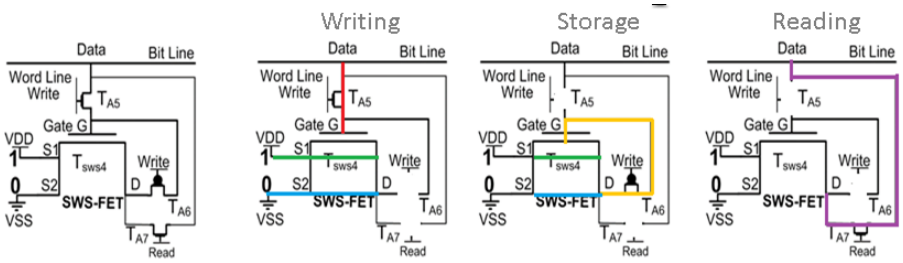


Figure 54A. TM3 SWS-FET SRAM [32]. **Figure 54B. TM4 SWS-FET SRAM [32].**

Figure 55 illustrations the write-stored-read operations of modified SWS-FET SRAM circuit. For the write operation, cell is accessed by applying V_{DD} to the gate of SWS2, this connects source 1 (S1) to drain (D) for SWS2. In this case the data is passed to gate of SWS1 then to drain of SWS1. When the write signal became low source 2 (S2)

connecting to drain (D), and this conduction provides a loop between SWS1 and SWS2 which lets the data to store.



Writing

The write signal is high (TA5 ON and TA6/7 OFF)

- Date is passed to TSWS4 gate (G)
- Data (1) => TSWS4 (D) (1)
- Data (0) => TSWS4 (D) (0)

Storage

The write signal is low (TA5/7 OFF and TA6 ON)

- Loop TSWS4 (D)- TA6 and TSWS4(G)
- Data (1) => TSWS4 (D) (1) or Data (0) => TSWS4 (D) (0)

The loop enables the data to be stored.

Reading

TA7 turns ON and the stored data passes to the data line.

Figure 55. The operations of modified SWS-FET SRAM circuit.

4-3 Half-Adder Circuit Using SWS-FET.

Figure 56 shows the one-bit Half-Adder circuit. The truth table of a one bit Half-Adder is shown in Table 19. In CMOS Half-Adder the circuit has 22 transistors (16 for XOR plus 4 for NAND and 2 for NOT). But the circuit for SWS-FET has 11 n-channel-SWSFET transistors (6 transistors for XOR, 3 transistors for NAND and 2 for NOT) [24].

Table 19. the truth table for a half adder

A	B	SUM=A XOR B	CARRY= A AND B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1
No. of CMOS transistors 22 T		16 T	4 for NAND+ 2 for NOT=6T
No. of SWS transistors 11 T		6 T	3 for NAND+ 2 for NOT=5T

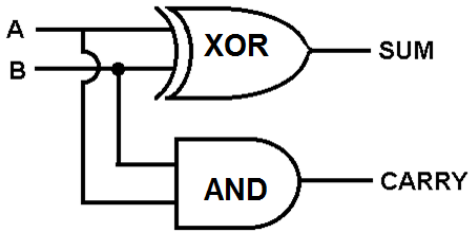


Figure 56. The Half-Adder circuit.

4-5 3-Bit Flash Analog-to-Digital Converter (ADC) Circuits Using SWS-FET.

The design of 3-bit flash Analog-to-Digital Converter (ADC) using n-SWS-FETs is implemented in two different architectures [17, 39] as shown in Figure 57 and 58. In architecture I, one three-well n-SWS-FET is used to design a 3-bit ADC. This architecture senses the current levels in different channels using 6 CMOS inverters. In the architecture II, the main idea is to change the threshold voltages of the two channels of the n-SWS-FET by adding two different source voltages to the n-SWS-FET sources. This design has 8 n-SWS-FETs and two CMOS current comparators. Both architectures I and II have a smaller device count than would be required to perform the ADC function implemented with a conventional CMOS circuit. The conventional circuit would need (2^3-1=7) Threshold Inverter Quantization (with different W/L) and more than 7 CMOS inverters to work as voltage comparator (7+7=14 n-MOSFET and 7+7=14 p-MOSFET) as shown in Figure 59.

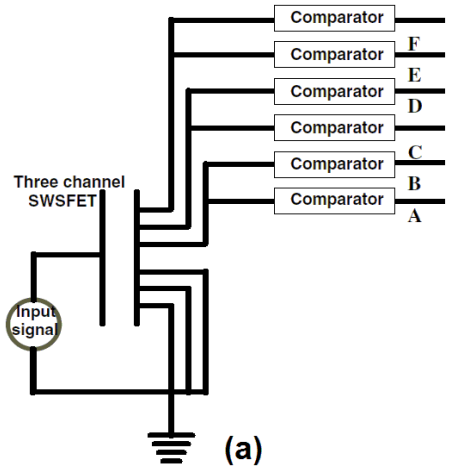


Figure 57. n-SWS-FET 3-Bit Flash ADC Architecture I.

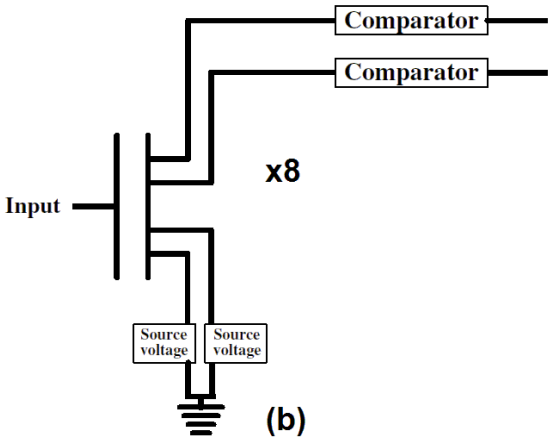


Figure 58. n-SWS-FET 3-Bit Flash ADC Architecture II

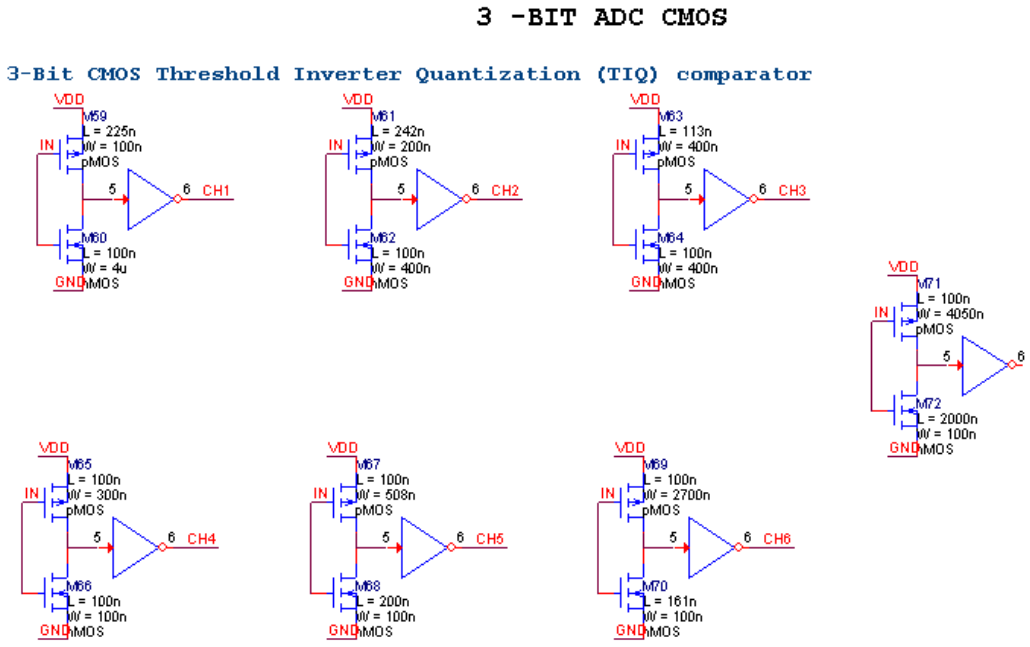


Figure 59. CMOS 3-Bit Flash ADC.

A 3-bit ADC design integrating complementary SWS-FETs (e.g. a two-well n-SWS-FET and p-SWS-FET) is shown in Figure 60. This design has 6 SWS-FET transistors (four n-SWS-FET and two p-SWS-FET). The circuit works as a voltage comparator.

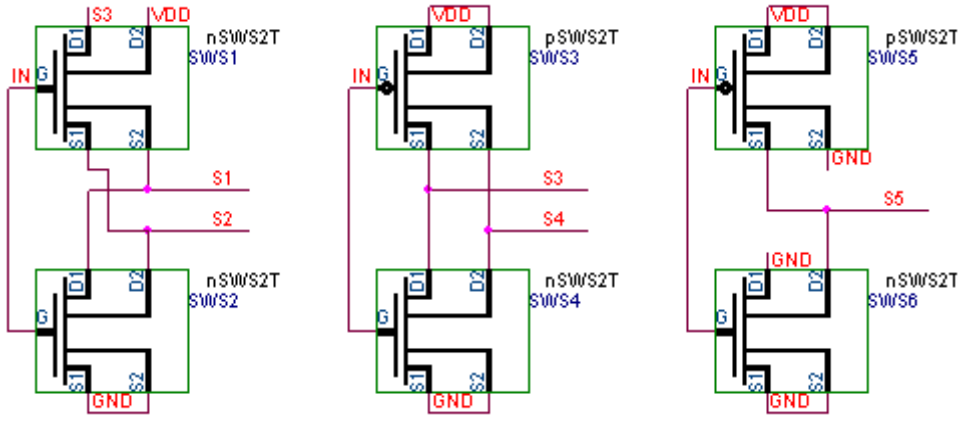


Figure 60. 3-Bit Flash ADC comparator using n- and p- SWS-FET.

In the ADC design, the outputs S_1 to S_5, selected by the magnitude of input analog signal applied, change between V_{DD} or V_{SS} (0). This is provided by the switching properties of SWS-FETs. The S_1-S_5 outputs are fed to encoder. Figure 61 shows an encoder

circuit using n-SWS-FET gates. The SWS encoder is designed by 26 n SWS-FET. The same encoding circuit are implanted by 46 CMOS transistors (22 n-MOSFET and 22 p-MOSFET) as shown in figure 62. The number of the FETs is reduced from 74 in conventional CMOS architecture to 32 using complementary SWS as showing in Table 20.

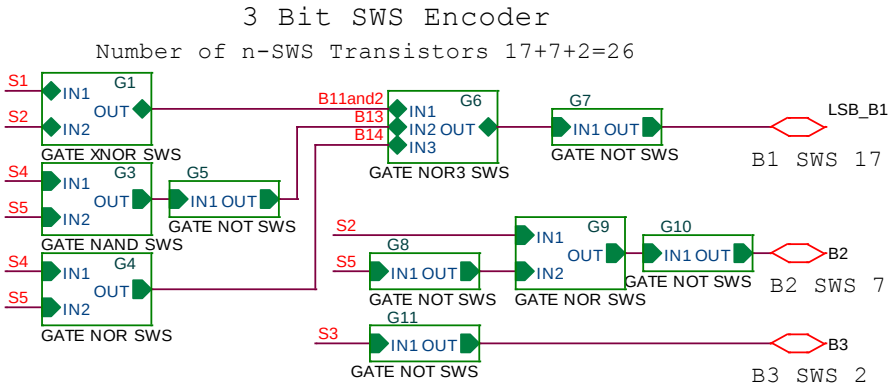


Figure 61. 3-Bit ADC encoder using n-SWS-FET.

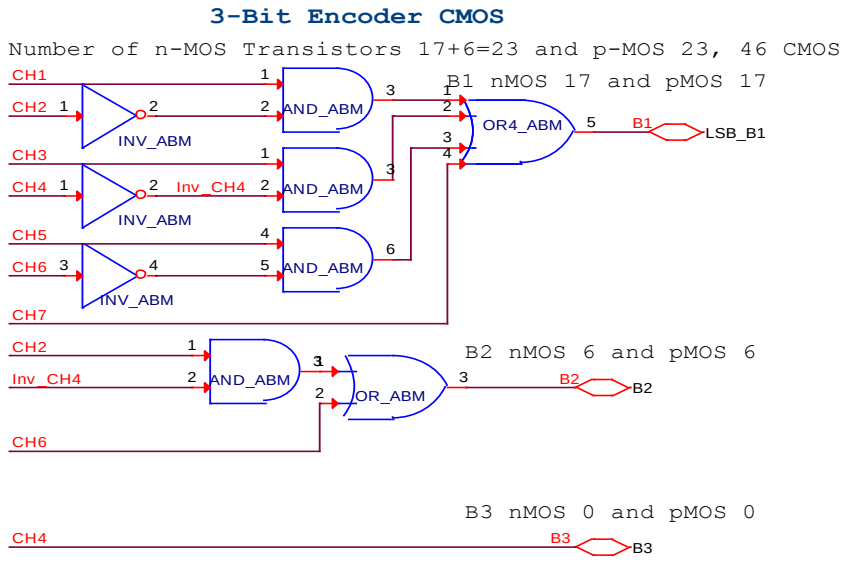


Figure 62. 3-Bit ADC encoder CMOSFET

Table 20. The number of transistors for SWS-FET and CMOS.

Circuit	Reduction % $1-\frac{Total_{SWS}}{Total_{CMOS}}$	CMOS			n- p- SWS-FET		
		n-FET	p-FET	Total	n-SWS-FET	p-SWS-FET	Total
3-Bit ADC Comparator	78.5%	14	14	28	4	2	6
3-Bit ADC Encoder	43.5%	23	23	46	26	0	26
3-Bit ADC	56.7%	37	37	74	30	2	32

5 SIMULATION OF LOGIC GATES, SRAM'S, AND ADC'S USING SWS-FET

In this section, the performance of logic gates, half adder, D latch, SRAM, and 3-Bit flash ADC circuits is investigated using Cadence-OrCAD CIS v16.5 simulator. BSIM-Two-Transistors (BSIM-2T) model is used for the simulations of SWS-FET logic gates, SWS-FET Half-Adder and SWS-FET D latch, and 3-Bit flash ADC. SWS-FET SRAMs are simulated using BSIM Transistor and BSIM -Equivalent Circuit (BSIM-1T&EC).

5-1 The simulation of Logic Gates Circuit Using n-SWS-FET

Figure 63A illustrates the simulation of L=5 μm n-SWS-FET inverter (circuit in Figure 49A) and CMOS inverters. The top figure is the input of the inverts (COMS and SWS-FET), while the bottom is the outputs of the COMS inverter (dish line) and the output of SWS-FET inverter (solid line). The simulation shows the n-SWS-FET inverter has voltage drop when the input voltage is V_{DD} which does not appear in CMOS because p-MOSFET has low drop-out voltage when it is on. Where n-SWS- FET is n-channel transistor which has lower R_{DS} when it is on.

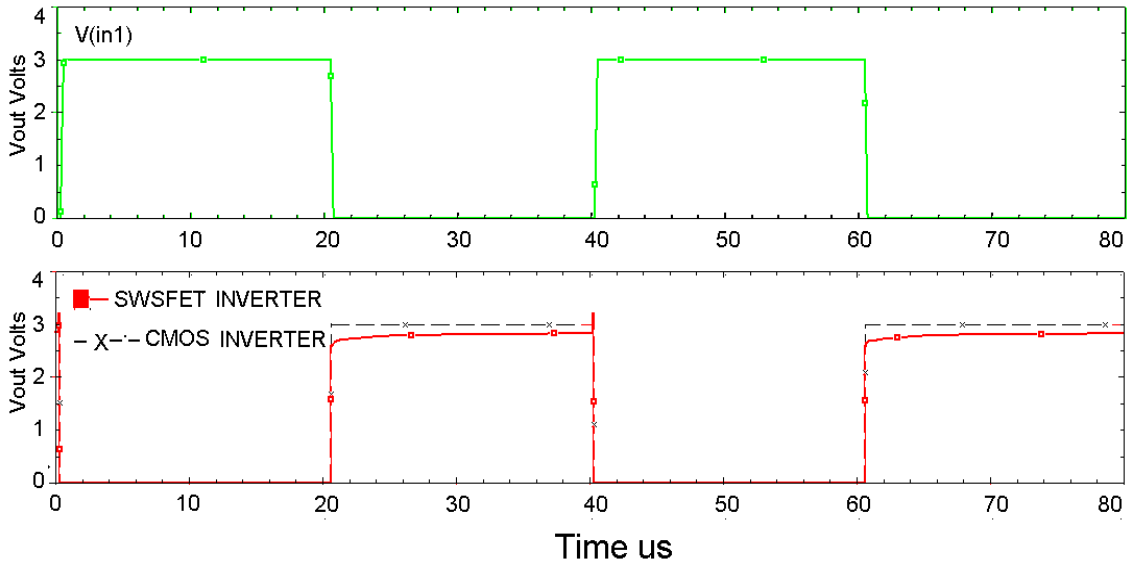


Figure 63A. The simulation of 5μm n-SWS-FET and CMOS inverter.

In addition, the simulations of L=1 µm and 20 nm n-SWS-FET inverter are shown in Figures 63B and 63C, respectively. Table 21 shows the parameters of 5 µm, 1 µm, and 20 nm inverter.

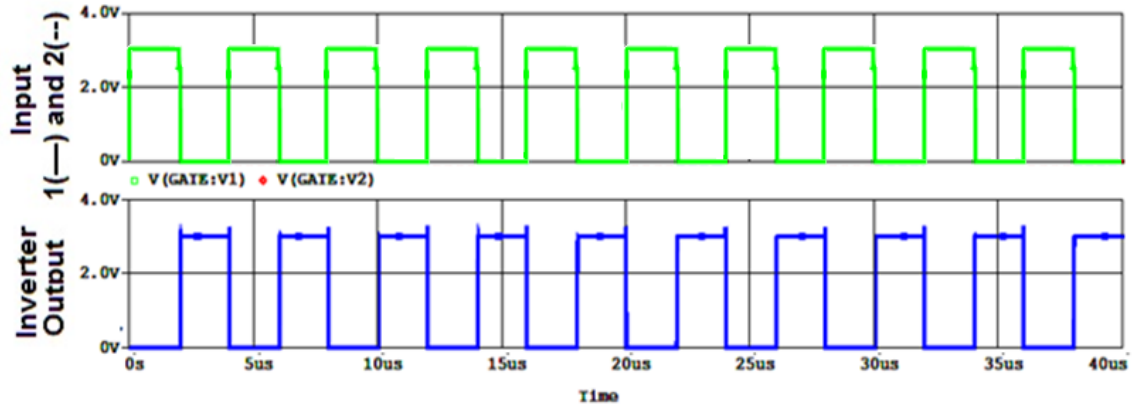


Figure 63B. The simulation of 1 µm n-SWS-FET inverter.

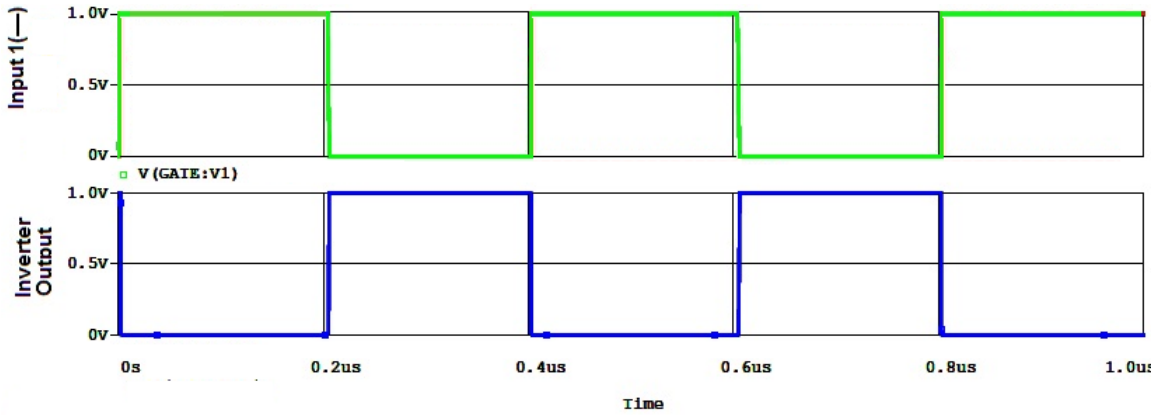


Figure 63C. The simulation of 20 nm n-SWS-FET inverter.

Table 21. The transistor parameters use in logic gate Inverter, NAND, NOR, XNOR

Transistor	Channel Length L	Gate Width		V_{DD} V	Vth V		V_{UL} V
		W1	W2		V_{TH1}	V_{TH2}	
n-FET	5 µm	10 µm	-	3	0.72	-	-
p-FET	1 µm	20 µm	-	3	-0.91	-	-
n-SWS-FET	5 µm	10 µm	20 µm	3	0.8	0.6	0.72
n-SWS-FET	1 µm	2 µm	4 µm	3	0.5	0.3	0.4
n-SWS-FET	20 nm	40 nm	80 nm	1	0.1	0.2	0.15

The simulation of 5 µm, 1 µm, and 20 nm n-SWS-FET NAND logic is shown in Figure 64A. It has two data inputs Vin1 and Vin2, the inputs are two squire pulse signal providing the four possible outputs of NAND gate. As expected, the output is low (0) when Vin1=Vin2=0, otherwise the output is high (≈ V_{DD}), which is indicating a correct NAND function. The transient simulation was performed by making Vin2 run at 2*pulse- width of Vin1. This causes a rogue pulse when Vin1 rises and Vin2 falls.

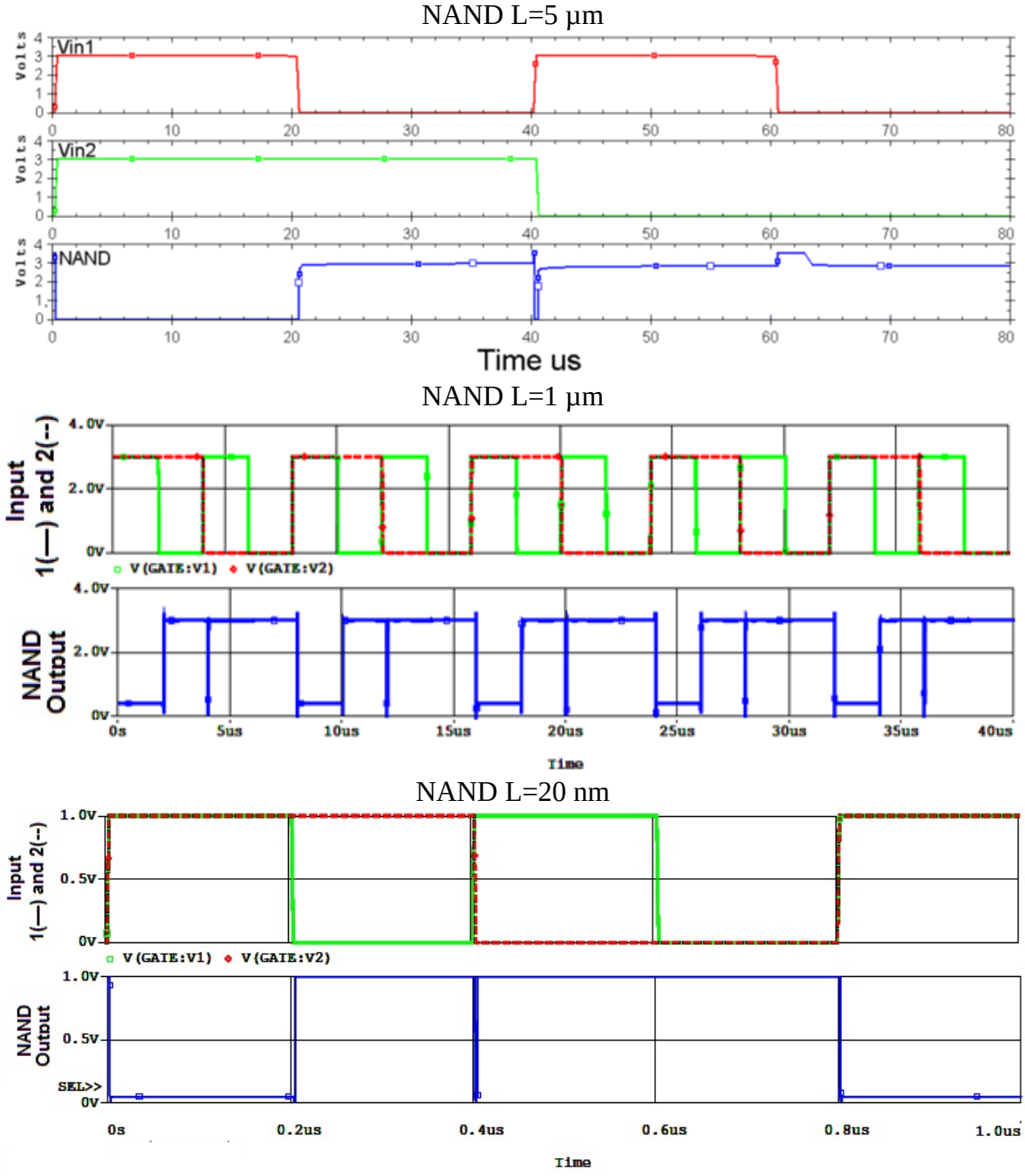
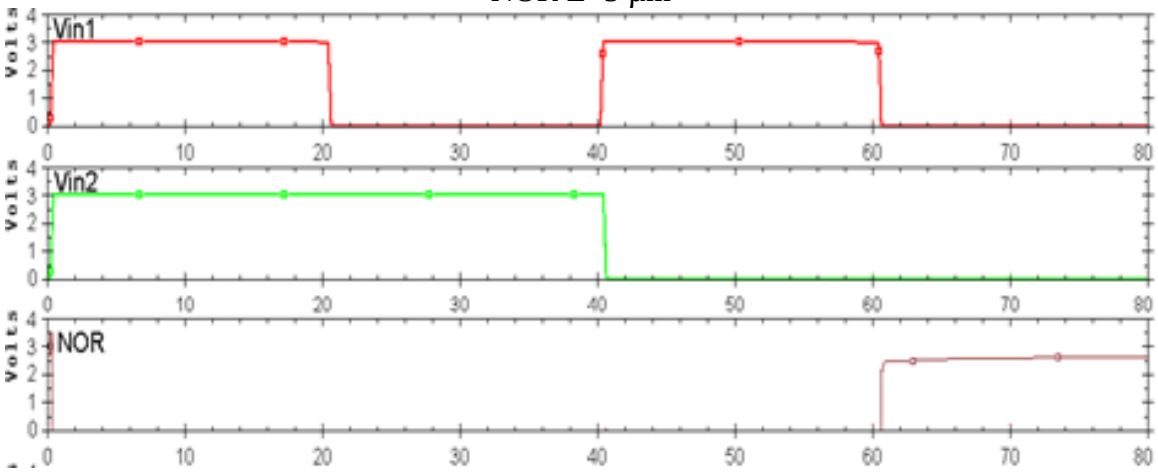


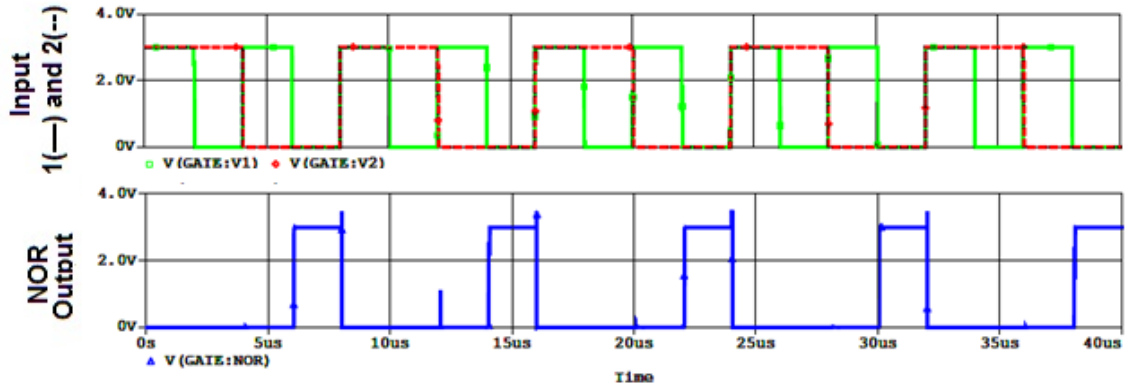
Figure 64A. The simulation of 5 µm, 1 µm, and 20 nm n-SWS-FET NAND

Figure 64B presents the simulation of 5 µm, 1 µm, and 20 nm n-SWS-FET NOR. It has two data inputs Vin1 and Vin2, the inputs are two squire pulse signal providing the four possible outputs of NOR gate. As expected, the output is high (≈ V_{DD}) when Vin1=Vin2=0, otherwise the output is low (0), which is a NOR gate.

NOR L=5 µm



NOR L=1 µm



NOR L=20 nm

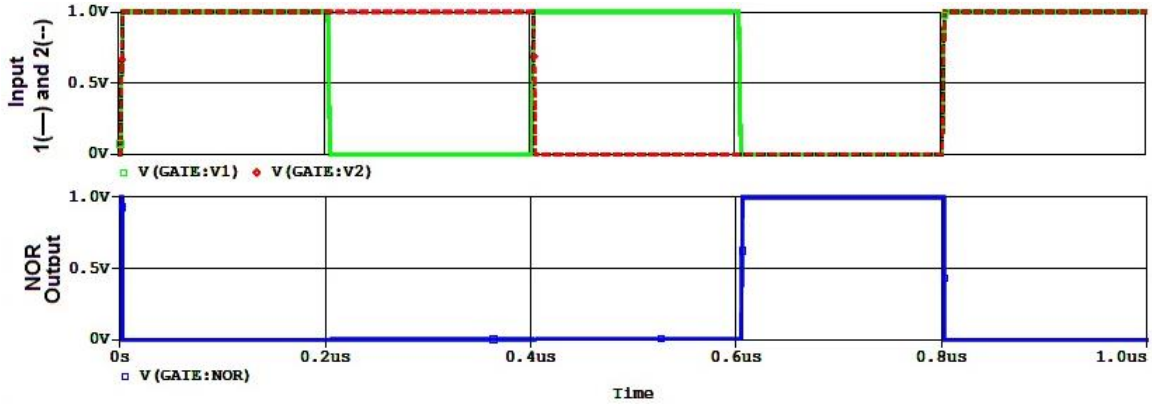


Figure 64B. The simulation of 5 µm, 1 µm, and 20 nm n-SWS-FET NOR

n-SWS-FET (L=5 µm) XNOR gate and XOR gate simulation are shown in Figure 64C, the gate inputs are Vin1 and Vin2. As expected, when Vin1≠Vin2 XOR is high (≈ V_{DD}) and XNOR is low (0), otherwise the output is low. The rogue pulse occurs for the reason in NAND gate.

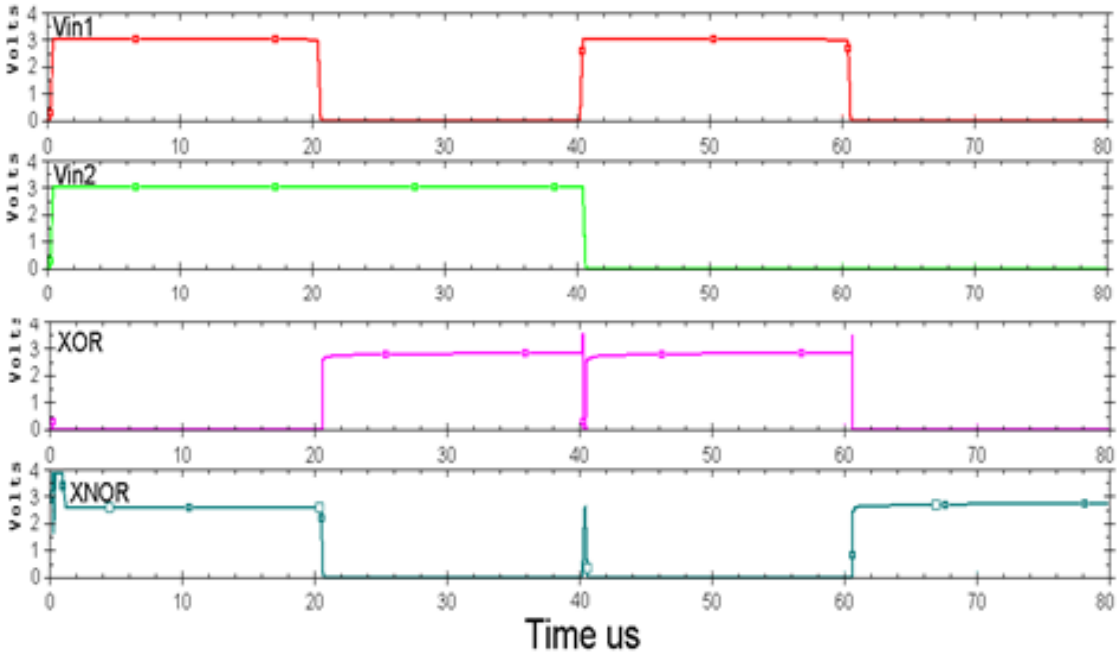


Figure 64C. The simulation of 5 µm n-SWS-FET XOR and XNOR

The SWS-FET half-adder is presented in Figure 65. The half-adder binary inputs are V(A) and V(B). A sum of the binary input data is denoted by V(SUM) and a carry bit is indicated as V(CARRY). In the simulation, the sum is the XOR of the inputs and the carry is the AND of inputs which confirmed the functionally of half-adder circuit. The simulations of the SWS-FET half-adder circuit have been done at 5µm channel length.

Figure 66 illustrates the simulation of L=5 µm D Latch circuit using CMOS and n-SWS-FET. DATA and CLOCK are the inputs of circuit. The outputs of the COMS circuit and the SWS-FET circuit are identical, except that the SWS-FET circuit output has some rogue pulse, but it is sufficient to show that -SWS-FET circuit can be used to implement D Latch.

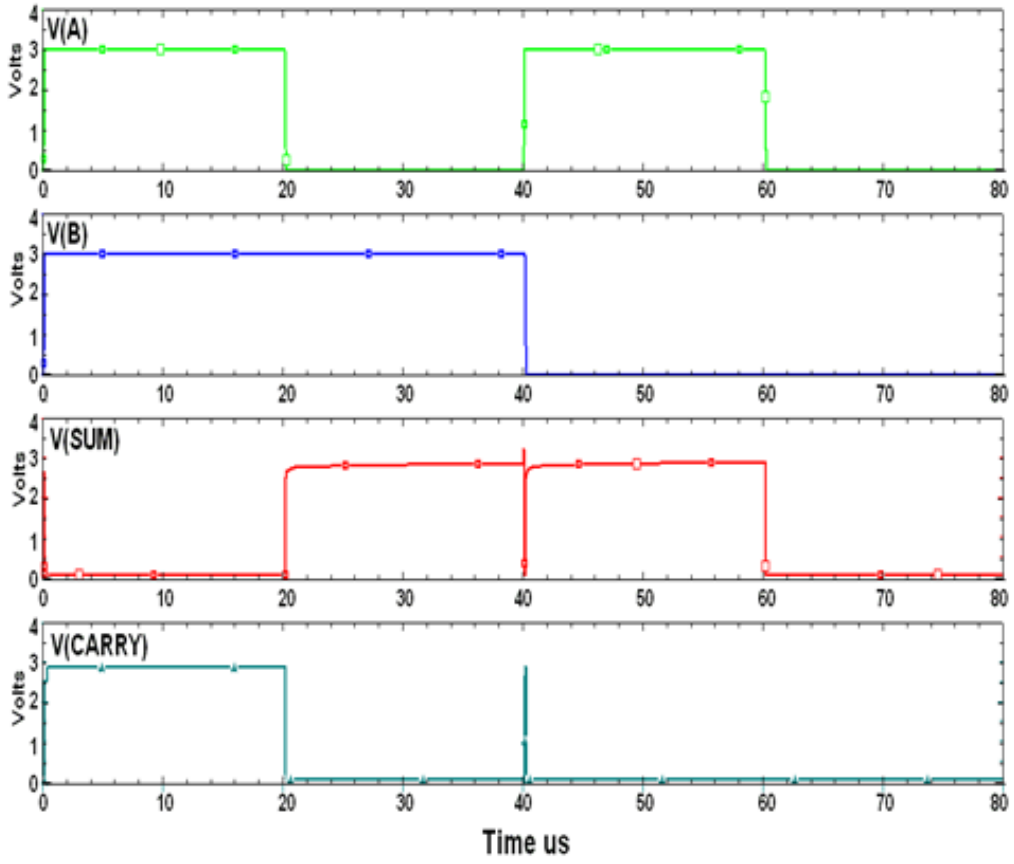


Figure 65. The simulation for n-SWS-FET-Half Adder

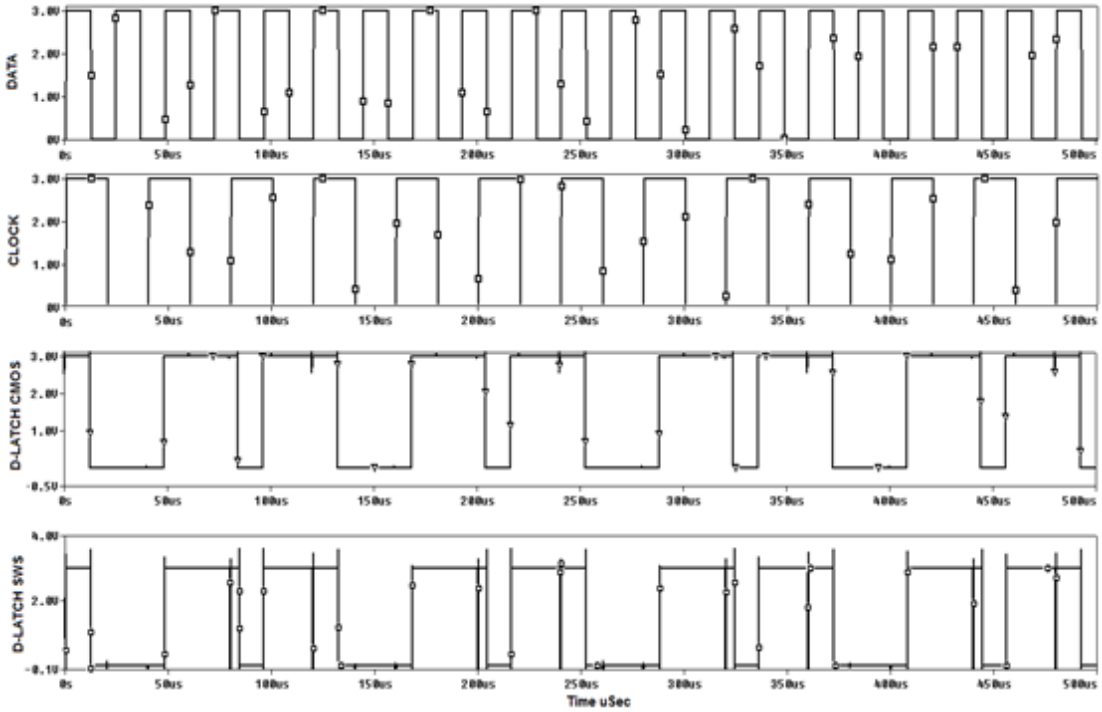


Figure 66. The simulation of CMOS and n-SWS-FET D Latch circuit

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5-2 The simulation of SRAM Using n-SWS-FET

Figure 67 shows transient simulations of 6T-COMS SRAM, SWS-FET SRAM T3, and the modified SWS-FET SRAM (TM2) cells. The parameters of 5µm in Table 21 are used to simulate SRAM's. The simulations of the COMS and SWS SRAM cells are identical. In case of Write input signal is on (=V_{DD}), Stored Data signal flows Data input signal. When Write input signal is switched off (=0), the voltage stays at the storage node. The simulation result depicts the n-SWS-FET SRAM stored the data as expected.

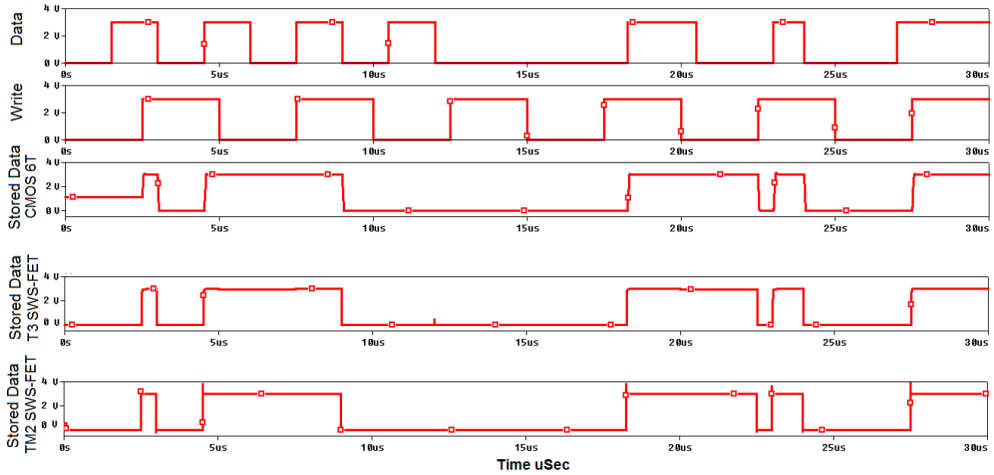


Figure 67. The simulation of SRAM.

5-3 The Simulation of 3-Bit Flash ADC Using SWS-FET

The three bit Analog-to-Digital (ADC) SWS-FET voltage detector/ compactor is shown in Figure 68 using 180nm process (see AppendixB). the SWS-FET compactor provide 8-different state for outputs signal S1-5 according the input signal as shown in Table 22. Moreover, the simulation of SWS-FET and CMOS- TIQ comparators are shown in Figure 69. Table 22 shows the relation between of SWS-FET and CMOS- TIQ output.

Table 22. The compactors output CMOS- TIQ (Out 1-7) and SWS-FET (S1-5).

Vin	**[0,1/8]**	**[1/8,2/8]**	**[2/8,3/8]**	**[3/8,4/8]**	**[4/8,5/8]**	**[5/8,6/8]**	**[6/8,7/8]**	**[7/8,8/8]**
TIQ output	**ALL 0**	**Out1 V_{DD}**	**Out2 V_{DD}**	**Out3 V_{DD}**	**Out4 V_{DD}**	**Out5 V_{DD}**	**Out6 V_{DD}**	**Out7 V_{DD}**
S1	0	V_{DD}	V_{DD}	0	0	0	0	0
S2	0	0	V_{DD}	V_{DD}	0	0	0	0
S3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	0	0	0	0
S4	0	0	0	Floating=0	Floating=0	V_{DD}	V_{DD}	Floating=0
S5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Floating=0	Floating=0

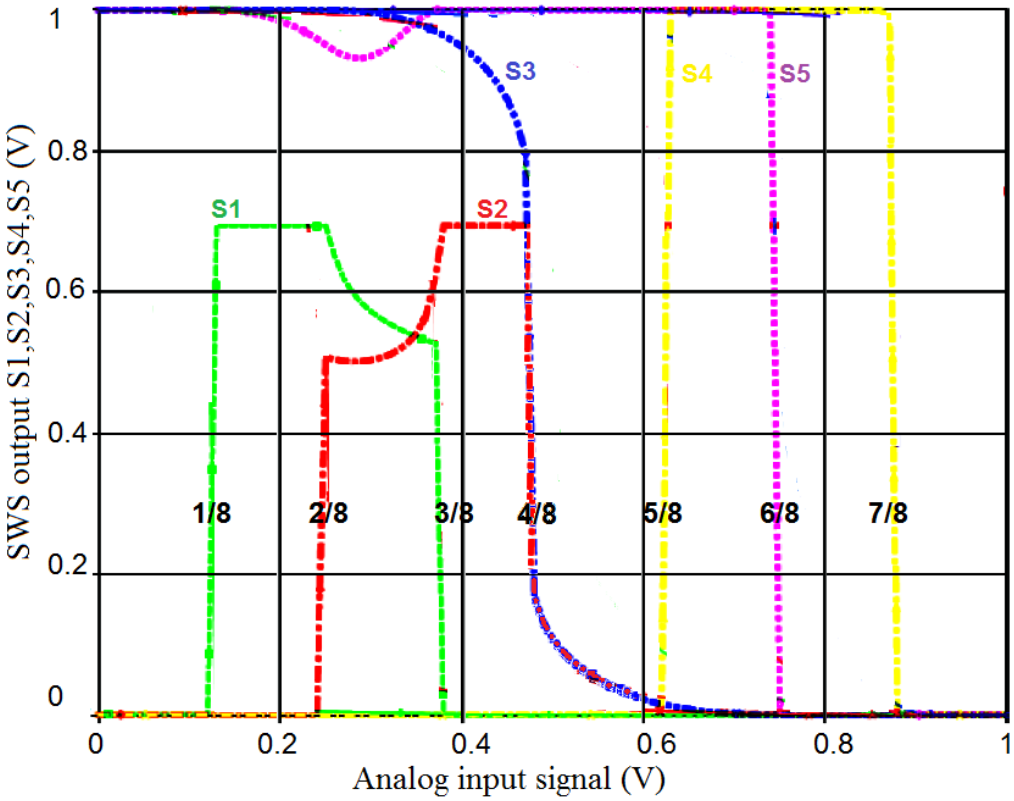


Figure 68. SWS (S1-5) compactors output.

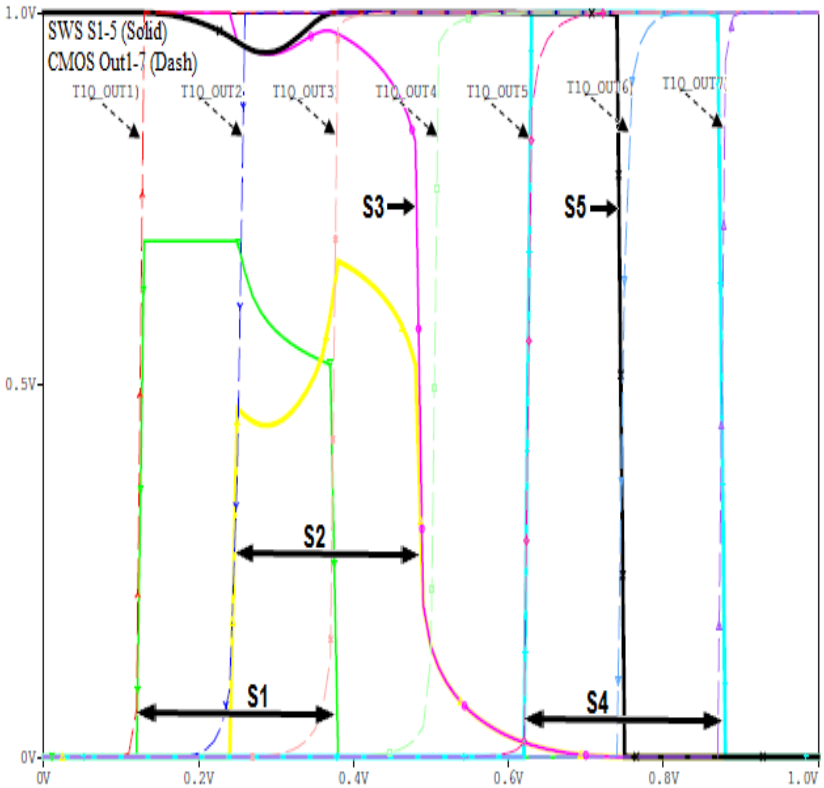


Figure 69. SWS (solid) and CMOS (dished) compactors output.

The simulation of 3-Bit SWS-FET encoder (LSB-B1 least-significant-bit, B2 second bit, and B3 most significant-bit) is shown in Figure 70. In addition Figure 71 shows the simulation of 3-Bit CMOS encoder. The outputs of both encoders (SWS-FET and CMOS) are identical and responding in the same time.

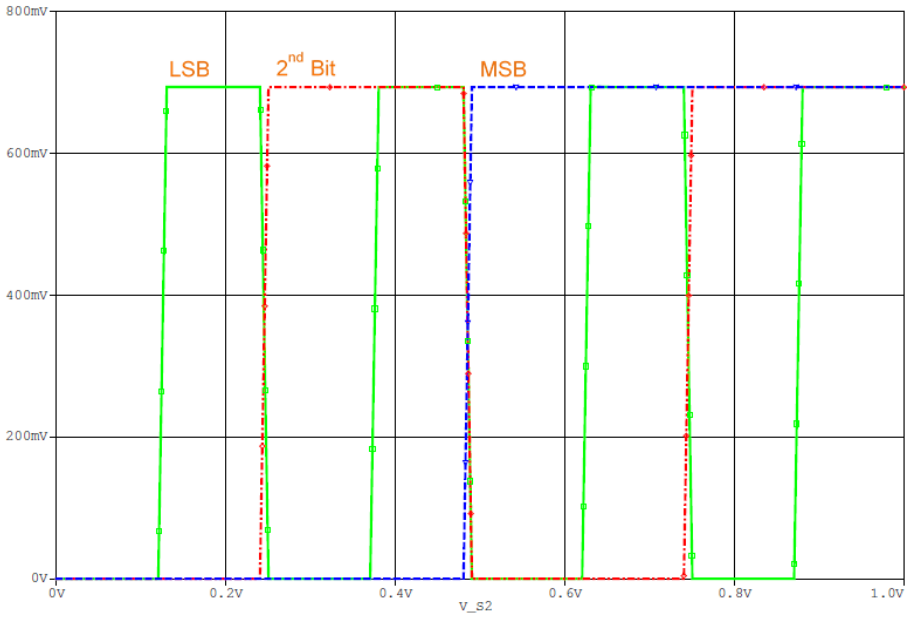


Figure 70. SWS (solid) and CMOS (dished) compactors output.

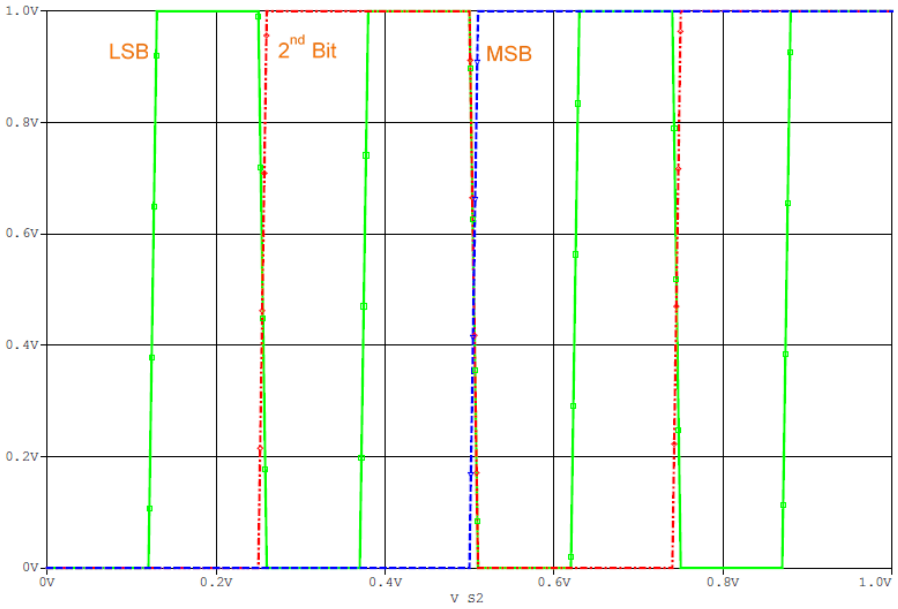


Figure 71. SWS (solid) and CMOS (dished) compactors output.

The Equation 22 is used to generate DAC. The DAC simulation of C-SWS-FET, CMOS, and Ideal DAC is shown in Figure 72. The DAC simulation show that 3-bit ADC based on C-SWS-FET design works as expected.

DAC=MSB/2+2nd Bit/4+LSB/8 **(22)**

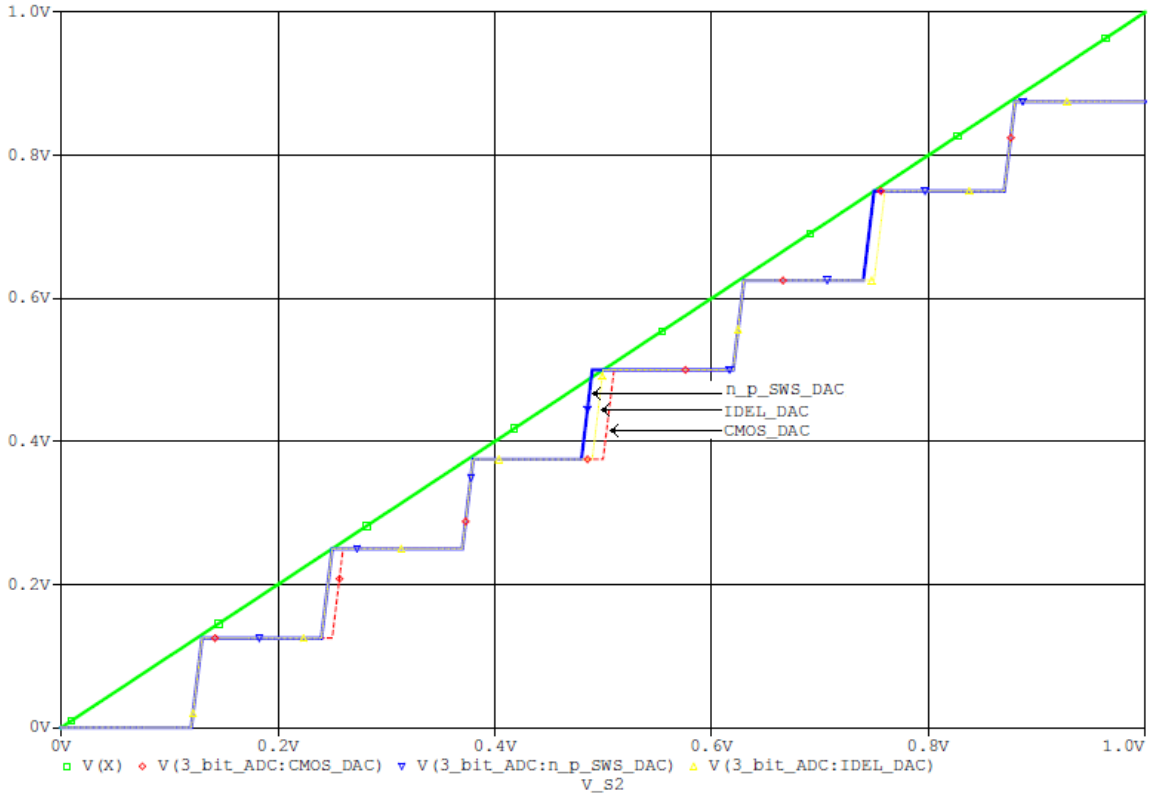


Figure 72. The DAC simulation of C-SWS-FET, CMOS, and ideal DAC.

The simulation of a 3-Bit DAC based on C-SWS-FET is shown in Figure 73 (at 10 MHz input) and Figure 74 (at 100 MHz input). The simulations have the expected result.

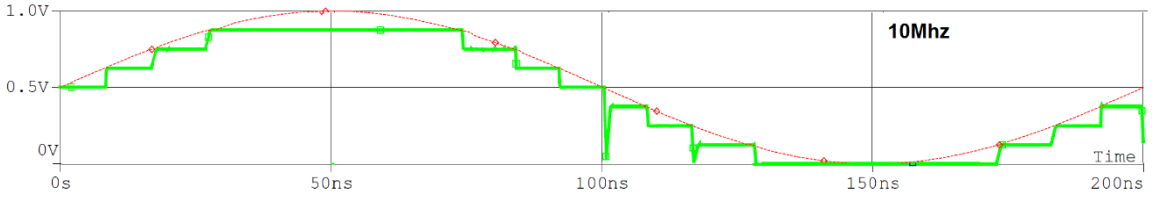


Figure 73. SWS-FET 3 Bit ADC input (red) and output (green) at 10 MHz

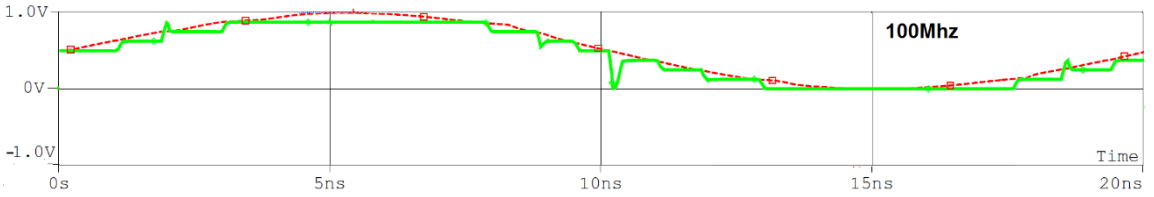


Figure 74. SWS-FET 3 Bit ADC input (red) and output (green) at 100 MHz

The total delay of LSB 3- bit flash ADC is shown in Figure 75, the CMOS circuit has 1ns delay, where C-SWS-FET circuit has 1.4ns delay.

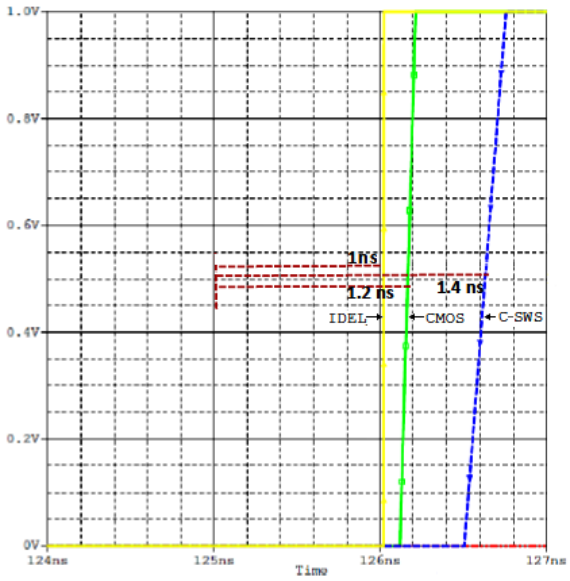


Figure 75 LSB Delay for 1 MHz ramp input.

Finally, the simulations of SWS-FET logic gates, Half-Adder, D Latch SRAMs, and ADC show the circuit work as conventional CMOS circuit and the truth tables with fewer number of transistors as shown in Figure 76.

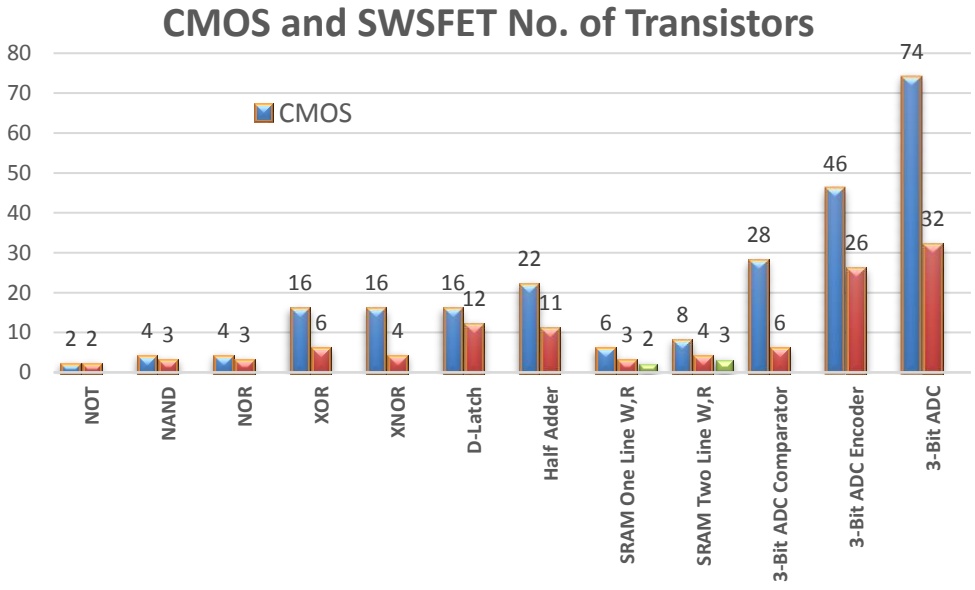


Figure 76. The number of transistors between CMOS and SWSFET technology.

6-CONCLUSION

This dissertation presents the modeling of the Spatial Wavefunction Switched Field-Effect Transistors (SWS-FETs). We have used Cadence simulator using models of BSIM 3v3 for 1 μm, BSIM 4.6 for 20 nm, and EKV v301.01 for 180 nm.

Using the two wells n-channel SWSFETs, we have been able to design compact circuits and power efficient NOT, NAND, NOR, XOR, and & XNOR gates, the transient simulations were done in order to verify the gates functionality and logical agreements. The total number of the FETs is reduced by 25% for NAND-NOR and %75 for XOR-XNOR. Furthermore, the one bit Half-adder circuit is simulated using n-SW-SFET AND/XOR. Also the D Latch circuit is simulated using four n-SW-SFET NAND.

In addition, we have design two compact power efficient circuits of SRAM (TM2 and TM3). The SRAM TM2 circuit has two n-SWS-FET, the SRAM TM3 circuit has two n-SWS-FET and one n-MOSFET. The transient simulations present to verify the functionality of The SRAM circuits and both circuits offer the write and the read operation as standard CMOS 6T and 8T SRAMs. This makes the savings as 60% for implementing SRAM cell using SWS-FETs.

Finally, we have demonstrated 3-bit Analog-to-Digital Converter based on two quantum well channel complementary SWS-FETs with 180 nm channel length. The number of the FETs is reduced from 74 in conventional CMOS architecture to 32 using complementary SWS-FETs. This reduces cell area and power dissipation, making SWS-FET a promising technology for analog applications.

Future Work

SWSFET model was made to verify the functionality of device in several VLSI logic and circuits. The quantum simulation of the unconnected device have presented to confirm the switching. The most interesting dimension of these SWSFETs is the multi-valued logic but there are several challenges pertinent to fabrication in sub nm regime and realization of these circuits.

7-REFERENCES:

1. Jain, F. C., B. Miller, E. Suarez, P.-Y. Chan, S. Karmakar, F. Al-Amoody, M. Gogna, J. Chandy, and E. Heller. "Spatial Wavefunction -Switched (SWS) InGaAs FETs with II–VI Gate Insulators." Journal of Electronic Materials Journal of Elec Materi 40.8 (2011): 1717-726.
2. Jain, F., P.-Y. Chan, M. Lingalugari, J. Kondo, E. Suarez, P. Gogna, J. Chandy, and E. Heller. "Si and InGaAs Spatial Wavefunction -Switched (SWS) FETs with II–VI Gate Insulators: An Approach to the Design and Integration of Two-Bit SRAMs and Binary CMOS Logic." Journal of Electronic Materials Journal of Elec Materi 44.9 (2015): 3108-115
3. Karmakar, Supriya, John A. Chandy, and Faquir C. Jain. "Implementation of Unipolar Inverter Based on Spatial Wavefunction Switched FET (SWSFET)." 2012 Lester Eastman Conference on High Performance Devices (LEC) (2012)
4. Karmakar, Supriya, John A. Chandy, and Faquir C. Jain. "Unipolar Logic Gates Based on Spatial Wavefunction Switched FETs." IEEE Transactions on Very Large Scale Integration (VLSI) Systems IEEE Trans. VLSI Syst. 23.4 (2015): 609-18.
5. Gogna, P. "Quaternary Logic and Applications Using Multiple Quantum Well Based SWSFETs." International Journal of VLSI Design & Communication Systems VLSICS 3.5 (2012):27-42.
6. Karmakar, Supriya, and Faquir C. Jain. "Future Semiconductor Devices for Multi-Valued Logic Circuit Design." MSA Materials Sciences and Applications 03.11 (2012): 807-14
7. Karmakar, Supriya. "Design of Three Bit Analog-To-Digital Converter (ADC) Using Spatial Wavefunction Switched (SWS) FETS." International Journal of VLSI Design & Communication Systems VLSICS 4.3 (2013): 1-14

8. Heller, E.k, S.k Islam, G. Zhao, and F.c Jain. "Analysis of In0.52Al0.48As/In0.53Ga0.47As/InP Quantum Wire MODFETs Employing Coupled Well Channels." Solid-State Electronics 43.5 (1999): 901-14.

9. S. K. Islam and F. C. Jain.” Design and Analysis of INGAN-GAN Modulation-Doped Field-Effect Transistors (MODFETS) For 90 Ghz Operations.” International Journal of Infrared and Millimeter Waves, Vol. 22, No. 10.10 (2001)

10. Yeo, Yee-Chia, Qiang Lu, Tsu-Jae King, Chenming Hu, T. Kawashima, M. Oishi, S. Mashiro, and J. Sakai. "Enhanced Performance in Sub-100 Nm CMOSFETs Using Strained Epitaxial Silicon-germanium." International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138) (2000)

11. BSIM Group at UC Berkeley, BSIM4.6.4 MOSFET model: User's manual.

12. Zhao, W., and Y. Cao. "New Generation of Predictive Technology Model for Sub-45 Nm Early Design Exploration." IEEE Trans. Electron Devices IEEE Transactions on Electron Devices 53.11 (2006): 2816-823

13. Borisov, S., and A. S. Korotkov. "Procedure for Building a MOS Transistor High Frequency Small-signal Model." Radioelectron.Commun.Syst. Radioelectronics and Communications Systems 53.7 (2010): 356-66.

14. Schneider, Márcio Cherem., and Carlos Galup-Montoro. CMOS Analog Design Using All-region MOSFET Modeling. Cambridge: Cambridge UP, 2010

15. Lovelace, D., J. Costa, and N. Camilleri. "Extracting Small-signal Model Parameters of Silicon MOSFET Transistors." 1994 IEEE MTT-S International Microwave Symposium Digest (Cat. No.94CH3389-4) (1994)

16. Angelov, I., M. Fernhdal, F. Ingvarson, H. Zirath, and H.o. Vickes. "CMOS Large Signal Model for CAD." IEEE MTT-S International Microwave Symposium Digest, 2003 (2003)

17. Cao, K.m., W.-C. Lee, W. Liu, X. Jin, P. Su, S.k.h. Fung, J.x. An, B. Yu, and C. Hu. "BSIM4 Gate Leakage Model including Source-drain Partition."International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138) (2000)

18. Sohrab Emami, Chi& H. Doan, Ali M. Niknejad, and Robert W. Brodersen.” Large-Signal Millimeter-Wave CMOS Modeling with BSIM3” Berkeley Wireless Research Center, University of California, Berkeley, CA 94704, USA

19. Cadence SPICE Reference Manual. N.p., 23 Nov. 2001. Web. 20 Nov. 2015.

20. Kim, Seong-Dong, Cheol-Min Park, and J.c.s. Woo. "Advanced Model and Analysis of Series Resistance for CMOS Scaling into Nanometer Regime. II. Quantitative Analysis." IEEE Trans. Electron Devices IEEE Transactions on Electron Devices 49.3 (2002): 467-72.

21. Cirit, M.a. "The Meyer Model Revisited: Why Is Charge Not Conserved? (MOS Transistor)." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. 8.10 (1989): 1033-037

22. Zaki, Tarek, Susanne Scheinert, Ingo Horselmann, Reinhold Rodel, Florian Letzkus, Harald Richter, Ute Zschieschang, Hagen Klauk, and Joachim N. Burghartz. "Accurate Capacitance Modeling and Characterization of Organic Thin-Film Transistors." IEEE Trans. Electron Devices IEEE Transactions on Electron Devices 61.1 (2014): 98-104

23. Cadence Application Note. ”A Nonlinear Capacitor Model for Use in the PSpice Environment.” 12 (2009)

24. Saman, Bander, P. Mirdha, M. Lingalugari, P. Gogna, F. C. Jain, El-Sayed Hasaneen, and E. Heller. "Logic Gates Design and Simulation Using Spatial Wavefunction Switched (SWS) FETs." International Journal of High Speed Electronics and Systems Int. J. Hi. Spe. Ele. Syst. 24.03n04 (2015): 1550008

25. Swati Sharma, Rajesh Mehra. “ Area & Power Efficient Design of XNOR-XOR Logic Using 65nm Technology.” National Conference on Synergetic Trends in engineering and Technology (STET-2014) International Journal of Engineering and Technical Research ISSN: 2321-0869, Special Issue.

26. Maruf M Ali,S. M. Mainul Islam,Md. Mehedi Farhad,Md. Rubaiyat Ialam,and Nazmun.Islam, “Analysis of CMOS Multiplexer Circuits of Different Area and Logic Style.” IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 3, Issue 6 (Nov. – Dec. 2013), PP 17-27

27. V, Ganesan., and Shaji. K. S. "Design of RS and D-Flip-Flop Using AlGaAs/GaAs MODFET Technology." International Journal of Computer Applications IJCA 83.8 (2013): 16-20.

28. Boley, James, Jiajing Wang, and Benton H. Calhoun. "Analyzing Sub-Threshold Bitcell Topologies and the Effects of Assist Methods on SRAM VMIN." Journal of Low Power Electronics and Applications JLPEA2.4 (2012): 143-54

29. Gogna, P., E. Suarez, M. Lingalugari, J. Chandy, E. Heller, E.-S. Hasaneen, and F.-C. Jain. "Ge-ZnSSe Spatial Wavefunction Switched (SWS) FETs to Implement Multibit SRAMs and Novel Quaternary Logic." Journal of Electronic Materials Journal of Elec Materi 42.11 (2013)

30. Gogna, P., M. Lingalugari, J. Chandy, F. C. Jain, E. Heller, and E-S. Hasaneen. "Efficient Multi-bit SRAMs Using Spatial Wavefunction Switched (SWS)-FETs." 2012 Lester Eastman Conference on High Performance Devices (LEC) (2012):

31. Jain, F. C., J. Chandy, B. Miller, E-S. Hasaneen, and E. Heller. "Spatial Wavefunction -Switched (Sws)-Fet: A Novel Device To Process Multiple Bits Simultaneously With Sub-Picosecond Delays." International Journal of High Speed Electronics and Systems Int. J. Hi. Spe. Ele. Syst. 20.03 (2011)

32. F. Jain1 , M. Lingalugari1 , B. Saman1 , P. Mirdha1 , P-Y. Chan1 , P. Gogna1 , E-S. Hasaneen1 , J. Chandy1 and E. Heller." Multi-State QDC-SWS FETs for Compact Memory Circuits." Submitted to IEEE International Electron Devices Meeting (IEDM), 8 (2015)

33. Bander Saman*, P. Gogna, E-S. Hasaneen, E. Heller And F.C. Jain." Spatial Wavefunction Switched (SWS) FETs SRAM Circuits and Simulation." Submitted to International Journal for High-Speed Electronics and Systems (IJHSES), 9 (2015).

34. K. Iniewski, S. Voinigescu, J. Atcha and C.A.T. Salama, "Analytical Modeling of Threshold Voltages in p-Channel Si/SiGe/Si MOS Structures", Solid-State Electron., 36(5), 775–783, 1993.F. Jain, M. Lingalugari, J. Kondo, P. Mirdha, E. Suarez, J. Chandy, and E. Heller, "Quantum Dot Channel (QDC) FETs with Wraparound II–VI Gate Insulators: Numerical Simulations," Journal of Electronic Materials, vol. 45, no. 11, pp. 5663–5670, Mar. 2016.F.

35. Jain, M. Lingalugari, J. Kondo, P. Mirdha, E. Suarez, J. Chandy, and E. Heller, "Quantum Dot Channel (QDC) FETs with Wraparound II–VI Gate Insulators: Numerical Simulations," Journal of Electronic Materials, vol. 45, no. 11, pp. 5663–5670, Mar. 2016.

36. "Using MOS gate capacitance models", [Online]. Available: http://helpme.scudc.scu.edu/hspice2001/hspice_and_qrg/hspice_2001_2-150.html. Accessed: Oct. 29, 2016.

37. N. Arora, Mosfet modeling for VLSI simulation: Theory and practice. Singapore, Singapore: World Scientific Publishing Co Pte, 2007.

38. P. E. Allen and D. R. Holberg, CMOS analog circuit design, 3rd Ed. New York: Oxford University Press, USA, 2011.

39. S. Karmakar and F. C. Jain, "Design of Three bit ADC and DAC Using Spatial Wavefunction Switched SWSFETs," Silicon, vol. 8, no. 3, pp. 369–379, 2016.

40. Avant!, Star-Hspice Manual, Release 2001.2, pp. 20-94 to 20-98, June 2001,

PUBLICATIONS & CONFERENCE PROCEEDINGS:

1. P. Mirdha, M. Lingalugari, P.-Y. Chan, S. Bander, and F. Jain, Proceedings of 22nd Connecticut Microelectronics and Optoelectronics (CMOC) Symposium, March 13, Yale University (2013).

2. B. Saman, P. Mirdha, M. Lingalugari, J. Kondo, and F. Jain, Proceedings of 23rd Connecticut Microelectronics and Optoelectronics (CMOC) Symposium, April 9, University of Connecticut (2014).

3. B. Saman1, M. Alzaidi, J. Kondo, P. Gogna, and F.C. Jain of 24th Connecticut Microelectronics and Optoelectronics (CMOC) Symposium, April 9, University of Bridgeport (2015).

4. Saman, Bander, P. Mirdha, M. Lingalugari, P. Gogna, F. C. Jain, El-Sayed Hasaneen, and E. Heller. "Logic Gates Design and Simulation Using Spatial Wavefunction Switched (SWS) FETs." International Journal of High Speed Electronics and Systems Int. J. Hi. Spe. Ele. Syst. 24.03n04 (2015): 1550008

5. Bander Saman, P. Gogna, E-S. Hasaneen, E. Heller And F.C. Jain." Spatial Wavefunction Switched (SWS) FETs SRAM Circuits and Simulation." Submitted to International Journal for High-Speed Electronics and Systems (IJHSES), 9 (2016)

6. Bander Saman, Pawan Gogna, Sayed Hasaneen, John Chandy, Evan Heller, and Faquir Jain, "Complementary Spatial Wave-function Switched (SWS) FETs and Circuits ." Submitted to Solid-State Electronics Journal, 12 (2016)

APPENDIX A: BSIM MODELS

1µm n-MOSFET

```
.MODEL  1umn  NMOS  (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=2E-8 XJ=1.84E-7 NCH=1E17 NSUB=1E17 XT=8.66E-8
+VTH0=0.858 U0= 650 WINT=0.81E-7 LINT=0.5E-7
+NGATE=5E20 RSH=1082 JS=1.E-8 JSW=1E-8 CJ=0.32E-4 MJ=0.64 PB=0.757
+CJSW=0.26E-10 MJSW=0.5 PBSW=0.757 PCLM=5
+CGSO=0.354E-10 CGDO=0.354E-10 CGBO=0.45E-10)
```

0.5µm n-MOSFET

```
******  AMI 0.5u bsim3 data
** N8BN AMI 0.5U run data SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS
* DATE: Jan 25/99
* LOT: n8bn                WAF: 03
* Temperature_parameters=Default
.MODEL AM05L7N NMOS (                          LEVEL   = 7
+                    TNOM    = 27          TOX     = 1.41E-8
+XJ      = 1.5E-7        NCH     = 1.7E17        VTH0    = 0.7086
+K1      = 0.8354582     K2      = -0.088431     K3      = 41.4403818
+K3B     = -14           W0      = 6.480766E-7   NLX     = 1E-10
+DVT0W   = 0             DVT1W   = 5.3E6         DVT2W   = -0.032
+DVT0    = 3.6139113     DVT1    = 0.3795745     DVT2    = -0.1399976
+U0      = 533.6953445   UA      = 7.558023E-10  UB      = 1.181167E-18
+UC      = 2.582756E-11  VSAT    = 1.300981E5    A0      = 0.5292985
+AGS     = 0.1463715     B0      = 1.283336E-6   B1      = 1.408099E-6
+KETA    = -0.0173166    A1      = 0             A2      = 1
+RDSW    = 2.268366E3    PRWG    = -1E-3         PRWB    = 6.320549E-5
+WR      = 1             WINT    = 2.043512E-7   LINT    = 3.034496E-8
* +XL     = 0             XW      = 0
+ DWG     = -1.446149E-8
+DWB     = 2.077539E-8   VOFF    = -0.1137226    NFACTOR = 1.2880596
+CIT     = 0             CDSC    = 1.506004E-4   CDSCD   = 0
+CDSCB   = 0             ETA0    = 3.815372E-4   ETAB    = -1.029178E-3
+DSUB    = 2.173055E-4   PCLM    = 0.6171774     PDIBLC1 = 0.185986
+PDIBLC2 = 3.473187E-3   PDIBLCB = -1E-3         DROUT   = 0.4037723
+PSCBE1  = 5.998012E9    PSCBE2  = 3.788068E-8   PVAG    = 0.012927
+DELTA   = 0.01          MOBMOD  = 1             PRT     = 0
+UTE     = -1.5          KT1     = -0.11         KT1L    = 0
+KT2     = 0.022         UA1     = 4.31E-9       UB1     = -7.61E-18
+UC1     = -5.6E-11      AT      = 3.3E4         WL      = 0
+WLN     = 1             WW      = 0             WWN     = 1
+WWL     = 0             LL      = 0             LLN     = 1
+LW      = 0             LWN     = 1             LWL     = 0
+CAPMOD  = 2             XPART   = 0.4           CGDO    = 1.99E-10
+CGSO    = 1.99E-10      CGBO    = 0             CJ      = 4.233802E-4
+PB      = 0.9899238     MJ      = 0.4495859     CJSW    = 3.825632E-10
+PBSW    = 0.1082556     MJSW    = 0.1083618     PVTH0   = 0.0212852
+PRDSW   = -16.1546703   PK2     = 0.0253069     WKETA   = 0.0188633
+LKETA   = 0.0204965     )
```

50nm n-MOSFET

```
.model BSIM50nmN nmos level = 8
*+Lambda={lam}
+vth0=0.22
+binunit = 1 paramchk= 1 mobmod = 0
+capmod = 2 igcmod = 1 igbmod = 1 geomod = 1
+diomod = 1 rdsmod = 0 rbodymod= 1 rgatemod= 1
+permod = 1  acnqsmod= 0 trnqsmod= 0
+tnom = 27  toxe = 1.4e-009 toxp =1.4e-009 toxm = 1.4e-009
+epsrox = 3.9  wint = 5e-009 lint = 1.2e-009
*+II =0
+wl =0 lln =1
*+win = 1
+lw =0  ww =0
*Iwn = 1
+wwn = 1
+lwl = 0  wwl = 0 xpart = 0 toxref = 1.4e-009
+vth0 = 0.25  k1 = 0.35 k2 = 0.05 k3 =0
+k3b = 0
*+wO = 2.5e-006
*+dvtO = 2.8 +dvtl = 0.52 +dvt2 = -0.032  dvtOw = 0 dvtlw =0 dvt2w =0
+dsub = 2  minv = 0.05 voffl =0
*+dvtpO = 1e-007
+dvtp1 = 0.05
*IpeO = 5.75e-008 +Ipeb =2.3e-010
+xj = 2e-008
+NSUB=1e17
+ngate = 5e020  ndep =2.8e+018 nsd =1e+020 phin = 0
+cdsc = 0.0002  cdscb = 0 cdscd = 0 cit =0
+voff =-0.15  nfactor = 1.2
*+etaO =0.15
+etab = 0
+vfb = -0.55  u0 = 320 ua =1.6e-010 ub =1.1e-017
+uc =-3e-011  vsat =1.1e+005
*+aO =2
+ags = 1e-020
+a1 =0  a2 =1
*+bO =-1e-020
+b1 =0
+keta = 0.04  dwg = 0 dwb =0 pclm =0.18
*+pdibld = 0.028
+pdiblc2 = 0.022 pdiblcb = -0.005 drout =0.45
+pvag = 1e-020  delta =0.01
*+pscbel = 8.14e+8
+pscbe2 =1e-007
+fprout =0.2  pdits = 0.2 pditsd =0.23 pditsl =2.3e+006
+rsh = 3  rdsw = 150 rsw = 150 rdw =150
+rdswmin = 0  rdwmin = 0 rswmin = 0 prwg = 0
+prwb = 6.8e-011  wr =1
*+alphaO =0.074
*+alphal =0.005
+beta0 =30  agidl =0.0002 bgidl =2.1e+009 cgidl =0.0002
+egidl =0.8
+aigbacc = 0.012  bigbacc = 0.0028 cigbacc = 0.002
+nigbacc = 1  aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004
```

+eigbinv= 1.1 nigbinv = 3 aigc =0.017 bigc = 0.0028
+cigc = 0.002 aigsd =0.017 bigsd =0.0028 cigsd =0.002
+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1
+xrcrg1 = 12 xrcrg2 = 5
+cgso =6.238e-010 cgdo =6.238e-010 cgbo =2.56e-011 cgdl = 2.495e-10
+cgsl = 2.495e-10 ckappas = 0.02 ckappad = 0.02 acde = 1
+moin = 15 noff = 0.9 voffcv =0.02
+kt1 = -0.21
*+ktll =0.0
+kt2 = -0.042 ute =-1.5
+ua1 = 1e-009 ub1 =-3.5e-019 uc1 =0 prt =0
+at = 53000
+fnoimod = 1 tnoimod = 0
+jss = 0.0001 jsws =1e-011 jswgs = 1e-010 njs = 1
+ijthsfwd= 0.01 ijthsrev= 0.001 bvs = 10 xjbvs = 1
+jsd = 0.0001 jswd =1e-011 jswgd = 1e-010 njd =1
+ijthdfwd= 0.01 ijthdrev= 0.001 bvd =10 xjbvd = 1
+pbs =1 cjs = 0.0005 mjs = 0.5 pbsws = 1
+cjsws =5e-010 mjsws = 0.33 pbswgs = 1 cjswgs = 3e-010
+mjswgs = 0.33 pbd =1 cjd = 0.0005 mjd = 0.5
+pbswd = 1 cjswd =5e-010 mjswd = 0.33 pbswgd = 1
+cjswgd = 5e-010 mjswgd = 0.33 tpb = 0.005 tcj = 0.001
+tpbsw =0.005 tcjsw = 0.001 tpbswg =0.005 tcjswg =0.001
+xtis = 3 xtid = 3
+dmcg =0e-006 dmci =0e-006 dmdg = 0e-006 dmcgt = 0e-007
+dwj= 0.0e-008 xgw = 0e-007 xgl= 0e-008
+rshg= 0.4 gbmin = 1e-010 rbpb= 5 rbpd = 15
+rbps= 15 rbdb = 15 rbsb= 15 ngcon =1

20nm n-MOSFET

.MODEL 20nmn NMOS LEVEL = 8
+VERSION = 4.6.0 BINUNIT = 1 PARAMCHK= 1 MOBMOD = 0
+CAPMOD = 2 IGCMOD = 1 IGBMOD = 1 GEOMOD = 1
+DIOMOD = 1 RDSMOD = 0 RBODYMOD= 0 RGATEMOD= 1
+PERMOD = 1 ACNQSMOD= 0 TRNQSMOD= 0
*TEMPMOD = 0
+TNOM = 27 TOXE = 1.8E-009 TOXP = 10E-010 TOXM = 1.8E-009
+DTOX = 8E-10 EPSROX = 3.9 WINT = 5E-009 LINT = 1E-009
+LL = 0 WL = 0 LLN = 1 WLN = 1
+LW = 0 WW = 0 LWN = 1 WWN = 1
+LWL = 0 WWL = 0 XPART = 0 TOXREF = 1.4E-009
*+SAREF = 5E-6
*+SBREF = 5E-6
*+WLOD = 2E-6
*+KU0 = -4E-6
*+KVSAT = 0.2 KVTH0 = -2E-8 TKU0 = 0.0 LLODKU0 = 1.1
*+WLODKU0 = 1.1 LLODVTH = 1.0 WLODVTH = 1.0 LKU0 = 1E-6
*+WKU0 = 1E-6 PKU0 = 0.0 LKVTH0 = 1.1E-6 WKVTH0 = 1.1E-6
*+PKVTH0 = 0.0 STK2 = 0.0 LODK2 = 1.0 STETA0 = 0.0
*+LODETA0 = 1.0
+LAMBDA = 4E-10
+VSAT = 1.1E+005
*+VTL = 2.0E5 XN = 6.0 LC = 5E-9
*+RNOIA = 0.577 RNOIB = 0.37
*+LINTNOI = 1E-009

```
*+TVOFF          = 0.0              TVFBSDOFF = 0.0
+VTH0   = 0.2
+K1     = 0.35       K2     = 0.05       K3     = 0
+K3B    = 0          W0     = 2.5E-006   DVT0   = 1.8        DVT1   = 0.52
+DVT2   = -0.032     DVT0W  = 0          DVT1W  = 0          DVT2W  = 0
+DSUB   = 2          MINV   = 0.05       VOFFL  = 0          DVTP0  = 1E-007
+DVTP1  = 0.05       LPE0   = 5.75E-008  LPEB   = 2.3E-010  XJ     = 2E-008
+NGATE  = 5E+020     NDEP   = 2.8E+018   NSD    = 1E+020    PHIN   = 0
+CDSC   = 0.0002     CDSCB  = 0          CDSCD  = 0          CIT    = 0
+VOFF   = -0.15      NFACTOR = 1.2       ETA0   = 0.05       ETAB   = 0
+UC     = -3E-011
+VFB    = -0.55      U0     = 0.032      UA     = 5.0E-011   UB     = 3.5E-018
+A0     = 2          AGS    = 1E-020
+A1     = 0          A2     = 1          B0     = -1E-020    B1     = 0
+KETA   = 0.04       DWG    = 0          DWB    = 0          PCLM   = 0.08
+PDIBLC1 = 0.028     PDIBLC2 = 0.022     PDIBLCB = -0.005    DROUT  = 0.45
+PVAG   = 1E-020     DELTA  = 0.01       PSCBE1 = 8.14E+008  PSCBE2 = 5E-008
+FPROUT = 0.2        PDITS  = 0.2        PDITSD = 0.23       PDITSL = 2.3E+006
+RSH    = 0          RDSW   = 50         RSW    = 50         RDW    = 50
+RDSWMIN = 0         RDWMIN = 0          RSWMIN = 0          PRWG   = 0
+PRWB   = 6.8E-011   WR     = 1          ALPHA0 = 0.074      ALPHA1 = 0.005
+BETA0  = 30         AGIDL  = 0.0001     BGIDL  = 2.1E+009   CGIDL  = 0.0001
+EGIDL  = 0.8
*+AGISL  = 0.0002     BGISL  = 2.1E+009   CGISL  = 0.0002
*+EGISL  = 0.8
+AIGBACC = 0.012     BIGBACC = 0.0028    CIGBACC = 0.002
+NIGBACC = 1         AIGBINV = 0.014     BIGBINV = 0.004     CIGBINV = 0.004
+EIGBINV = 1.1       NIGBINV = 3         AIGC   = 0.012      BIGC   = 0.0028
+CIGC   = 0.002
*+AIGS   = 0.012      BIGS   = 0.0028     CIGS   = 0.002
+NIGC   = 1          POXEDGE = 1         PIGCD  = 1          NTOX   = 1
*+AIGD = 0.01         BIGD   = 0.003      CIGD   = 0.0015
+XRCRG1 = 12         XRCRG2 = 5
+CGSO   = 6.238E-010  CGDO   = 6.238E-010  CGBO   = 2.56E-011  CGDL   = 2.495E-10
+CGSL   = 2.495E-10   CKAPPAS = 0.03      CKAPPAD = 0.03      ACDE   = 1
+MOIN   = 15         NOFF   = 0.9        VOFFCV = 0.02
+KT1    = -0.37      KT1L   = 0.0        KT2    = -0.042     UTE    = -1.5
+UA1    = 1E-009     UB1    = -3.5E-019  UC1    = 0          PRT    = 0
+AT     = 53000
+FNOIMOD = 1         TNOIMOD = 0
+JSS    = 0.0001     JSWS   = 1E-011     JSWGS  = 1E-010     NJS    = 1
+IJTHSFWD= 0.01      IJTHSREV= 0.001     BVS    = 10         XJBVS  = 1
+JSD    = 0.0001     JSWD   = 1E-011     JSWGD  = 1E-010     NJD    = 1
+IJTHDFWD= 0.01      IJTHDREV= 0.001     BVD    = 10         XJBVD  = 1
+PBS    = 1          CJS    = 0.0005     MJS    = 0.5        PBSWS  = 1
+CJSWS  = 5E-010     MJSWS  = 0.33       PBSWGS = 1          CJSWGS = 3E-010
+MJSWGS = 0.33       PBD    = 1          CJD    = 0.0005     MJD    = 0.5
+PBSWD  = 1          CJSWD  = 5E-010     MJSWD  = 0.33       PBSWGD = 1
+CJSWGD = 5E-010     MJSWGD = 0.33       TPB    = 0.005      TCJ    = 0.001
+TPBSW  = 0.005      TCJSW  = 0.001      TPBSWG = 0.005      TCJSWG = 0.001
+XTIS   = 3          XTID   = 3
+DMCG   = 0E-006     DMCI   = 0E-006     DMDG   = 0E-006     DMCGT  = 0E-007
+DWJ    = 0.0E-008   XGW    = 0E-007     XGL    = 0E-008
+RSHG   = 0.4        GBMIN  = 1E-010     RBPB   = 5          RBPD   = 15
+RBPS   = 15         RBDB   = 15         RBSB   = 15         NGCON  = 1
+JTSS   = 1E-4       JTSD   = 1E-4       JTSSWS = 1E-10      JTSSWD = 1E-10
```

```
+JTSSWGS = 1E-7        JTSSWGD = 1E-7
*+NJTS    = 20.0       NJTSSW  = 15         NJTSSWG = 6          VTSS   = 10
*+VTSD    = 10         VTSSWS  = 10         VTSSWD  = 10
*+NJTSD   = 15.0       NJTSSWD  = 20        NJTSSWGD = 6
*+TNJTS   = 0.1        TNJTSD  = 0.05
*+VTSSWGS=2 VTSSWGD=2
*+XTSS = 0.02 XTSD = 0.02 XTSSWS = 0.02 XTSSWD = 0.02 XTSSWGS = 0.02 XTSSWGD = 0.02
```

APPENDIX B: EKV MODELS

The model is used in 3-Bit ADC

180nm n-MOSFET

```
.MODEL N180_EKV nmos
* Flags
*+ SIGN = 1 TG = -1
* Scale parameters
*+ SCALE = 1.0 XL = 0.0 XW = 0.0
* Cgate parameters
+ COX = 8.58E-3
*GAMMAG = 18.4 AQMA = 0.0 AQMI = 0.0 ETAQM = 0.75
* Nch. parameters
+ VTO = 400.0E-3
*PHIF = 450.0E-3
+GAMMA = 300.0E-3 XJ = 30.0E-9 N0 = 1.025
* Mobility
+ KP = 390.0E-6 E0 = 438.0E+6
*E1 = 159.0E+6
+ETA = 0.57
*ZC = 1.0E-6 THC = 0.0
* Source and Drain Charge Sharing
+ LETA0 = 1.0E+6 LETA = 1.3
*LETA2 = 0.0
+WETA = 1.0
*NCS = 0.5
* DIBL (Drain Induced Barrier Lowering)
*+ ETAD = 0.75 SIGMAD = 1.0
* RSCE (Reverse Short Channel Effect)
*+ LR = 100E-9 QLR = 580E-6 NLR = 100.0E-3 FLR = 2
* INWE (Inverse Narrow Width Effect)
+ WR = 80.0E-9
*QWR = 500.0E-6 NWR = 12.0E-3
* Series resistance
*+ RLX = 170.0E-6
* Overlap & fringing
*+ LOV = 25.0E-9 GAMMAOV = 5.0 VFBOV = 0.0 KJF = 150.0E-12 CJF = 300.0E-3
* Long-ch. gds degr.
+ PDITS = 2.58E-6 PDITSD = 0.91 PDITSL = 0.0 FPROUT = 1.85E+6
*DDITS = 0.1
* Matching par.
+ AVTO = 0.0 AKP = 0.0 AGAMMA = 0.0
* Vsat & CLM (Channel Length Modulation)
+ UCRIT = 5.0E+6 DELTA = 1.5 LAMBDA = 0.5
*ACLM = 0.85
* Gate current (IGS, IGD, IGB)
*+ KG = 50.0E-6 XB = 5.5 EB = 21.0E+9 LOVIG = 40.0E-12
* Temperature par. scaling
+ TNOM = 30.0 TCV = 600.0E-6 BEX = -1.6
*TE0EX = -4.15 TE1EX = 0.0
*+ TETA = 2.0E-3 UCEX = 1.2 TLAMBDA = 0.15 TCVL = 0.0 TCVW = 0.0 TCVWL = 0.0
* Geometrical par. scaling
+ DL = -16.7E-9 DLC = -23.0E-9 LL = 0.0    DW = -45.3E-9 DWC = 0.0
*LDW = 0.0 WDL = 0.0
+ LLN = 1.0
```

180nm p-MOSFET

```
.MODEL P180_EKV PMOS
* Flags
*+ SIGN = -1 TG = 1
* Scale parameters
*+ SCALE = 1.0 XL = 0.0 XW = 0.0
* Cgate parameters
+ COX = 8.80E-3
*GAMMAG = 300 AQMA = 400.0E-3 AQMI = 1.0 ETAQM = 0.75
* Nch. parameters
+ VTO = = -0.4
*PHIF = 452.0E-3
+GAMMA = 610.0E-3 XJ = 50.0E-9 N0 = 1.050
* Mobility
+ KP = 82.0E-6 E0 = 2.10E+6
*E1 = 760.0E+6 +ETA = 0.0 ZC = 1.0E-6 THC = 0.0
* Long-ch. gds degr.
+ PDITS = 0.0 PDITSD = 0.9 PDITSL = 0.0 FPROUT = 1.4E+6
*DDITS = 0.16
* Matching par.
+ AVTO = 0.0 AKP = 0.0 AGAMMA = 0.0
* Vsat & CLM par.
+ UCRIT = 5.5E+6 DELTA = 2.0 LAMBDA = 0.54
*ACLM = 0.83
* Geometrical par.
+ DL = -24.2E-9 DLC = -0.0E-9
*WDL = 7.0E-15
+LL = 0.0 LLN = 1.0 DW = -7.2E-9 DWC = 0.0
*LDW = 500.0E-18
* Charge sharing
+ LETA0 = 0.0 LETA = 1.0
*LETA2 = 0.0
+WETA = 1.0
*NCS = 1.0
* DIBL
*+ ETAD = 1.1 SIGMAD = 0.3
* RSCE
*+ LR = 55.0E-9 QLR = -2.9E-3 NLR = 11.0E-3 FLR = 1.34
* INWE
+ WR = 80.0E-9
*QWR = 4.5E-3 NWR = 14.5E-3
* Series resistance
*+ RLX = 700.0E-6
* Overlap & fringing
*+ LOV = 16.0E-9 GAMMAOV = 4.2 VFBOV = 0.0 KJF = 210.0E-12 CJF = 300.0E-3
* Gate current
*+ KG = 10.0E-6 XB = 5.5 EB = 21.0E+9 LOVIG = 3.0E-12
* Temperature par.
+ TNOM = 30.0 TCV = -1.250E-3 BEX = -850.0E-3
*TE0EX = 0.0 TE1EX = -4.0 TETA = 0.0
+ UCEX = 1.7
*TLAMBDA = 0.0 TCVL = 0.0 TCVW = 0.0 TCVWL = 0.0
```

APPENDIX C: AMI GATE CAPACITANCE MODEL

This is used in chapter 2

AMI Gate Capacitance Model, *"Star-Hspice Manual - Release 2001.2 - June 2001".*

Define:

$vgst = vgs - \frac{(vth + vfb)}{2}$	$cox = \frac{cox}{TOX \cdot 1e\text{-}10} \cdot Weff \cdot Leff$	$Leff = L + XL - 2 \cdot LD$	$Weff = W + XW - 2 \cdot WD$

I-The gate capacitance *CGS*

$$arg = vgst \cdot \frac{(3 \cdot vgst - 2 \cdot vds)}{(2 \cdot vgst - vds)^2}$$

1	(vth + vfb)/2 > vgs		$cgs = 0$
2	(vth + vfb)/2 <vgs <vth	For vgst < vds,	$cgs = \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$
		For vgst > vds,	$cgs = arg \cdot \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$
3	vgs > vth	For vgst < vds	$cgs = \frac{2}{3} \cdot cox$
		For vgst > vds	$cgs = arg \cdot \frac{2}{3} \cdot cox$,

II-The gate capacitance CGD

$$arg = (3 \cdot vgst - vds) \cdot \frac{(vgst - vds)}{(2 \cdot vgst - vds)^2}$$

1	vgs < vth or vgs > vth and vgst < vds	$cgd = 0$
2	vgs > vth and vgst > vds	$cgd = arg \cdot \frac{2}{3} \cdot cox$

III-The gate capacitance CGB

$$cgb = \frac{cgbx \cdot cd}{cgbx + cd}$$

$$cgbx = cox - cgs - cgd$$

$$cd = \frac{esi}{wd} \cdot Weff \cdot Leff$$

$$wd = \left(\frac{2 \cdot esi \cdot vc}{q \cdot NSUB}\right)^{1/2}$$

vc = *The effective voltage from channel to substrate (bulk)* , vc under various conditions:

1	vgs + vsb < vfb	$vc = 0$
2	vgs + vsb > vfb	$vc = vgs + vsb - vfb$
3	vgst > 0, vgs < vth, vgst < vds	$vc = \frac{1}{2} \cdot (vth - vfb) + \frac{3}{2} \cdot vgst + vsb$
4	vgst > 0, vgs < vth, vgst > vds	$vc = \frac{1}{2} \cdot (vth - vfb) + vgst + \frac{1}{2} \cdot vds + vsb$
5	vgs > vth, vgst < vds	$vc = vth - vfb + \frac{1}{2} \cdot vgst + vsb$
6	vgs > vth, vgst > vds	$vc = vth - vfb + \frac{1}{2} \cdot vds + vsb$

APPENDIX D: SI & CGS UNITS

The International System SI and the centimeter–gram–second system (CGS) units.

Quantity	SI	CGS
Force	1 Newton (N)	1 dyne (dyn) $= 10^{-5}$ N
Work, energy	1 Joule (J)	1 erg $= 10^{-7}$ J
Dynamic viscosity	1 Pa·s	1 Poise (P) $= 0.1$ Pa·s
Kinematic viscosity	1 m^2/s	1 Stokes (St) $= 10^{-4}$ m^2/s
Pressure	1 Pascal (Pa)	1 barye (ba) $= 0.1$ Pa
Charge	1 Coulomb (C)	1 esu $= 10/c \approx 3.3356 \cdot 10^{-10}$ C
Current	1 Amperes (A)	1 esu/s $= 10/c \approx 3.3356 \cdot 10^{-10}$ A
Voltage	1 Volt (V)	1 Statvolt $= 10^{-8}c \approx 300$ V
Resistance	1 Ohm (Ω)	1 s/cm $= 10^{-9}c^2 \approx 9 \cdot 10^{11}\,\Omega$
Capacitance	1 Farad (F)	1 cm $= 10^9/c^2 \approx 10^{-11}/9$ F
Magnetic field strength	1 A/m	1 Oersted (Oe) $= 10^3/(4\pi) \approx 79.6$ A/m
Magnetic flux density	1 Tesla (T)	1 Gauss (G) $= 10^{-4}$ T
Magnetic flux	1 Weber (Wb)	1 Maxwell (Mx) $= 10^{-8}$ Wb

Semiconductors data at room temperature.

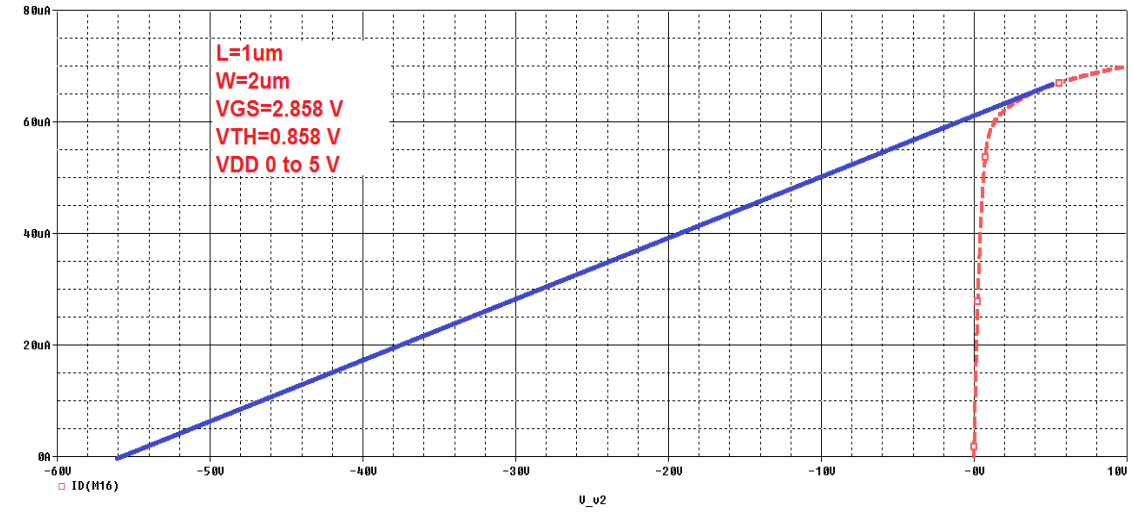
			Effective mass,[a] m_0		Mobility, $cm^2/V\,sec$		
Semiconductor	E_g, eV	Band	m_e^*	m_h^*	μ_e	μ_h	ϵ
Ge	0.66	I	0.57	0.37	3900	1900	16.0
Si	1.12	I	1.08	0.59	1400	450	11.9
GaAs	1.42	D	0.063	0.53	8800	400	12.9
GaP	2.26	I	0.8	0,83	250	150	11.4
GaN	3.44	D	0.22	0,61	8500	400	10.4

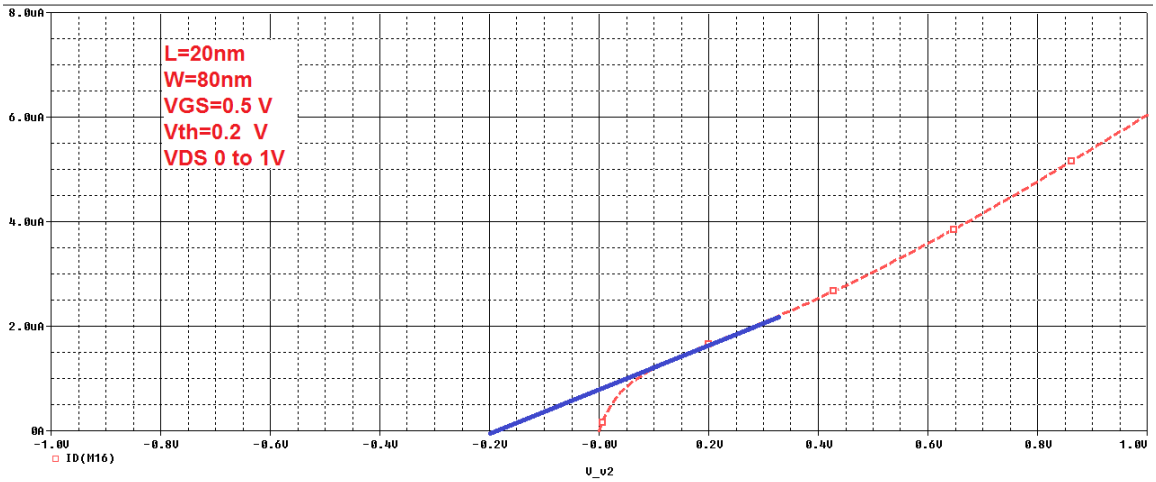
[a] Effective mass

APPENDIX E: LAMBDA CALCULATION

Lambda Estimating for 1um and 20nm n-MOSFET

1. Set n-MOSFET parameter and assign the device sizes and types.
2. VGS=V_{DD}/2+Vth, therefore the device in saturation from at V_{DS}=V_{DD}/2 and above.
3. V_{DS} have a DC voltage of sweep from 0 to 5 V.
4. Run the simulation which will produce the I_{DS}-V_{DS} characteristic.
5. Find Early Voltage V_A when I_{DS} =0.
6. The reciprocal of Early Voltage is λ.
    - For 1µm n-MOSFET $|V_A|$ = 55 V , λ=0.018 V^{-1}
    - 20 nm n-MOSFET $|V_A|$ = 17 V , λ=0.058 V^{-1}





Done by God's goodness