2-1-2016

Efficiency Enhancement of Micro-Thermoelectric Generators via Scaling and Minority Carrier Extraction

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Thermoelectric generators (TEGs) are solid state devices (no moving parts) that directly convert thermal energy into electrical energy utilizing thermoelectric phenomena known as the Seebeck and Peltier effect. TEGs have been studied over the past 100 years as a possible energy generation and cooling technology. Interest in TEGs has become considerably popular in the last 10-15 years due to the awareness of climate change, environmental issues, and advancement in material fabrication. TEGs can recover energy from waste heat, the byproduct of many industrial/commercial processes, an example of which is automobiles, where waste heat accounts for ~30% of energy losses. However, relatively low efficiencies have limited TEG application to niche areas. Significant increase in the efficiency is necessary before TEGs can be implemented in widespread applications.

In this work, the effects of scaling the dimensions of a TEG are analyzed using finite element modeling in Synopsys Sentaurus software. Temperature dependent material parameters and a thermodynamic model are utilized to determine the output power and efficiency of Silicon and Silicon Germanium TEGs for dimensions ranging from 1 mm to 5 nm and operating temperatures from 300 K to the melting temperature. The role of minority carriers is examined using TEG designs which utilize built-in electric fields to extract generated minority carriers and transport them to a corresponding majority carrier area.

Temperature dependent material parameters are critical for modeling TEG operation at high temperatures. TEGs can be tailored to achieve optimum efficiency and power generation depending upon operating temperature and dimensions. Large aspect ratios at small dimensions exhibit the greatest power density suggesting that nanowire TEGs are a possible option for waste heat recovery. Results show that minority carriers are one of the TEG performance limitations at higher temperatures. TEG geometries that use PIN junctions are able to extract and transport minority carriers to their corresponding majority carrier leg. Extraction decreases the minority carrier density improving efficiency at higher temperatures due to reduced recombination. If leg widths are scaled down, depletion of majority carriers occurs for lower operating temperatures. Depletion can be minimized by converting PIN junction into PN junctions.

Nicholas E Williams - University of Connecticut, 2016

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Nicholas E Williams
University of Connecticut, 2010

A Dissertation

Submitted in Partial Fulfillment of the

Requirements for the Degree of

Doctor of Philosophy

at the

University of Connecticut

2016

APPROVAL PAGE

Doctor of Philosophy Dissertation

Efficiency Enhancement of Micro-Thermoelectric Generators via Scaling and Minority Carrier Extraction

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University of Connecticut

2016

Acknowledgments

I would like to thank my mother Susan Fagan, my father Arthur Williams, my step-mother Ginger Williams, and my step-father Mark Fagan for their support of my education over the years. I would also like to thank my wife Fay Lynn who has been with me and supported me since the beginning of my undergraduate degree.

I would like to thank my advisors, Prof. Helena Silva and Prof. Ali Gokirmak for their mentorship and guidance during my Ph.D. I would also like to thank Prof. Rajeev Bansal, Prof. Michael Pettes, and Prof. Quing Zhu for being on my advisory committee.

I would like to thank my former and current labmates; accordingly I thank Adam Cywar for training me when I first started my Ph.D., for being my roommate for two years, and for various jam sessions/cook-outs, Sadid Muneer for discussions on modelling semiconductor physics which have been extremely helpful for my thesis, Azer Faraclas for numerous arguments/discussions on a variety of topics and for introducing me to Settlers of Catan, Gokhan Bakan for showing everyone what it means to be a Ph.D student, Mustafa Akbulut for teaching me how to use Synopsys Sentaurus and for helping to debug its numerous problems, Niaz Khan, Sean Fischer, Nadim Kanan, Kadir Cil, Abdiel Rivera, Nafisa Muneer, Luca Lucera, Nabila Adnane, Zachary Woods, Zoila Jurado, Lindsay Sullivan, Jon Rarey, Jacob Scoggin, Lhacene Adnane, and Sencer Ayas for their help and insight during my Ph.D.

I would like to acknowledge my graduate fellowship from the Department of Education.

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1 Introduction

1.1 Thermoelectric Generators

Thermoelectric generators (TEGs) are solid state devices that convert thermal energy to electrical energy. A TEG is composed of a pair of n-type and p-type semiconductor legs that are connected via a top metal wire (Figure 1.1). Individual TEGs are electrically connected in series and parallel to achieve a desired output voltage/current and they are enclosed inside a ceramic or metallic material that is electrically isolated but thermally conductive. The assembled device consisting of multiple TEG units is known as a TEG module. If a constant temperature difference (heat flux) is applied across a TEG then electrical power can be delivered to an external load. Alternatively, if electrical energy (electric current) is applied to the TEG then heat is transferred from one side of the TEG to the other establishing a temperature difference. When a TEG is operated in this fashion, it is known as a Peltier cooler.

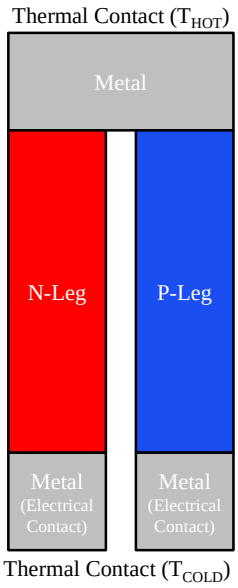

Figure 1.1 2D diagram of a thermoelectric generator.

Functional TEGs were first reported in the early 20th century where they were used in gas powered radio systems[1]. TEGs converted the heat generated from burning gas into a DC power source for the radio allowing for mobile radio operation. The commercialization of TEGs was hampered by low efficiencies as early TEGs were composed of metal alloys which are highly inefficient thermoelectric materials[2]. During the 1940-50s, improvements in semiconductor fabrication and synthesis resulted in the use of semiconductor materials with larger Seebeck coefficients[2] (on the order of ±100 μV/K). The introduction of new materials led to TEGs with efficiencies of ~5% and Peltier coolers that achieved cooling below 273 Kelvin. The increase in efficiency led to the possibility of thermoelectric cooling for food and air conditioning[3]. Although TEGs could not outperform conventional freon cooling systems, they were able to succeed in niche applications where size constraints, portability, and modularity are primary concerns.

In the 1960-70s TEGs were adapted for use in outer space or extreme cold[2] where conventional power sources (batteries or gas generators) do not function well. In these cases, TEGs convert the waste heat generated by the decay of a radioactive isotope into electrical energy and these types of devices are known as radioisotope thermoelectric generators (RTGs)[4]. RTGs are used on deep space missions to power space probes[5] (such as Voyager 2[6] and Pioneer 10[7]) where solar cells cannot provide significant energy at such distances away from the Sun. Space probes can be powered by an RTG for ~ 50 years before the energy output of the RTG no longer powers the onboard electronics. RTGs are still the standard deep space power supply choice for NASA[8, 9].

In the past 20 years, concerns with climate change, rising fossil fuel costs, and environmental regulations have renewed research into TEGs for waste heat energy

recovery. Recent advances in engineering thermoelectric materials with figure of merit (ZT) greater than 1 have improved the outlook for TEGs for direct thermal-electrical energy conversion and solid-state cooling[10-14]. There is considerable interest in widespread integration of TEGs into systems where waste heat is a significant by-product such as automobiles, power plants, and factories[15]. TEG equipped cars with improved fuel efficiencies have been designed by several companies such as Hyundai, GM[16], BMW[17], and Volkswagen[18]. BMW has reported a 5% net increase in fuel efficiency for TEG equipped vehicles cruising at highway speeds[19]. The US Department of Energy has a target efficiency of 10% at which it will promote integration of TEG modules on all existing large trucks[19]. TEG coolers/heaters are already incorporated into automobile seats to provide local, more efficient cooling or heating. However, significant enhancement of TEG efficiency is required before TEGs will be implemented in large-scale waste heat recovery systems.

1.2 Thermoelectric Effects

TEGs operate based on a set of physical phenomena known as thermoelectric effects which were discovered ~75 years before the construction of the earliest TEGs. They convert thermal flux into electric energy via two related thermoelectric mechanisms, the Peltier effect and Seebeck effect.

1.2.1 Seebeck Effect

The Seebeck effect is named after Thomas Johann Seebeck who in 1821 observed that a compass needle was deflected when a closed loop circuit composed of two dissimilar metals was heated at one junction[20]. The temperature difference between the two junctions results in an electric potential (Seebeck voltage) which under closed circuit conditions drives a net current flow. This net current flow was responsible for deflecting the compass needle due to induced magnetic field. The magnitude and polarity of the electric potential generated is related to the temperature difference by the equation,

$$\Delta V = S \cdot (T_H - T_C)$$

where S is the Seebeck coefficient, T_H and T_C are the hot and cold side temperature respectively[2]. The Seebeck coefficient is a material property which is highly dependent upon the absolute temperature, temperature gradient, and material composition. The above formula is commonly rewritten as,

$$S = \frac{\Delta V}{\Delta T}$$

where ΔT is $T_H - T_C$. Generally, the Seebeck coefficient is measured using a small temperature difference ($\Delta T \approx$ 5-10 K) where the average temperature of the material is raised to determine the absolute temperature dependence.

In semiconductors the Seebeck effect can be observed in a single material system when a temperature gradient is formed across a material. In the case of an n-type semiconductor, majority carriers (electrons) at the hot end of the temperature gradient diffuse to the cooler side and in open circuit conditions this leads to an electrostatic potential (Seebeck voltage) across the temperature gradient. For a closed circuit, the diffusion of electrons results in a short circuit current. N-type semiconductors have a negative Seebeck coefficient as the electrostatic potential as measured from hot to cold is negative whereas the opposite is true for p-type semiconductors. At lower temperatures, the effective Seebeck coefficient is determined by the majority carrier type as minority carrier contribution is mostly negligible. For higher temperatures the magnitude of the Seebeck coefficient decreases when the Seebeck contribution from thermally generally minority carriers (which have opposite polarity to majority carriers) cancels out the contribution from majority carriers. When a heat source is applied to the TEG, majority carriers diffuse to the cool end resulting in a net current if a load is attached (Figure 1.2).

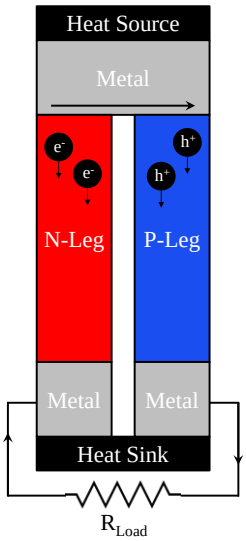

Figure 1.2 Thermoelectric generator diagram.

1.2.2 Peltier Effect

The Peltier Effect was first observed in 1843 by Jean Charles Peltier who saw that an electric current passing through a junction of dissimilar metals could heat or cool the junction depending upon the direction of current[21]. This effect was also observed by Emil Lenz in 1938 when he froze water or melted ice by passing current through a bismuth-antimony junction[22]. The heat generated or absorbed at the junction of two dissimilar conductive materials is written as,

$$Q_{Peltier} = (\pi_1 - \pi_2) \cdot J$$

where J is the current density through the junction interface, and π_1 and π_2 are the Peltier coefficients (total energy of the free carriers) for each respective material[2]. For semiconductors, the Peltier effect can be observed when a current passes through a semiconductor-semiconductor or metal-semiconductor interface (where there are differences in Peltier coefficient).

The Peltier coefficient is proportional to the Seebeck coefficient and temperature and it is defined by the Thomson relation,

$$\pi = S \cdot T$$

where S is the Seebeck coefficient. The Thomson relation, stated in 1854 by Lord Kelvin (Sir William Thomson, also its namesake), shows the fundamental link between the Peltier and Seebeck effects[23].

If a TEG is operated in reverse, where a current is applied to the structure without the presence of a temperature gradient (from a heat source), it is known as a Peltier cooler (Figure 1.3).

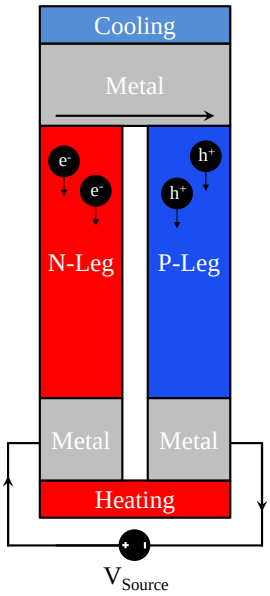

Figure 1.3 Peltier cooler diagram.

In a Peltier cooler, the Peltier effect is exploited to create a temperature gradient across the structure. A current passing through the structure as shown cools and heats at the various semiconductor-metal junctions resulting in a net temperature gradient from top to bottom. If the current direction is reversed, then the temperature gradient also reverses. When a heat sink is applied to the hot side to remove the generated heat, the cool side can be used for active cooling. Without a heat sink, the heat cannot be removed and it diffuses to the cool side eventually eliminating the temperature gradient.

1.2.3 Thomson Effect

When a current passes through a material which has a temperature gradient (and subsequently a Seebeck coefficient gradient) charge carriers transfer heat and modify the temperature distribution. This phenomenon is known as the Thomson Effect and it was first observed in 1851 by Lord Kelvin[23]. He heated the bottom of a U-shaped metal rod (Figure 1.4, point C) creating a temperature gradient from C to B and C to A while measuring the resistance of two wires wrapped around sections of the metal rod[24].

Without a current flowing through the metal rod, the two wires resistances were equivalent but when a current was passed through the rod the wire resistances were no longer equal. The current passing through the metal rod shifted the temperature gradient along the rod creating a difference in temperature of each metal wire (reducing temperature of one, increasing temperature of the other). The asymmetry of the temperature profile resulted in a difference of metal wire resistance (temperature coefficient of resistivity for metals).

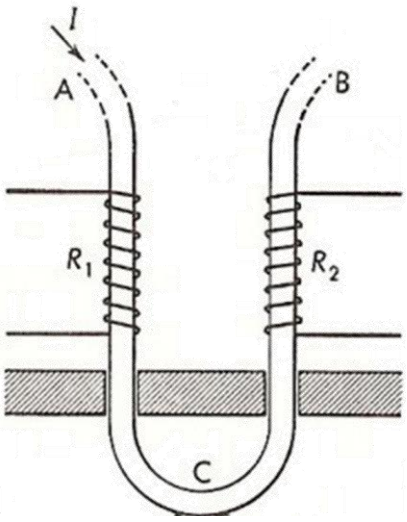

Figure 1.4 Experimental setup of original Thomson effect observation[24].

The heat exchange rate caused by a current flowing through a temperature gradient is written as[2],

$$Q_{Thomson} = -K \cdot \vec{J} \cdot \nabla T$$

where K is the Thomson coefficient,

$$K = T\frac{dS}{dT}$$

The Thomson Effect can be thought of as a continuous form of the Peltier Effect as a spatial gradient in Seebeck coefficient implies a spatial gradient in Peltier coefficient as well. The

gradient in the Peltier coefficient results in carriers absorbing and releasing energy as they travel through the material skewing the temperature gradient.

Semiconductors exhibit the same Thomson Effect behavior as observed in metals (asymmetric temperature profile). Thomson Effect is relevant when high current density and large temperatures/temperature gradients are expected such as in phase change memory[25-27]. In these cases, asymmetric temperature gradients can result in unexpected device operation (asymmetric amorphization in phase change memory [28]).

1.3 ZT – Thermoelectric Figure of Merit

The thermoelectric efficiency of a material is characterized by the unitless figure of merit ZT[2, 22],

$$ZT = \frac{\sigma S^2 T}{k_e + k_p}$$

where σ is electrical conductivity, S is Seebeck coefficient, T is temperature, k_e and k_p are electrical and phonon thermal conductivity respectively. An ideal thermoelectric material would have low total thermal conductivity ($k_e + k_p$) and a large electrical conductivity and Seebeck coefficient. However, an ideal material is hard to realize as optimizing for any one material parameter (k, S, or σ) usually results in degradation of one or more of the other parameters. For example, metals generally have large electrical conductivity but their Seebeck coefficient is small and electronic thermal conductivity is large. Conversely, insulators have very low thermal conductivity but extremely low electrical conductivity. Furthermore, k, S, or σ are all temperature dependent (making ZT temperature dependent), resulting in a peak ZT for only a small range of temperature. Semiconductors are the best candidates for thermoelectric materials as doping, composition, and physical structure can

be manipulated. For any particular semiconductor, the figure of merit is analyzed for both p-type and n-type as TEGs are composed of both dopant types.

The most commonly used thermoelectric material is Bismuth Telluride (Bi_2Te_3) as it has a relatively large Seebeck coefficient (n-type ≈ -170 μV/K, p-type ≈ 160 μV/K), electrical conductivity (n-type ≈ $1.655 \times 10^3\ \Omega^{-1}\ cm^{-1}$, p-type ≈ $1.4 \times 10^3\ \Omega^{-1}\ cm^{-1}$) and low thermal conductivity (~3 W/mK) resulting in a room temperature ZT value for both p and n-type bulk Bi_2Te_3 of ≈ 0.9-1[29]. Further enhancement of ZT for Bi_2Te_3 has been achieved using nanostructures[30], sintering to achieve nano-sized grains[29], nanocomposites[31], alloying[13], band gap tuning[32], and impurity optimization[2]. Generally these methods are employed to either increase the Seebeck coefficient or to decrease the lattice thermal conductivity (via increased phonon scattering at interfaces) without reducing electrical conductivity. Peak ZT improvements of up to ~1.5 for p-type and 1.1 for n-type Bi_2Te_3 were reported where the peak values occur between 300 to 400 K[33]. Outside of the of peak value, ZT drops off relatively sharply.

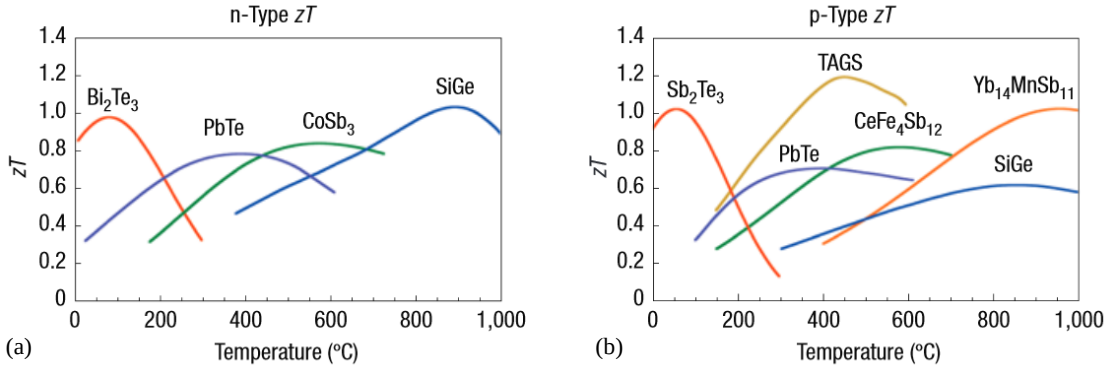

Figure 1.5 Reported ZT values for n-type (a) and p-type (b) thermoelectric materials[33].

ZT has also been reported[33] for a number of other thermoelectric materials of interest (Figure 1.5) and a peak ZT value of ~1 is achievable for a variety of materials at

different temperature ranges. Improvements in ZT for these materials also used similar enhancement methods as for Bi_2Te_3. Research continues today to find new classes of materials which may yield larger ZT values. Integration of TEGs into commercial and industrial energy systems is estimated to require ZT values of 1.5 – 10+ (Table 1.1)[34]. Thus significant improvement in ZT is required as even the best reported materials have a peak ZT of ~1.5.

Power Scale (kW)	Examples	Required ZT	Impact on climate crisis
1000+	Solar thermal replacement	> 8 - 20	Highly Unlikely
10+	Industrial waste heat	> 4	Unlikely
0.5+	Vehicle waste heat, car cooling/heating, home co-generation	> 1.5 - 2	TBD
<0.5	Remote power, ''personal' micropower	> 0.5 - 1	(almost) None

Table 1.1 Required ZT values for thermoelectric materials and potential impact on climate crisis. [34].

It is important to note that ZT is often used to evaluate a materials thermoelectric efficiency without actually creating a TEG from the particular material being tested. Efficiency optimization for a TEG encompasses not only the ZT of the material (n-type and p-type) but also dimensions of the leg height and width, thermal shunting losses, and quality of metal/semiconductor contacts. A more generalized TEG efficiency[1] written as,

$$n = \frac{P_{out}(W)}{Heat\ Flux(W)}$$

is used to evaluate the performance of the simulated TEGs in this work. Heat Flux refers to the amount of thermal energy that is absorbed by the hot contact while P_{out} refers to the amount of electrical power delivered to a load attached to the TEG.

In this work, we attempt to address TEG efficiency without consideration for the ZT of the thermoelectric materials but instead by analyzing scaling, semiconductor transport, the role of majority/minority carrier concentrations, and novel device designs. Future enhancement of TEG efficiency will require not only ZT improvements but also novel and unique approaches to TEG design that boost performance.

1.4 Micro-Thermoelectric Generators

Commercially available TEGs[35] (Figure 1.6) are relatively large devices with module areas of ~1-10 cm^2 and TEG leg widths and heights ranging from 1 mm to 1 cm. These dimensions are considerably larger than modern semiconductor devices whose critical dimensions are < 100 nm. With the advent of transistor scaling into μm and nm regions, TEGs can be constructed using leg dimensions from hundreds of μm to tens of nm (MicroTEGs or μTEGs). μTEGs are of interest for on chip, spot cooling to improve the performance and reliability of microprocessors[36]. Spot cooling of a 3.5 x 3.5 mm^2 area by 15° K has been reported[37] using a superlattice based thermoelectric Peltier cooler composed of nanostructured Bi_2Te_3. μTEGs decreased leg dimensions can result in nanoscale effects such as 2D/1D carrier confinement and reduced thermal conductivity which may improve performance (increased output power/efficiency). Recent reports on silicon nano-structures[38] or nanostructured[39] silicon with ZT values close to 1 suggest possible use of silicon for CMOS compatible TEGs. Silicon nanowires (Si NW) with widths of ~ 10 nm were reported to have thermal conductivity of 0.76 $Wm^{-1}k^{-1}$, below the limit of bulk disordered crystals of ~ 1 $Wm^{-1}k^{-1}$[40].

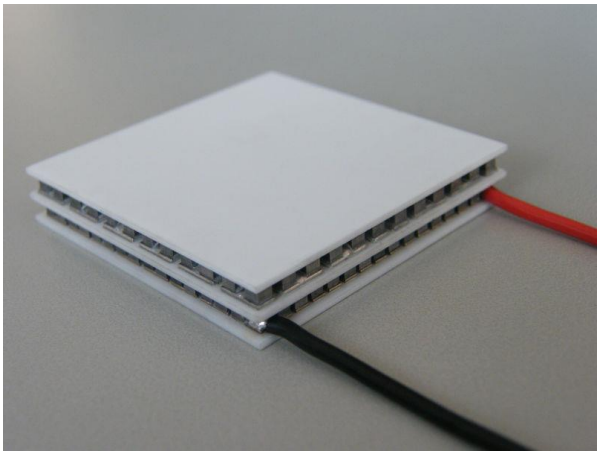

Figure 1.6 Example of commercially available TEG[35]. Individual TEG legs can be observed inside of the white electrically insulating top and bottom layers. Module is ~ 5 cm x 5 cm with individual TEG units with leg height and width of ~ 5 mm.

Li *et al*[41] have demonstrated a Silicon nanowire based TEG module composed of 540 x 540 bundles of vertically aligned nanowires with a diameter of 80 nm and height of 1 μm. μTEGs composed of Bi_2Te_3 and fabricated on flexible substrates have been reported by Schwyter *et al*[42] with leg heights of 100 – 300 μm and widths of 50 – 150 μm. A flexible substrate allows for the μTEG to conform to a surface such as the human body and may be used to power microelectronics, miniature sensors, and MEMS type devices[2].

μTEGs offer an advantage over conventional energy conversion methods (‘engines’, mechanical system) as they demonstrate better efficiency for lower power applications[34] (Figure 1.7). The efficiency of mechanical energy conversion methods decrease once the power levels are on the order of mW and μW where TEGs are much more efficient in comparison. ZT improvements shift the trade off point between TEGs and conventional

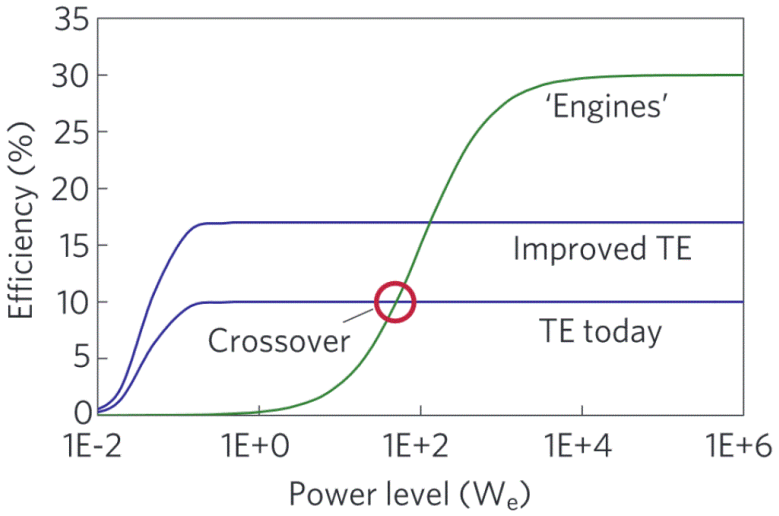

Figure 1.7 Efficiency of TEGs and 'Engines' as a function of power level. 'Engines' refers to mechanical systems which convert heat (and other energy sources) into electrical energy[34].

methods to higher power levels opening up the possibility of more TEG energy applications.

In conventional TEGs, the leg dimensions are such that all minority carriers that are generated are likely to recombine with majority carriers. When minority carrier density is significantly lower than majority carrier density, recombination (limited by minority carriers) has negligible impact on performance. Once minority carrier concentration is sufficiently large (higher average temperature) recombination results in performance degradation (decrease in Seebeck coefficient, reduction in contribution of majority carriers). μTEGs offer the possibility of exploiting decreased dimensions to reduce recombination.

1.5 Device Modeling

Modeling devices that operate at high temperatures and/or large temperature ranges is commonly done using effective media approximations. Effective media approximation (EMA) uses a simplified approach to the electrical transport where the current density is defined as:

$$J = \sigma \cdot E$$

where σ is electrical conductivity and E is electric field. σ is often an experimentally measured parameter which does not distinguish charge carriers (electrons and holes) and their mobility. Electro-thermal simulations using EMA are often used to model the operation of phase change memory (PCM). PCM stores information in the crystal phase of a chalcogenide semiconductor which can be reversibly changed between crystalline and amorphous. Changing the phase of the material requires heating to a crystallization temperature (> 423 K, amorphous to crystalline, SET) for a relatively long time or heating to the melting temperature (> 873 K, crystalline to amorphous, RESET) followed by rapidly cooling. Finite element software such as COMSOL Multi-Physics is used to simulate the RESET and SET operations of PCM using an EMA. This method gives reasonable results for PCM modeling but a more accurate approach would take into account the electronic band structure and charge carriers (electrons and holes).

Traditionally semiconductor devices are modeled using a drift-diffusion equation to describe electron (Jn) and hole (Jp) current density,

$$\overrightarrow{J_n} = -nq\mu_n\nabla\varphi_n,\ \overrightarrow{J_p} = -pq\mu_p\nabla\varphi_p$$

where μ_p and μ_n are hole and electron mobility, φ_n and φ_p are the electron and hole quasi fermi potentials, n and p are electron and hole density and q is electron charge. A drift-

diffusion based approach takes in account the electronic band structure, electron and hole density, and generation/recombination. Semiconductor device simulations however often do not consider operation for temperatures greater than 400-500 K. In the simplest cases, simulations are isothermal to reduce computation time associated with solving a Fourier heat equation and temperature dependence of material parameters. Synopsys Sentaurus is an industry standard, finite element software that can simulate the fabrication and operation of semiconductor devices. Synopsys Sentaurus includes several different current density models (drift-diffusion, thermodynamic, hydrodynamic, and Monte-Carlo), a variety of mobility, recombination, and band gap models, and a detailed material parameter database. The thermodynamic and hydrodynamic current density models allow for temperature dependent device simulations. Fabrication processes such as implantation, dopant diffusion, epitaxial growth, and etching can also be simulated to create realistic device geometries.

Using a semiconductor model for high temperature simulations is difficult due to a lack of measured material parameters at elevated temperatures. Measuring material parameters at high temperatures is difficult, requiring specialized equipment to accurately characterize relevant parameters. Semiconductor models usually extrapolate material parameters outside of the measured temperature range which can result in inaccurate results. EMAs avoid this problem by simplifying material parameters ($J = \sigma \cdot E$) and by allowing users to manipulate equation and models to approximate heat temperature behavior. For example, it is considerably easier to measure the electrical conductivity compared to measuring electron/hole mobility and density (which are required for semiconductor models). Although semiconductor models have problems accurately

simulating semiconductor behavior at higher temperatures, they can capture a variety of phenomena that EMA are unable to simulate. Semiconductor models can simulate effects such as the role of minority carriers, generation/recombination, and band gap which cannot be easily integrated into an EMA.

An example of an EMA simulation using COMSOL Multi-Physics and a full semiconductor device simulation using Synopsys Sentaurus are shown in Chapters 2 and 3 respectively.

2 Effective Media Approximation: Electro-Thermal Modeling of Set and Reset Operations of PCM Cells

2.1 Introduction

Phase change memory (PCM) is an emerging candidate for non-volatile storage class memory characterized by high density and fast writing and erasing speed[43]. PCM devices use localized heating from high current densities in order to transition between the crystalline (set) and amorphous (reset) states, which typically have ~10^2-10^4 times difference in resistance values. Scaling the device dimensions improves packing density, speed and power performance[44].

Finite element simulations of PCM cells provide insight into device operation and scaling, however studies to date typically do not report simulation of set operation and neglect latent heat of fusion (L_f) and temperature (T) dependence of material

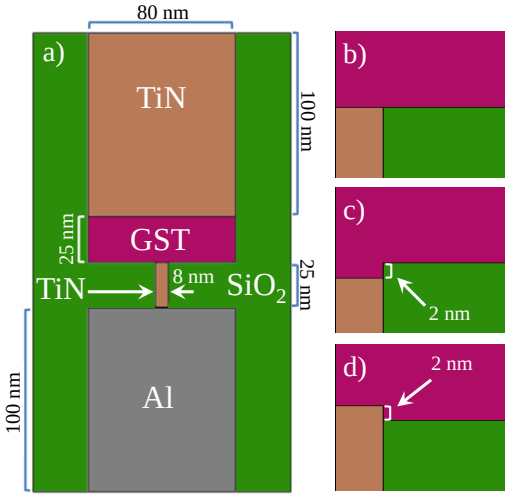

Figure 2.1. (a) Cross-section of planar mushroom cell geometry and materials. TiN-GST junction in (b) planar, (c) recessed, and (d) raised mushroom cells. In the recessed cell 2 nm of the TiN is replaced with GST so that the active region of the GST recedes into the oxide before contacting the TiN. The raised cell has an extra 2 nm of the TiN channel protruding into the active region of GST.

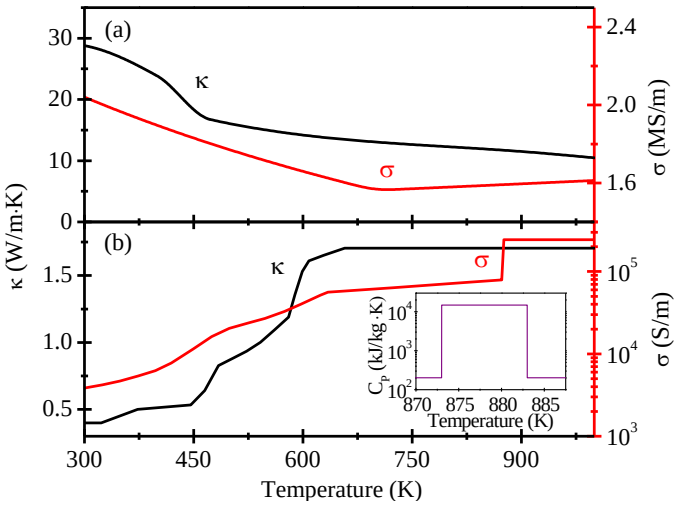

Figure 2.2. Temperature dependent thermal conductivity (κ), electrical conductivity (σ) and heat capacity (C_p) of (a) TiN and (b) c-GST. C_p includes a 10 K wide spike representing latent heat (L_f).

properties (electrical conductivity (σ), thermal conductivity (κ), heat capacity (C_p))[45]. In this study, set and reset operations of $Ge_2Sb_2Te_5$ (GST) mushroom cells are analyzed using COMSOL Multiphysics 2D finite element simulations with rotational symmetry[46], including temperature dependent κ(T)[47] and electric field dependent σ(T,E). Results on aggressively scaled planar mushroom cells and effect of possible process variations resulting in ± 2nm variation in TiN heater height are presented (Figure 2.1).

2.2 Simulations

Mushroom cells consisting of a cylindrical TiN pillar, with diameter (d) x height (h) = 8 nm x 25 ± 2 nm and a GST disk (d x h = 80 nm x 25 nm) (Figure 2.1a) are

	σ (S/m)	κ (W/m·K)	Cp (J/kg·K)
TiN	Fig. 2(a)	Fig. 2(a)	784
SiO_2	10.0 f	1.38	703
Al	37.7 M	160	900

Table 2.1. Simulation parameters used for TiN, SiO_2, and Al.

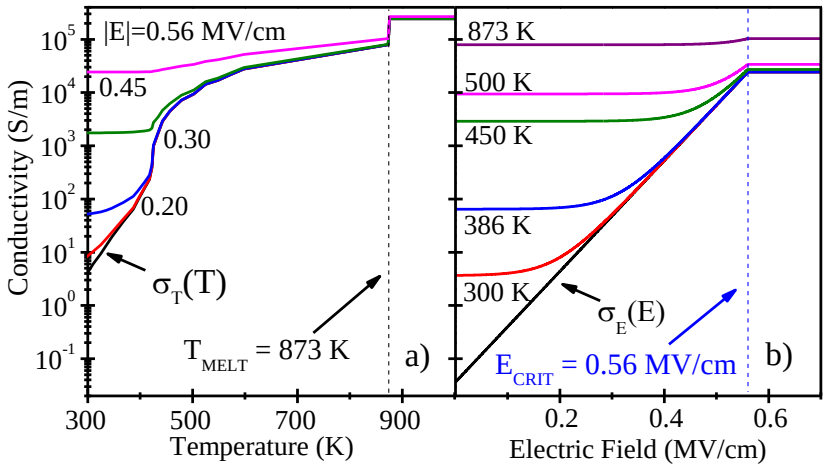

Figure 2.3. (a) Electrical conductivity, σ(T), of a-GST as a function of temperature with varying electric fields, and (b) electrical conductivity, σ(E), of a-GST as a function of electric field with varying temperatures.

simulated using the half-device geometries shown in Figure 2.1(b-d) with rotational symmetry around the left side and 1 kΩ series resistor. The constant parameters used for TiN, SiO_2, and Al are shown in Table 2.1. Temperature-dependent σ and k for TiN are shown in Figure 2.2a[48].σ-T data for crystalline GST (c-GST) (Figure 2.2b) are compiled from experimental results from Fallica et al. (from 300 K to 700 K)[49] and Endo et al. (from 883 K to 950 K)[50][50][50]. σ-T between 700 K and 883 K is interpolated using these two data sets. The heat capacity of GST (Figure 2.2inset) is included as a constant value of 202 J/(kg·K) with a 10 K wide plateau of 14.8 x 10^3 J/(kg·K) starting at melting temperature (873 K)[51] to account for L_f[52].

The resistance of the mushroom cell after reset is too high to allow sufficient joule heating without electrical breakdown. Hence, it is necessary to model electric field (E) dependence of σ of a-GST. Breakdown field of GST is E_{CRIT} = 0.56 MV/cm[53] and it is achievable for a-GST in typical cell operation. The total conductivity of a-GST is modeled as the combination of the electrical breakdown component, $\sigma_E(E)$, and the temperature

dependent conductivity, $\sigma_T(T)$, such that $\sigma(T,E) = \sigma_T(T) + \sigma_E(E)$. The electric breakdown component of electrical conductivity was not available in the literature at time of publication of this work but it is expected to increase exponentially with electric field[43, 54]. In this study $\sigma_E(E)$ is assumed to be an exponential function amounting to 1% of the room temperature conductivity of a-GST at zero field and 10% of the molten conductivity of GST at breakdown (E_{CRIT}):

$$\sigma_E(E) = 0.0364 \cdot e^{(|E| \cdot 239.5 x 10^{-9})} (S/m) \quad (1)$$

This practical assumption enables use of field to approximate electrical breakdown, which is responsible for self-heating of a-GST (Figure 2.3). The contributions of vertical (E_z) and radial field (E_r) dependent components were added separately [$\sigma_E(E) \approx \sigma_E(E_z) + \sigma_E(E_r)$] to minimize the simulation complexity. The error introduced by this simplification is expected to be insignificant due to relatively small contribution of E_r. Field dependence is neglected for c-GST since electric field is small due to high conductivity [$\sigma_T(T) >> \sigma_E(E)$]. The current continuity (2) and heat transport (3) equations are solved self-consistently in COMSOL Multiphysics: (2)

$$\nabla \cdot J = -\nabla \cdot (\sigma(T,E)\nabla V) = 0,$$

$$d_{GST} \cdot C_P(T)\frac{dT}{dt} - \nabla \cdot (\kappa(T)\nabla T) = \frac{J \cdot J}{\sigma(T,E)}, \quad (3)$$

where J is the current density, V is the electric potential, and d_{GST} is the mass density (Figure 2.4, Figure 2.5).

The applied voltage pulses for the reset and set operations have a total time of 1 ns and 20 ns respectively, with 200 ps rise/fall times. The reset pulse voltage is chosen such that at least 2 nm of GST is melted in any given direction from the conductive pillar (TiN).

The area of the GST which was heated above melting is assumed to be left in amorphous state upon resolidification. The set pulse voltage is chosen such that the entire amorphous region is over the crystallization temperature (423 K)[55] for approximately 20 ns.

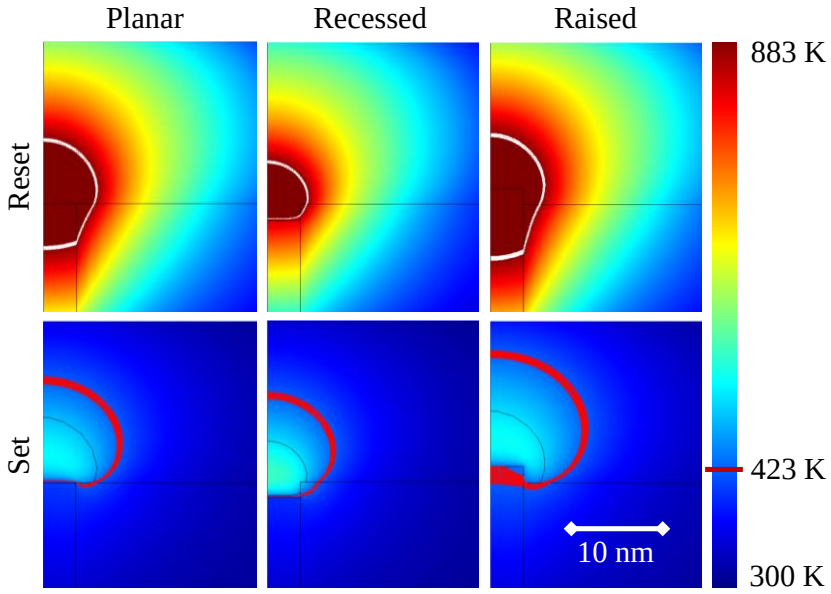

Figure 2.4. Peak thermal profile of mushroom cells during reset and set pulses. Contour lines are shown to denote the region which has reached the molten temperature (reset) and crystallization temperature (set).

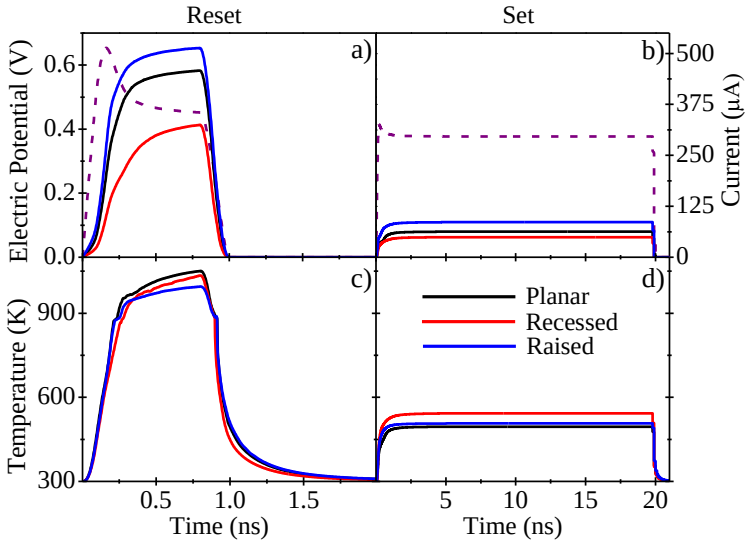

Figure 2.5. (a) Current (solid lines) during reset and (b) set operations with a standard voltage pulse (dashed lines). (c) Temperature during reset and (d) set operations.

2.3 Results

The 2nm recess (Figure 2.1) leads to reduced current, power, total energy consumption, and minimum pitch required to prevent the operations of one cell from affecting its neighbors (Table 2.2). The raised cell consumes more power due to increased current, despite a smaller voltage requirement. The set pulse consumes more energy than reset in all three cases despite lower power requirements due to 20 times longer pulse duration (Table 2.1).

When the results for the planar cell were compared to simulations using constant (commonly used, temperature and field independent) materials parameters[45] (Table 2.2, Table 2.3), the temperature independent model predicts 57.6 % less energy during the reset and 4.34 % less energy during the set pulse. The temperature independent model predicts 38 times more voltage required for the set operation since σ is significantly underestimated at elevated temperatures (Figure 2.2).

		Pulse time (ns)	Molten Volume (nm^2)	Applied V (V)	V_{peak} (V)	I_{peak} (μA)	T_{peak} (K)	P_{peak} (μW)	Total Energy (fJ)	Final R (Ω)	Minimum Pitch (nm)
Reset	Planar	1	787	0.91	0.654	458	1051	207	150	8.68 M	35
	Recessed	1	338	0.78	0.639	325	1035	148	98.9	14.5 M	32
	Raised	1	913	0.96	0.637	513	995	230	170	4.26 M	36
Set	Planar	20	-	0.44	0.406	62.8	495	23.7	461	15.2 k	16
	Recessed	20	-	0.47	0.444	49.3	543	20.7	403	26.4 k	14
	Raised	20	-	0.44	0.392	86.1	507	30.5	595	9.95 k	19

Table 2.2. Reset and set pulse time, volume melted, applied voltage across the resistor and cell, peak voltage across the cell (V), current (I), temperature (T), and power (P), total energy, resistance (R) after the pulse, and minimum pitch to ensure no interference in data from other cells.

	σ (S/m)	κ (W/mK)	C_p (J/kgK)
c-GST	2770	0.5	202
a-GST	3	0.2	202

Table 2.3. Common constant (room temperature) parameters for c-GST and a-GST.

It is important to note that thermoelectric effects have been excluded for simplicity, however these are expected to modify the temperature profile of the active region depending upon the electric polarity[28, 56]. Furthermore, the electrical and thermal boundary resistances[57, 58] have not been included, which would result in additional heat generation and confinement, reducing reset/set currents.

3 Semiconductor Modeling: Nanoscale RingFETs

3.1 Introduction

As critical dimensions of MOSFETs have shrunk below 50 nm, controlling leakage currents and off-state power has become the primary design challenge for each new generation[59]. A number of solutions, such as FinFETs[60, 61], Double Gates[62], accumulated-body[63], and gate wrap-around FETs[64] have been proposed to improve electrostatic control of the channel and suppress drain to source leakage currents[65] due to defects and positively charged traps in the side interfaces between the shallow trench isolation (STI) and the body. Improved electrostatic control reduces short channel effects (SCE) and suppression of leakage currents at the body-STI interface improves off-current (I_{OFF}), and enable use of narrower channel devices for higher packing density.

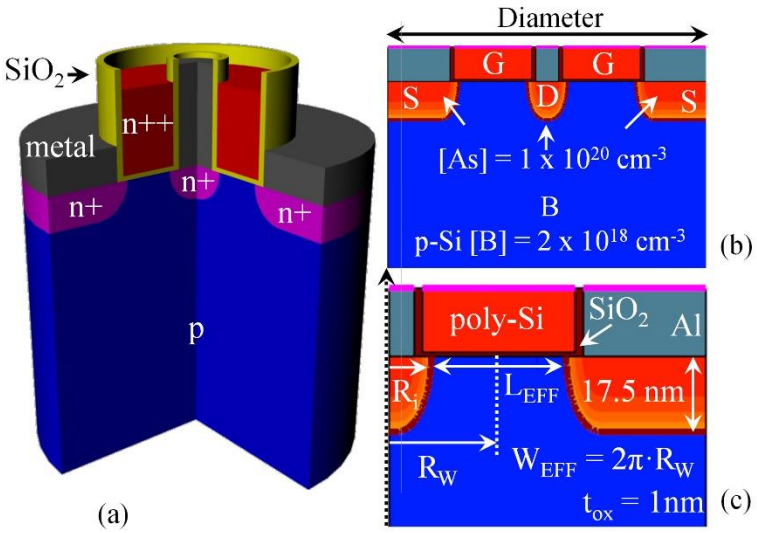

Figure 3.1. (a) 3D model of an n-channel RingFET (b) Full cross section of 3D RingFET showing example of drain on inner implanted region. (c) Radial cross section of RingFET showing relevant scaling parameters for width, and length. The cross section is rotated around the dashed arrow for the simulations. The gate has a 2 nm overlap on both sides of the channel.

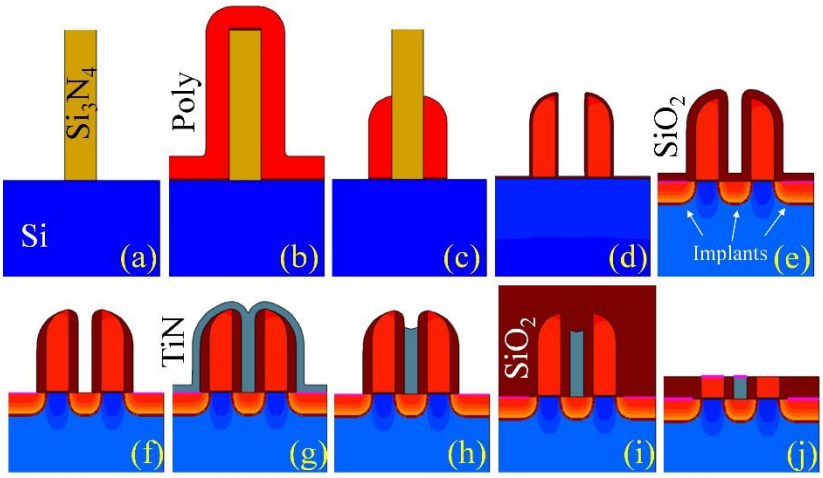

Figure 3.2. Proposed process setups; (a) lithography RIE Si_3N_4, (b) deposit SiO_2/poly, (c) RIE poly/ SiO_2, (d) grow SiO_2, (e) implant, deposit, SiO_2, (f) RIE SiO_2, (g) Deposite metal, (h) etch metal, (i) deposite SiO_2, (j) CMP

An alternative approach to eliminate leakage at the body-STI interface and suppressing SCE is to use a RingFET geometry, where the active area is defined by inner and outer contact regions, eliminating the side interfaces and achieving a strong divergence of drain field from the center to the edge at small scales. Furthermore, defect induced drain to substrate leakages at the STI interface[66] are eliminated when drain is defined on the inner contact. In this study, Synopsys Sentaurus TCAD[67] was used to perform 2D rotationally symmetric finite element simulations of nanoscale RingFETs (Figure 3.1) which can be fabricated using a self-aligned fabrication procedure (Figure 3.2). Large-scale RingFETs have previously been studied by others for power FETs to achieve high packing densities[68].

3.2 Simulation Results and Discussion

The Sentaurus hydrodynamic model with Phillips unified and normal electrical field mobility degradation, high field saturation, and Shockley-Read-Hall and Band-to-

Band recombination currents as a function of doping gradients was used to simulate RingFETs with three effective gate lengths (L_{EFF} = 22, 32, and 45 nm) and inner implanted region radius (R_i) from 5 to 25 nm with 5 nm increments (Fig. 1c). A 1 V supply was used for gate and drain. Gate dielectric of 1 nm SiO_2 with no tunneling current was used for all cases and 6.4 nm HfO_2, the same effective oxide thickness, was simulated for L_{EFF} = 22 nm and R_i = 10 nm for comparisons[69].

The source and drain regions of the RingFET are asymmetric. The relative difference in their size becomes significant as the devices are scaled down to sub-50 nm dimensions. Hence, the electrostatics and the I-V characteristics of the RingFETs depend on inner or outer drain as well as L_{EFF} and R_i.

A significant improvement in source-drain barrier is seen inner drain cases (Figure 3.3) since the drain fields diverge from the smaller inner contact and the source barrier is predominantly controlled by the source, gate, and body potentials. This results

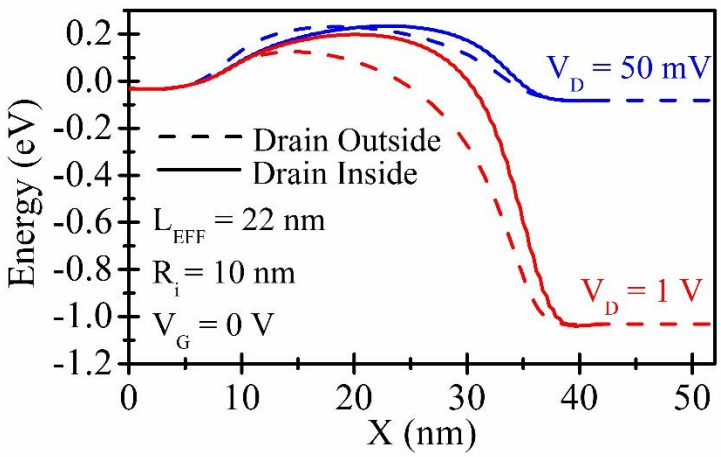

Figure 3.3. Source-Drain conduction barrier for a 22 nm effective gate length device when V_G is at 0V and V_D is 50 mV and 1 V.

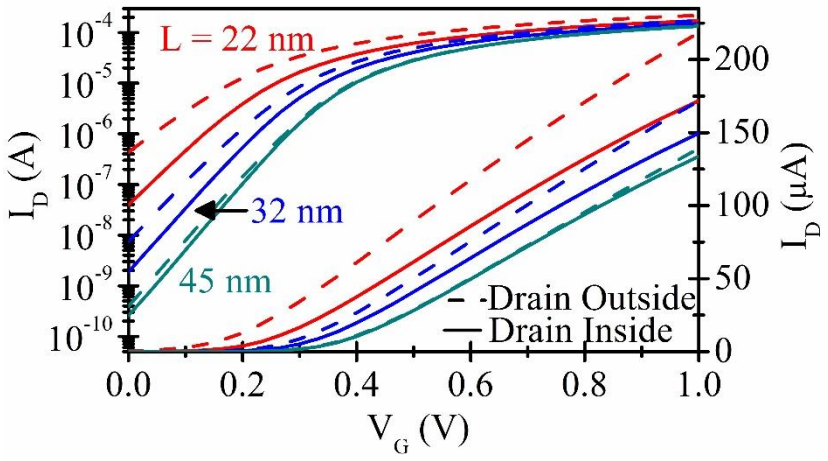

Figure 3.4. Log and linear scale I_D-V_G characterstics for 22, 32, and 45 nm gate length devices with R_i of 10 nm for inside drain (solid lines) and outside drain (dashed lines).

in reduced drain induced barrier lowering (DIBL), threshold voltage (V_t) roll-off and improved subtheshold slope (SS) (Figure 3.4), reduced output conductance (g_d) and lower drive currents (I_{ON}) (Figure 3.5). The contrast between drain inside versus drain outside polarities is more significant for L_{EFF} < 45 nm (Table 3.1).

The I_{ON}/I_{OFF} improves with reduced inner radius for inner drain cases with shorter L_{EFF} (Fig. 6). If a high-k material such as HfO_2 is used as the gate dielectric, the drain

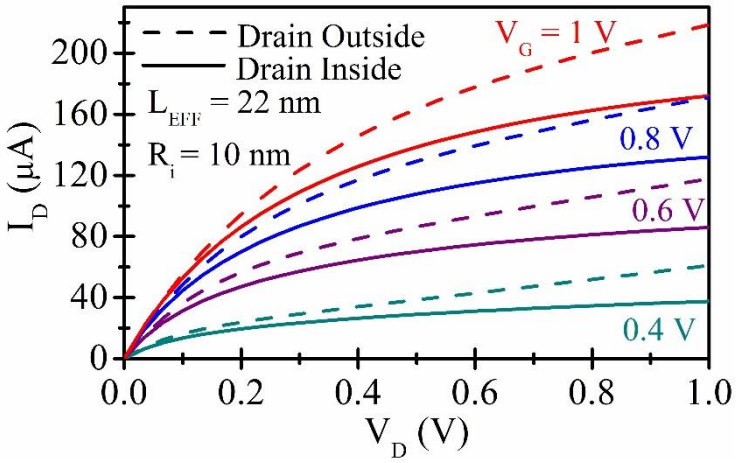

Figure 3.5. I_D-V_D curves for a 22 nm effective gate length device with R_i of 10 nm, inside drain (solid lines) and outside drain (dashed lines).

L_{EFF}	Drain Position	I_{OFF} (nA)	I_{ON} (μA)	I_{ON} (mA/μm)	DIBL (mV/V)	SS (V/dec)	g_d (μA/V)
32 (SiO_2)	Inner	1.89	149.5	0.92	43.6	79.7	30.8
	Outer	7.54	171.7	1.05	94.6	84.5	47.0
22 (SiO_2)	Inner	39.2	172.0	1.30	78	92	39.7
	Outer	432.7	218.4	1.66	179	121	85.4
22 (HfO_2)	Inner	47.1	100.1	0.76	158	121	6.31
	Outer	952.1	114.2	0.86	315	175	32

Table 3.1. Comparison of device characteristics with gate dielectric of 1 nm SiO_2 and 6.4 nm HfO_2 cases for R_i = 10 nm.

field penetration through the dielectric is stronger, leading to aggravated SCE for the same effective oxide thickness. The inner and outer drain contrast is very similar for HfO_2 (Table1), with a bigger improvement in I_{ON}/I_{OFF} for inner drain case (Fig 7).

Scaling the R_i for L_{EFF} < 45 nm decreases the drive current (mA/μm) in both inner and outer drain cases (Figure 3.6a), whereas I_{OFF} and I_{ON}/I_{OFF} improves for the inner drain case (Figure 3.6b). Reducing R_i decreases drive current as the effective width (W_{EFF}), average circumference of channel decreases;

$$W_{EFF} = 2\pi \cdot (R_i + 0.5 \cdot L_{EFF}) \quad (1)$$

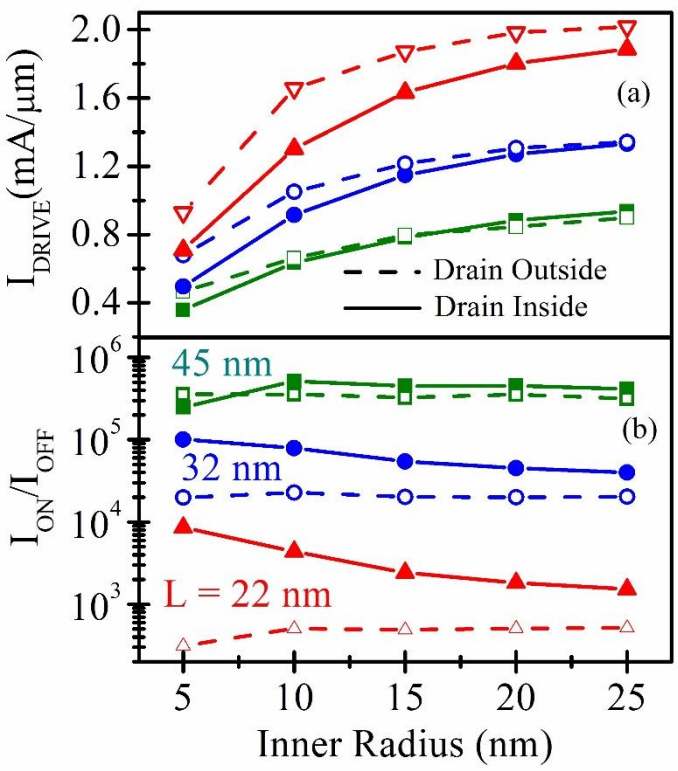

Figure 3.6. (a) Drive current for 22, 32, and 45 gate length devices with drain inner and drain outer orientations as a function Ri. (b) IOFF for 22, 32, and 45 gate length devices with drain inner and drain outer orientations as a function of Ri.

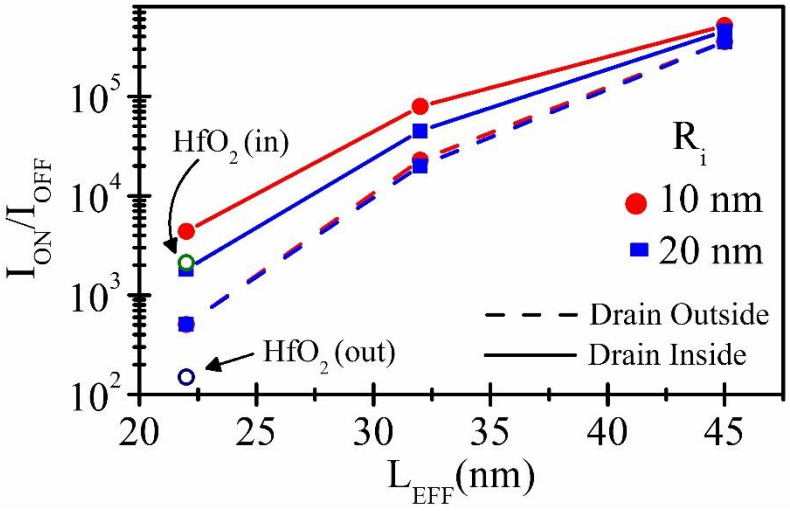

Figure 3.7. On/Off ratio as a function of effective gate length for inner drain (solid) and outer drain (dashed) as a function of R_i. Open circles denote HfO_2 gate dielectric with R_i of 10 nm.

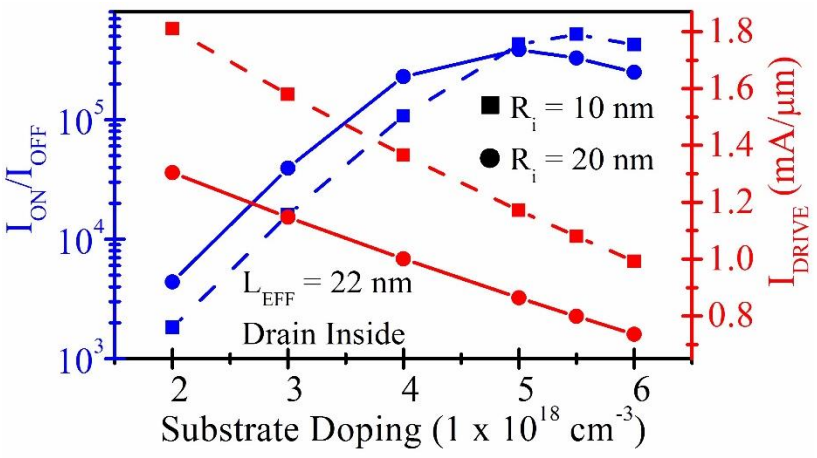

Figure 3.8. I_{ON}/I_{OFF} (blue) and drive current (red) for R_i of 10 nm (square) and 20 nm (circle) as a function of substrate doping.

However, for inner drain devices, the drain area is much smaller than the source area resulting in a further reduction in the drive current due to small field penetration. Similarly, I_{OFF} reduces as R_i decreases for both inner and outer drain cases. Improvement in I_{OFF} and I_{ON}/I_{OFF} is a result of the increased control over SCE for inner drain cases when L_{EFF} is decreased below 45 nm (Figure 3.7). For 22 nm RingFETs, $I_{ON}/I_{OFF} > 1 \times 10^4$ can be achieved by increasing substrate doping (Figure 3.8) up to 5×10^{18} cm^{-3}. The inner drain devices show improved gate length scaling behavior, and also reduced DIBL and SS for decreasing Ri. For $L_{EFF} \geq 45$ nm, all four cases (inner or outer drain with 10 or 20 nm inner radius) result in approximately the same SS and DIBL (Figure 3.9). RingFET geometry consumes a comparable area as conventional planar devices for the same drive current but its packing density is worse than the smallest feature size conventional planar devices unless a common source configuration is used.

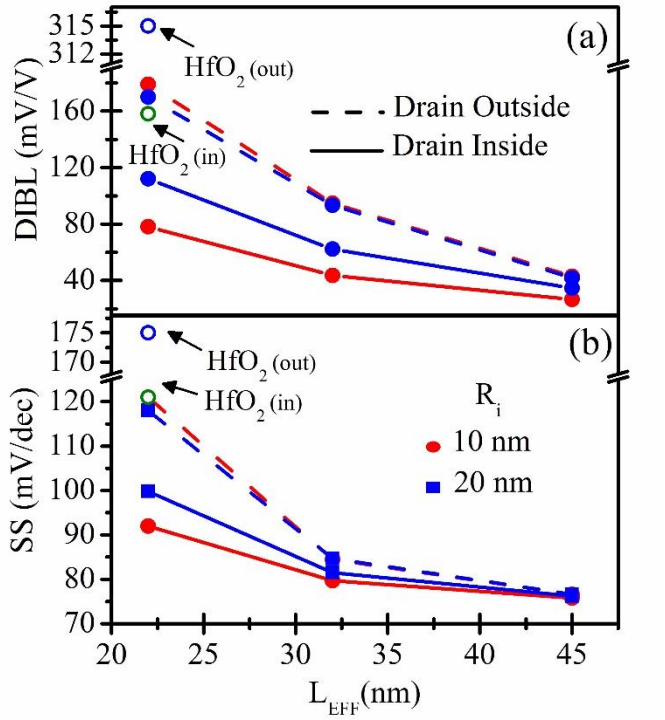

Figure 3.9. DIBL (a) and SS (b) for as a function of effective gate length for inside radius of 10 and 20 nm, inside drain (solid), and outside drain (dashed). Open circles denote HfO_2 gate dielectric with R_i of 10 nm.

4 TEG Scaling

We have analyzed the scaling effects on TEGs using finite element simulations in Synopsys Sentaurus software. TEGs composed of silicon and silicon germanium were created in 2D planar, 2D rotational and 3D (in the case of silicon germanium) geometries with temperature dependent material parameters where power density and efficiency were calculated. A modified drift-diffusion equation (thermodynamic) for heat transfer and current continuity was utilized to evaluate the impact of scaling on TEG performance.

4.1 Finite Element Analysis of Scaling of Silicon Micro-Thermoelectric Generators to Nanowire Dimensions

4.1.1 Introduction

Realization of greater efficiency and higher performance requires analysis of scaling of TEGs to understand how the device dimensions and operating temperature affect device performance. In this study, 2D finite element simulations using Synopsys Sentaurus TCAD are conducted to examine the effects of changes in the height, width, and temperature on the performance of TEGs. [70]In comparison to other finite element method based software such as COMSOL Multiphysics and ANSYS Multiphysics, Sentaurus is packaged with a multitude of semiconductor physics models and material parameters for common semiconductors like silicon which allows for robust and detailed investigation of device operation but does not allow as much flexibility.

Previously published works simulating the performance of TEGs often do not include temperature dependent material parameters[71-75] which can result in inaccurate evaluation of device performance across a wide temperature range and they do not consider

scaling into the sub-μm scale (Table 4.1). Sentaurus TCAD has previously been used to investigate the performance of a single crystal silicon (c-Si) TEG with varying doping concentrations and temperature differences[76]. 3D simulations of mm scale silicon TEGs (Figure 4.1a) have been reported by Gould *et al* where a resistive load was varied from open to short circuit to calculate the maximum power. Simulations showed that increasing the doping concentration resulted in an increase in the peak power.

Reference	3D/2D	Leg Material	Temp. Dependent Parameters	Scaling/Variables	Min /Max Dimension	Temp Range (K)	Simulation Tool
Gould[76]	3D	c-Si (10^{14} to 10^{16} cm^{-3} doped)	Yes	Doping Concentration, ΔT	800 μm/6.75 mm	300 - 400	Sentaurus
Egbert[77]	3D	c-Si ($5x10^{19}$ cm^{-3} doped)	No	Leg Width, and Height, Number of TEGs	5 μm/2 mm	295 - 305	COMSOL
Jang[71]	3D	Bi_2Te_3/ Sb_2Te_3	No	Leg Height and Area, Substrate Thickness	5 μm/500 μm	285 - 300	N/A
This Work	2D	c-Si (10^{19} cm^{-3} doped)	Yes	Leg Height and Width, ΔT	100 nm/1 mm	300 - 1650	Sentaurus

Table 4.1 Comparison of previously reported TEG simulations.

Egbert *et al.*[77] simulated 3-D silicon on insulator based μ-TEGs in COMSOL Multiphysics, (Figure 4.1b) where multiple TEGs were constructed in plane and connected in series around a square ring. The silicon legs have a width (W_{LEG}) that was varied from 5 to 200 μm, leg height (H_{LEG}) of 500 μm, 1 mm, and 2 mm with a temperature difference that varied from 0 to 10 K.

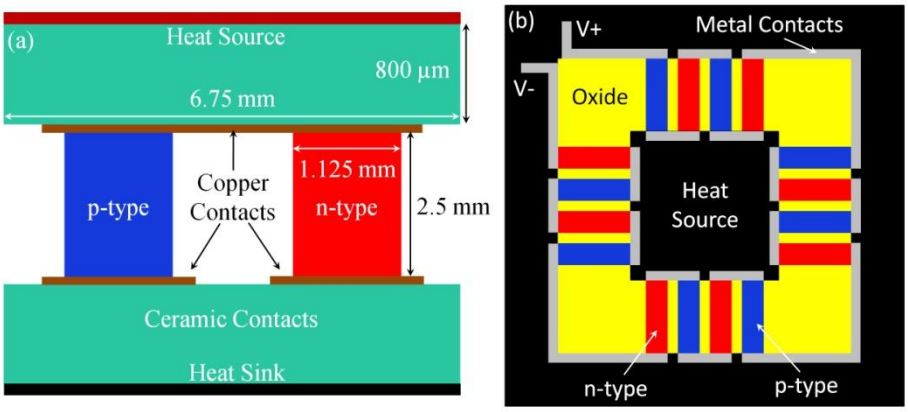

Figure 4.1 (a) 2D cross section diagram of TEG simulated by Gould et al. (b) Top down 2D image of TEG module simulated by Egbert et al.

The simulation results showed that the open circuit voltage (V_{OC}) increased but the maximum power decreased as the width decreased. As the width decreased, the number of TEG's in the square rings increased resulting in a larger V_{OC} but at the cost of increased series resistance which decreased current drive and generated power. The power increased as overall module area increased to allow for more TEG elements with shorter heights.

Jang *et al.*[71] used 3-D finite element simulations to optimize the design of µ-TEGs by scaling the H_{LEG}, leg cross-section area, and the thickness of the thermal contacts. The µ-TEGs had n-type Bi_2Te_3 and p-type Sb_2Te_3 legs with silicon thermal contacts and copper electrical contacts. A temperature difference of 15 K was placed across the device while the generated power and TEG efficiency was calculated.

Simulations showed that a H_{LEG} of 10 µm produced a maximum power due to optimum temperature difference and resistance.

As the thermal contact thickness increased, the power and efficiency decreased due to an increase in the thermal losses to the substrate. The efficiency of the TEG increased as H_{LEG} increased due to a large decrease in the heat flux. When the cross-sectional area of

the TEG legs is scaled from 25 μm^2 to 2.5 mm^2 the power increased due to decreased resistance while the efficiency decreased due to increased heat flux.

A systematic approach to scaling and inclusion of temperature dependent material parameters is needed to understand how TEGs operate over a large range of sizes from mm to sub-micron and over a large range of temperatures. In this study, temperature dependent material parameters (electrical resistivity (ρ), thermal conductivity (κ), Seebeck coefficient (S), and heat capacity (C_P)) are included for accurate calculations of device performance across a large temperature range (300 to 1650 K) and dimensions range (W_{LEG} from 0.5 to 5000 µm and H_{LEG} from 0.5 to 1000 µm). 2D planar (Figure 4.2b) and 2D axial symmetric (Figure 4.2c-e) simulations are performed. Axial symmetric simulations are expected to be more accurate since they capture the heat transfer throughout the 3D geometry and are used to examine differences between 2D planar and 3D models.

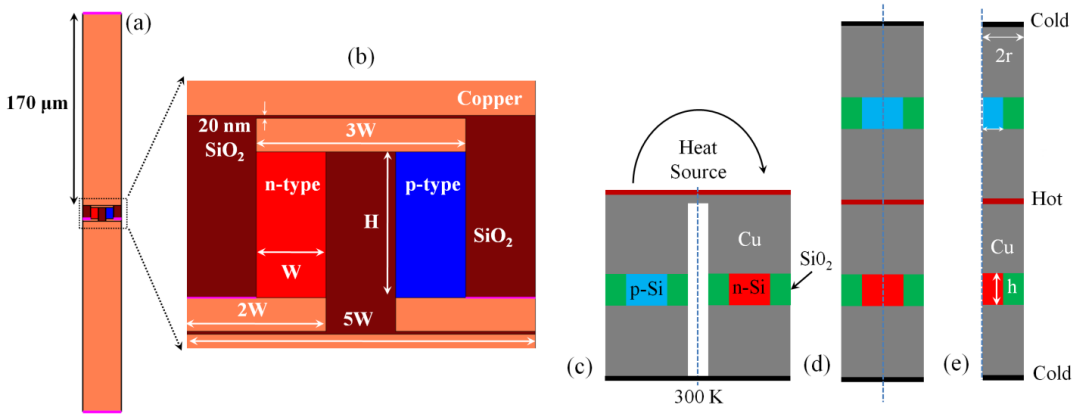

Figure 4.2 (a) Diagram of the simulated TEG device including the 170 µm tall top and bottom metal contacts, and (b) enlarged image from dashed region in 1(a) showing details of the TEG semiconductor legs, SiO2, and metal contacts. (c) Cross section of cylindrical

4.1.2 Simulated TEG Geometries

The 2D planar geometry (Figure 4.2a) is composed of a single TEG that is wedged between two, 170 μm tall copper thermal contacts. A thickness of 170 um was chosen as it is the thinnest available sheet metal. An enlarged view (Figure 4.2b) of the dashed region in Figure 4.2a shows the TEG which consists of one n-type ([As] = 10^{19} cm^{-3}) leg and one p-type ([B] = 10^{19} cm^{-3} leg representative of a single pair in an array that would form a TEG module. This doping level is approximate optimum in terms of the ZT of the material. The legs share a top copper electrical contact and have individual bottom metal electrical contact. The TEG is electrically isolated from the top and bottom thermal contacts by a 20 nm thick layer of SiO_2. The p and n legs are surrounded with silicon dioxide (SiO_2) providing a thermal shunt from the top to bottom of the device. When the width of TEG leg is scaled (W = 0.5 to 5000 μm, H = 0.5 to 1000 μm), the device dimensions are scaled by W (Figure 4.2b) to accommodate the change in leg width.

Simulations of 3D TEGs offer the best estimation of device performance as the heat diffusion is more accurately modeled but require significantly longer computational time. 3D models can be approximated using 2D axial symmetric simulations. Figure 4.2c shows a cross section of a cylindrical 3D TEG which consists of n and p-type silicon rods which share a top metal contact with top and bottom thermal contacts. The 3D model can be approximated by bisecting the 3D model on the dashed line shown, where one half of the device is flipped and stacked on top of the other half (Figure 4.2d) resulting in a 2D axial symmetric model (Figure 4.2e).

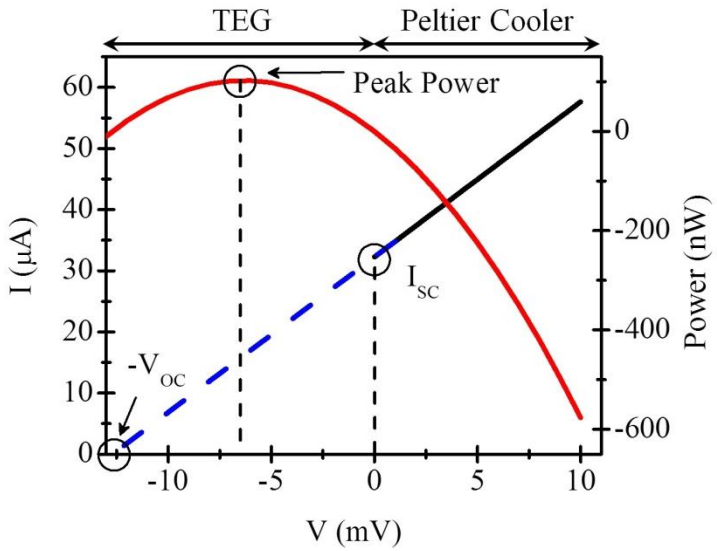

Figure 4.3 I-V data from simulation of TEG. Black line is the simulated data and the blue dashed line is the extrapolated data. Red line is the power generated (in TEG operation) and power supplied (Peltier cooling mode).

4.1.3 Models and Parameters

For the 2D planar TEG, a heat source with a T = 300 - 1650 K is applied to the top thermal contact (T_{TOP}) while the bottom thermal contact is at 300 K. A DC sweep from 0 to 10 mV is applied to the n-leg while the p-leg contact is kept at 0 V. In the 2D axial symmetric TEG, a heat source, T = 300 - 1650 K, is placed in the middle of the device while the top and bottom metal contacts are at 300 K. A DC sweep is applied to the top metal contact while the bottom metal contact is at 0 V. The voltage range is small to avoid any significant Joule heating in the device which would disturb the temperature difference. The I-V data (Figure 4.3) is extrapolated and the open circuit voltage (V_{OC}), short circuit current (I_{SC}), resistance, and peak power are extracted.

Lattice temperature and charge carrier transport are solved using the Sentaurus thermodynamic model[78] which expands the drift diffusion current density equation to include the thermoelectric contribution:

$$\overrightarrow{J_n} = -nq\mu_n(\nabla\Phi_n + S_n\nabla T),\ \overrightarrow{J_p} = -pq\mu_p\left(\nabla\Phi_p + S_p\nabla T\right)$$

where Φ is electron or hole quasi-Fermi potential, J is current density, μ is carrier mobility, S is absolute electron or hole thermoelectric power (Seebeck coefficient), n is electron density, p is hole density and ∇T is the temperature gradient. The approximate analytic expressions for the electron and hole Seebeck coefficient, S_n and S_p are used, which are valid for non-degenerate semiconductors with doping concentrations up to 1 x 10^{19} cm^{-3}[79]:

$$S_n = -\frac{k}{q}\left[\frac{3}{2} + ln\left(\frac{N_C}{n}\right)\right],\ S_p = +\frac{k}{q}\left[\frac{3}{2} + ln\left(\frac{N_V}{p}\right)\right]$$

where k is the Boltzmann constant, q is electron charge, N_C and N_V are effective densities of states for the conduction and valence bands. The default scattering coefficient of -1 and scaling coefficient of 1 are used here. These expressions accurately reflect the initial increase of absolute Seebeck coefficient with T and decrease with 1/T at higher temperatures.

The electrical and heat transport is modeled using the current continuity and the Fourier heat diffusion equations with Joule and thermoelectric heat contributions:

$$\nabla\cdot J_n = q\frac{\partial n}{\partial t},\ -\nabla\cdot J_p = q\frac{\partial p}{\partial t}$$

$$C_P\frac{\partial}{\partial t}T - \nabla\cdot\kappa\nabla T = -\nabla\cdot\left[(S_nT + \Phi_n)J_n + \left(S_pT + \Phi_p\right)J_p\right]$$

$$-\left(E_C + \frac{3}{2}kT\right)\nabla\cdot J_n - \left(E_V - \frac{3}{2}kT\right)\nabla\cdot J_p$$

where C_P is lattice heat capacity, and κ is thermal conductivity. Recombination and Peltier heating/cooling at the silicon/metal contact junction are considered negligible and

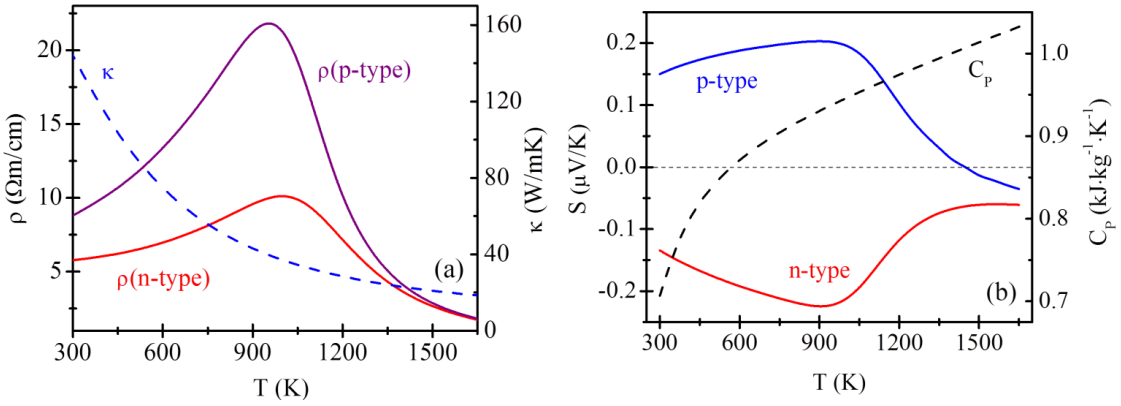

Figure 4.4 (a) Temperature dependent thermal conductivity (κ), and electrical conductivity (σ) for n-type [As] and p-type [B] 1 x 1019 cm-3 doped single crystal silicon. (b) Seebeck coefficient(s) for same doping n-type and p-type single crystal silicon and heat capacity (C_P).

are not included in the heat diffusion model. In the simulations, the c-Si legs have temperature dependent material parameters which are used from the Sentaurus material library (Figure 4.4). The maximum simulation temperature is limited to 1650 K to avoid the solid-liquid phase transition in silicon.

4.1.4 Simulation Results

Power density (PD) decreases with increasing W_{LEG} especially for smaller heights (Figure 4.5a). This trend is a result of significant drop in the temperature difference across short legs as W_{LEG} is scaled (Figure 4.5b). The thermal resistance of small aspect ratio legs (large widths and small height) is considerably smaller than high aspect ratio legs (small widths and large heights) and the resultant temperature difference is appreciably smaller.

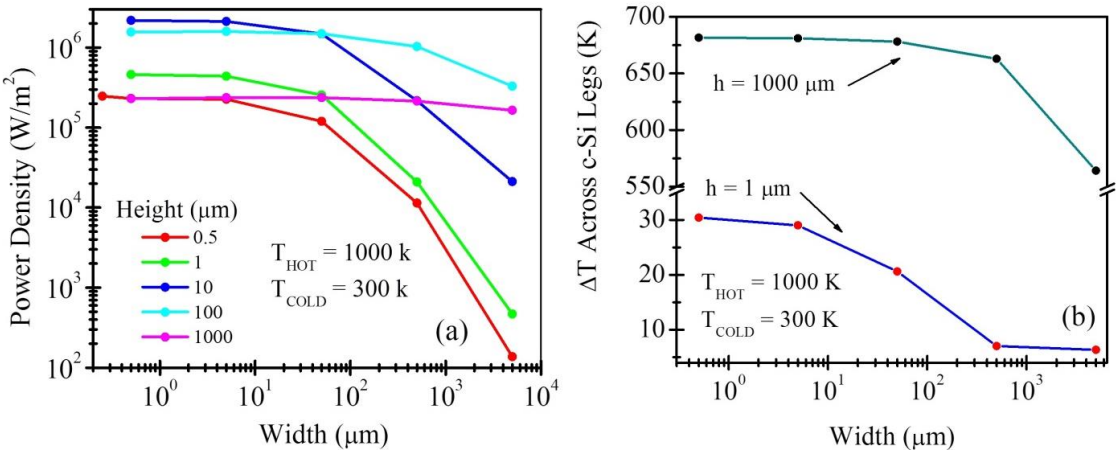

Figure 4.5 (a). Power density as a function of the width of the silicon leg for a T_{TOP} of 1000 K. Each line represents a single leg height indicated in the legend (units in μm). (b) Temperature gradient across the height of the silicon legs as a function of the width. The blue line is for a height of 1 μm and the green line is for a height of 1000 μm.

There is an optimum H_{LEG} corresponding to a peak power density (Figure 4.6a) which is due to a maximum in the product of voltage and current density (Figure 4.6b-c). As H_{LEG} increases, the current density decreases due to increased resistance while voltage increases as a result of a larger temperature difference across the legs (Figure 4.6d). When H_{LEG} is small, current density increases as leg resistance drops but the voltage sharply decreases. As the T_{TOP} increases, the optimum leg height (Figure 4.7a) decreases exponentially saturating at ~ 9 μm for T_{TOP} of 1550 K (Figure 4.7b). This trend is similarly

found for all W_{LEG} (Figure 4.7c). An increase in the optimum leg height for temperatures greater than ~1500 K is visible for widths of 500 and 5000 µm.

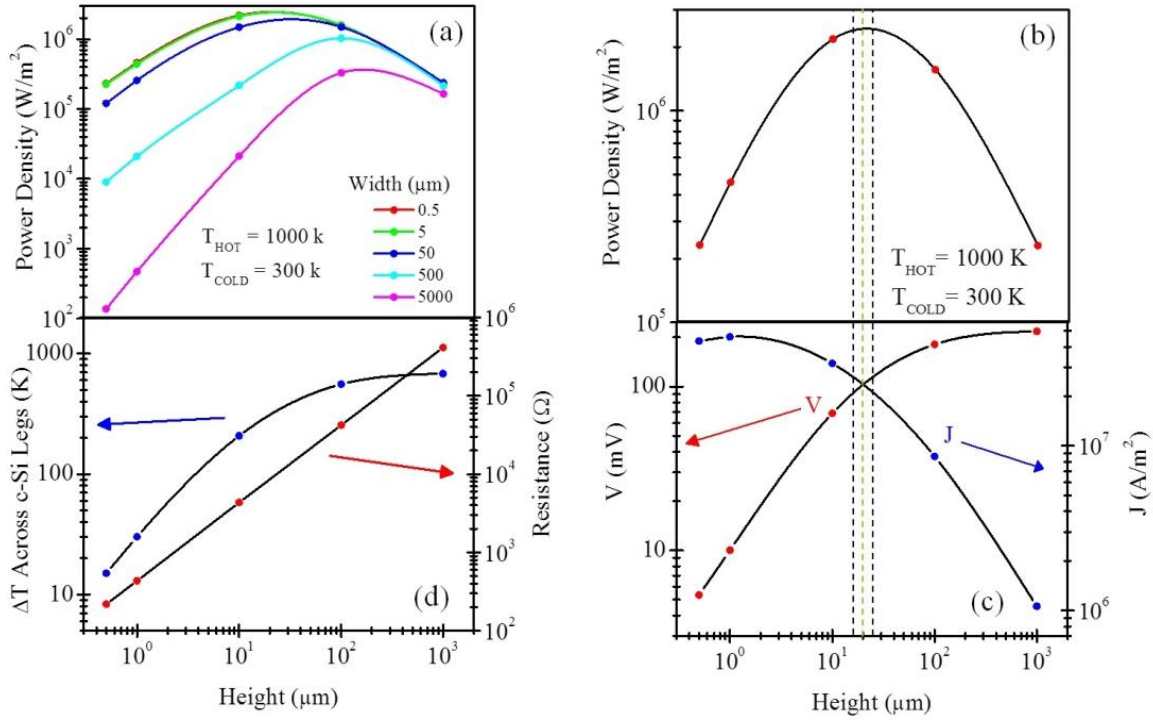

Figure 4.6 (a) Power density as a function of the height of the silicon leg for a T_{TOP} of 1000 K. Each line represents a single leg width indicated in the legend (units in µm). (b) Power density as a function of the leg height for a width of 0.5 µm with a T_{TOP} of 1000 K. (c) Voltage and current density that correspond to the power density in (b). Dashed lines indicate the region where maximum power density occurs. (d) Resistance of entire TEG device and the temperature gradient across the height of the silicon legs.

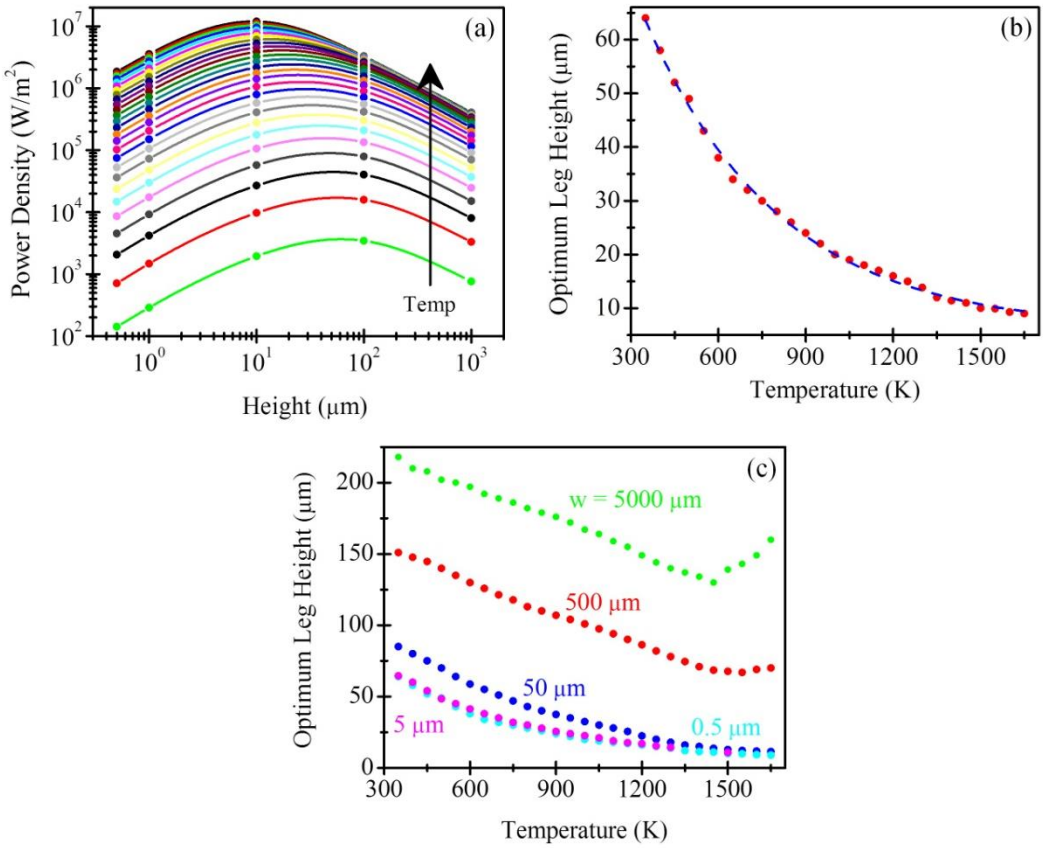

Figure 4.7 (a) Optimum leg height plotted as a function of the height for T_{TOP} ranging from 350 to 1650 K. Black arrow indicates direction of increasing temperature. Leg width is 0.5 μm. (b). Optimum leg height plotted as a function of the T_{TOP}. Leg width is 0.5 μm. (c) Optimum leg height plotted as a function of the T_{TOP} for various, simulated widths.

The efficiency of the TEG increases as the temperature increases (Figure 4.8a) and with H_{LEG} (Figure 4.8b), saturating at larger heights. Efficiency improves as temperature increases due to decreased heat flux as Silicon thermal conductivity decreases at elevated temperatures. The efficiency saturates as the power density reduces where Seebeck coefficient decreases significantly at very high temperatures.

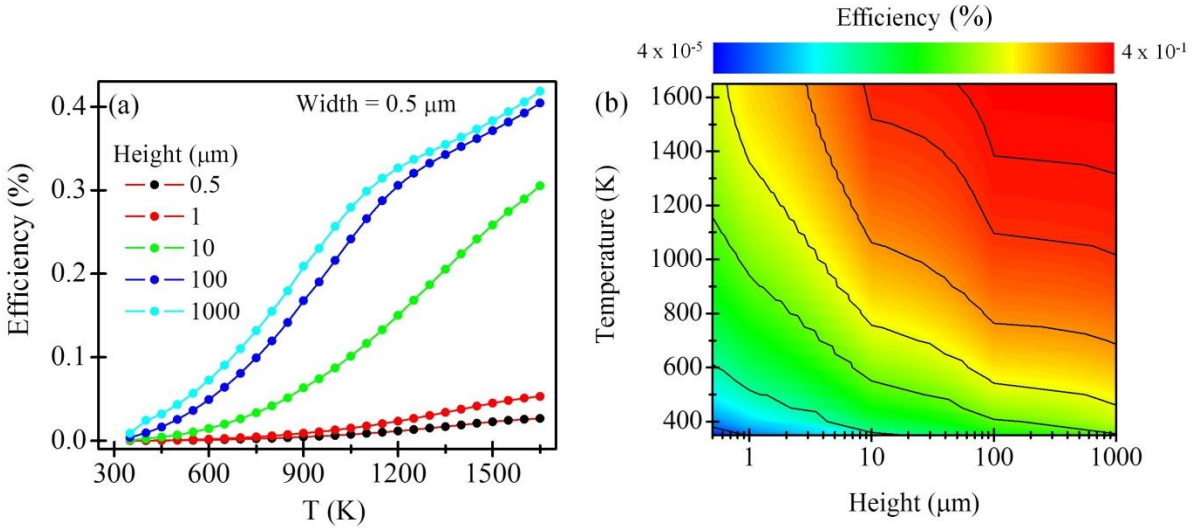

Figure 4.8 (a) Efficiency of the Si TEG plotted as a function of T_{TOP} for all possible heights. Leg width is 0.5 μm. (b) Efficiency contour map as a function of temperature and height.

TEGs with higher aspect ratios (H_{Leg}/W_{Leg}) show significantly larger power density (Figure 4.9a). For narrow widths, maximum power density is obtained with large aspect ratios (H_{Leg}/W_{Leg} ~ 100-1,000) while for wider legs it is obtained for smaller aspect ratios (H_{Leg}/W_{Leg} ~ 1-100). 2D axial symmetric TEGs with a width of 500 nm show reasonable agreement with 2D planar TEGs with a width of 500 nm. The peak in power density is achieved for a smaller aspect ratio for the 2D axial symmetric simulations while power density is slightly higher at the peak.

Cylindrical nanowire power generation is expected to be underestimated since simulated models assume bulk c-Si material properties while it has been reported that Si NWs have lower thermal conductivities[80, 81]. For both the axial symmetric and planar models, increasing the aspect ratio results in increased efficiency (Figure 4.9b) where all possible TEG widths saturate at the largest simulated aspect ratios with 0.25 % efficiency.

These results suggest that Si nanowires with widths on the order of 100 nm and aspect ratios of >~100 would give optimum power generation.

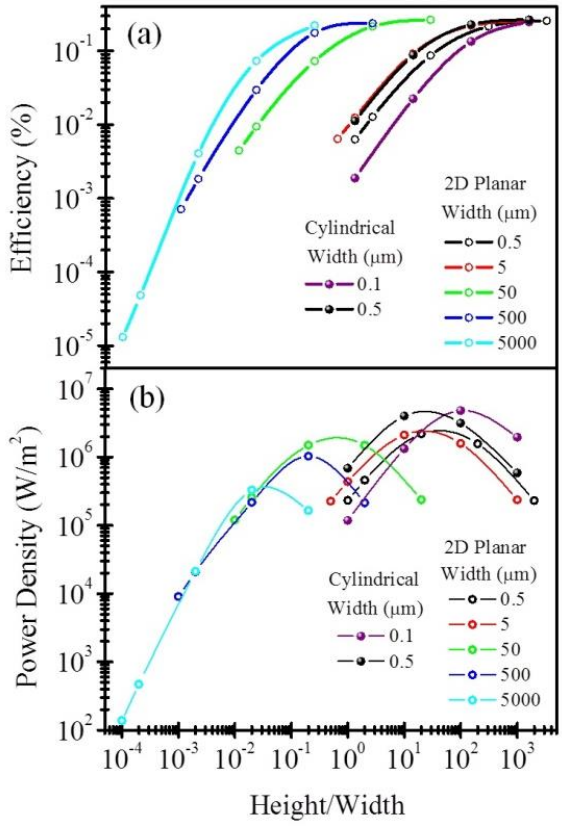

Figure 4.9 (a) Power density of TEG plotted as a function of aspect ratio for a T_{TOP} of 1000 K. (b) Efficiency of TEG plotted as a function of aspect ratio for a T_{TOP} of 1000 K. Widths are indicated in μm.

4.2 Finite Element Simulations on Scaling Effects of 3D Silicon Germanium Thermoelectric Generators

4.2.1 Introduction

3D finite element simulations in Synopsys Sentaurus TCAD are used to investigate the effect of scaling the device dimensions and changing the operating temperature on the performance of a single TEG composed of Silicon Germanium (Si_xGe_{1-x}). The TEG leg height (H_{LEG}) ranges from 100 nm to 10 µm while the width and depth range from 100 nm to 10 mm. Si_xGe_{1-x} is a commonly used high temperature thermoelectric material with a peak ZT value of ~ 1 for n-type and ~ 0.6 for p-type at 900° C[33]. ZT values of 1 are achieved as a result of a considerable decrease in thermal conductivity for SiGe as compared to pure Si or Ge.

4.2.2 Geometry

A complete 3D model (Figure 4.10a) of a TEG is used in this simulation for accurate estimation of device performance as the heat diffusion is more accurately modeled as compared to 2D simulations. The simulated geometry (Figure 4.10a-b) is composed of n-type ([A] = 10^{19} cm^{-3}) and p-type ([B] = 10^{19} cm^{-3} legs wedged between two 170 µm tall copper metal contacts used for heat transfer. The p-type and n-type SiGe legs are connected with a top electrical copper contact where each leg has a separate electrical contact. The legs and electrical contacts are completely enclosed in oxide to account for thermal shunting and to electrically isolate the legs and electrical contacts from the thermal contacts. The width, depth, and height of the TEG legs were scaled according to Figure 4.10c-d where the surrounding oxide, electrical contacts, and thermal contacts are stretched

as the legs are scaled to maintain equal relative sizing. The width and depth were scaled equally resulting in scaling the cross sectional area of the leg.

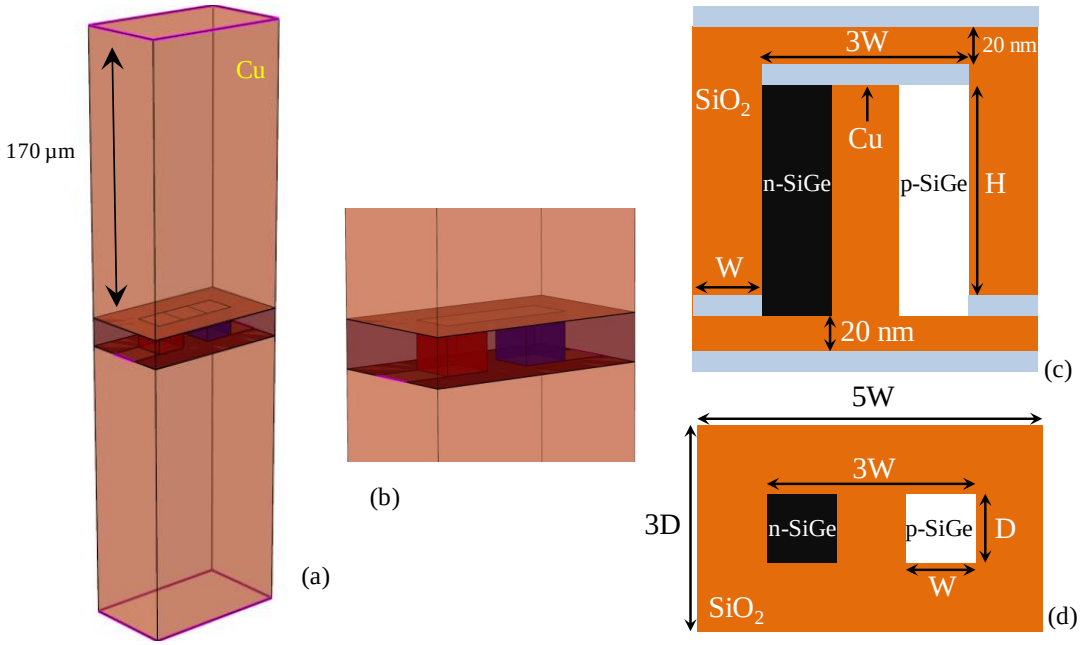

Figure 4.10 (a). Perspective view of 3D TEG model with transparency to show TEG legs inside oxide. (b) Zoomed in view of 3D model showing detail of TEG legs. (c) Cross section of surrounding oxide, electrical contacts and TEG legs showing the scaling parameters. (d) Top down cross section of surrounding oxide and TEG legs with scaling parameters. Metal contacts are excluded from this image.

In the simulations, a heat source with temperature from 300 to 1450 K is placed on the top thermal contact (T_{TOP}) while the bottom thermal contact is kept at 300 K. The voltage on the n-type leg electrical contact is swept from 0 to 10 mV while the p-type leg electrical contact is kept at 0 V. The applied DC bias is low voltage to avoid any Joule heating. The extracted IV characteristics (Figure 4.11) are used to calculate open circuit voltage (V_{OC}), short circuit current (I_{SC}), resistance, and peak power.

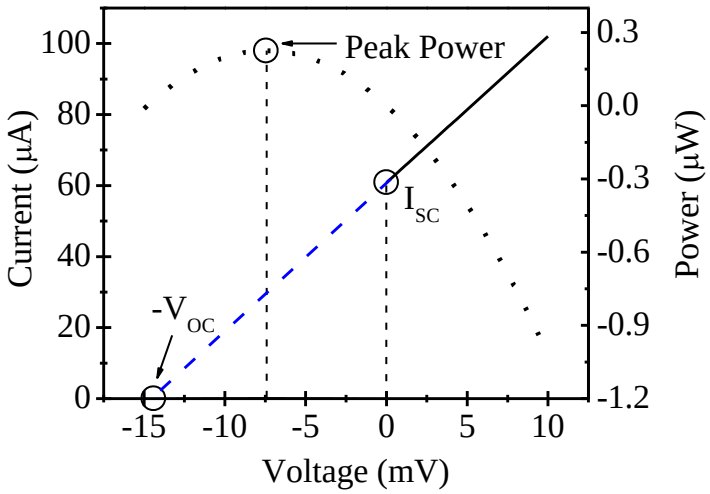

Figure 4.11 I-V data from simulation of TEG. Solid line is the simulated data and the dashed line is the extrapolated data. Dotted line is the power generated (in TEG operation) and power supplied (Peltier cooling mode).

4.2.3 Models and Parameters

This work utilizes the same semiconductor model as described in section 2.2.4. In these simulations, temperature dependent materials parameters for electrical resistivity (Figure 4.12a) and Seebeck coefficient (Figure 4.12b) of SiGe are used. Thermal conductivity of SiGe is assumed to be a constant value of ~7 W/mK. Maximum simulation

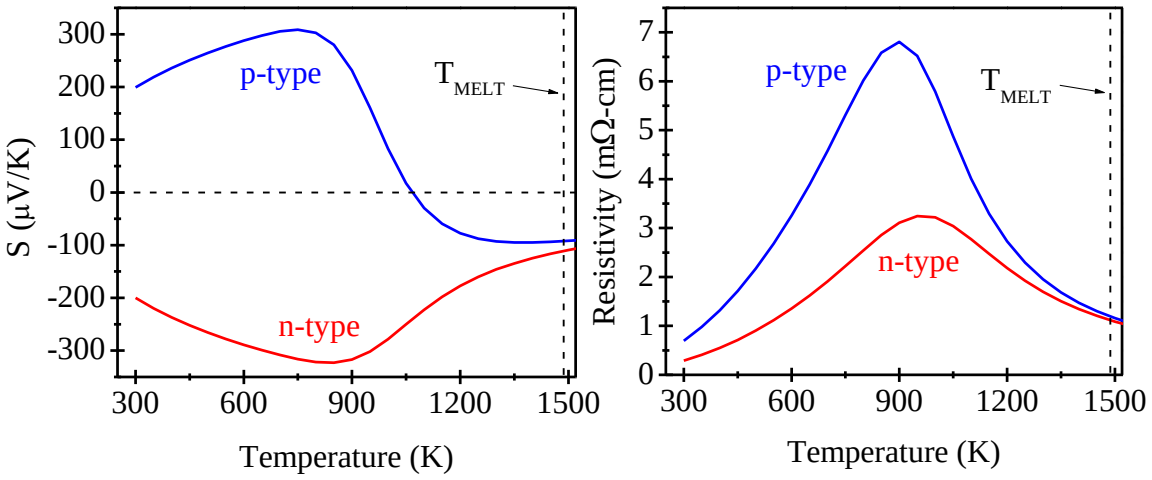

Figure 4.12 (a) Temperature dependent electrical resistivity (ρ) for n-type and p-type 1 x 10^{19} cm^{-3} doped SiGe. (b) Seebeck coefficient(s) for n-type and p-SiGe

temperature is limited to 1450 K to be below the melting temperature of $Si_{0.7}Ge_{0.3}$ (~1487 K). The material parameters for copper and SiO_2 are assumed to be constant.

4.2.4 Simulation Results

For smaller heights, power density (PD) decreases with increasing cross sectional area (Figure 4.13a). As the cross sectional area of the TEG legs increases, the heat flux increases which strongly affects TEG legs with small aspect ratios. The increase in heat flux reduces the temperature difference across the TEG legs due to an increase in thermal losses in the isolation oxide. A decrease in the temperature difference decreases the output voltage and consequently the PD.

When scaling height, an optimum H_{LEG}, corresponding to a peak PD (Figure 4.13b), is observed which is due to a maximum in the product of voltage and current density. When the H_{LEG} is increased above the optimum, the electrical resistance of the legs becomes significant, limiting the current drive. As the H_{LEG} is scaled down below the optimum, the heat flux increases which reduces the temperature difference across the legs.

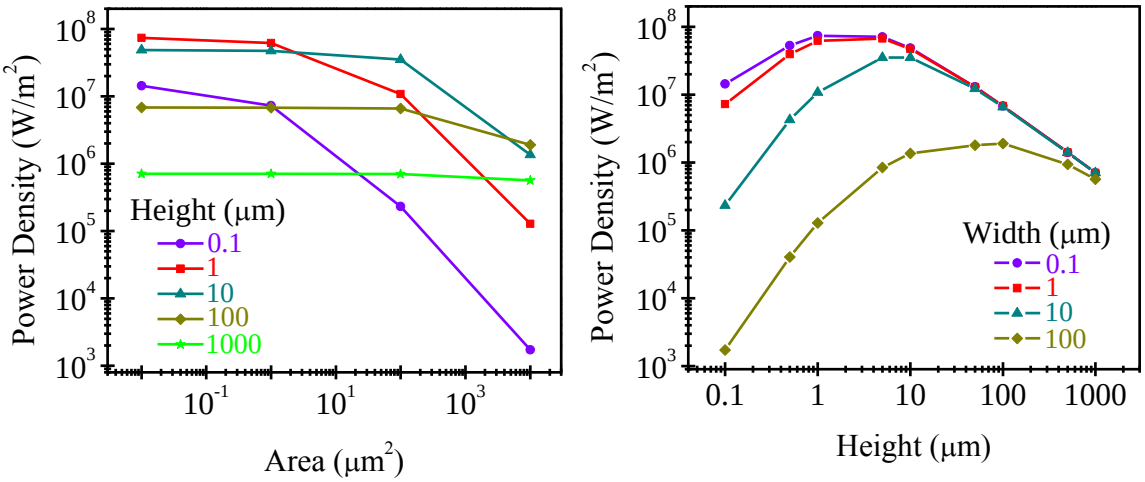

Figure 4.13 (a) Power density as a function of the cross sectional area of the SiGe leg for a T_{TOP} of 1000 K. (b) Power density as a function of the cross sectional area of the SiGe leg for a T_{TOP} of 1000 K.

PD is significantly larger for TEGs with higher aspect ratios (tall and narrow legs) on the order of ~10 – 100x larger as compared to TEGs with small aspect ratios (short and wide legs) (Figure 4.14). The simulation results suggest that nanowires with widths under 100 nm and aspect ratios from 10-100 could give optimum TEG performance. Further improvements in performance could be possible for nanowire TEGs as the models used

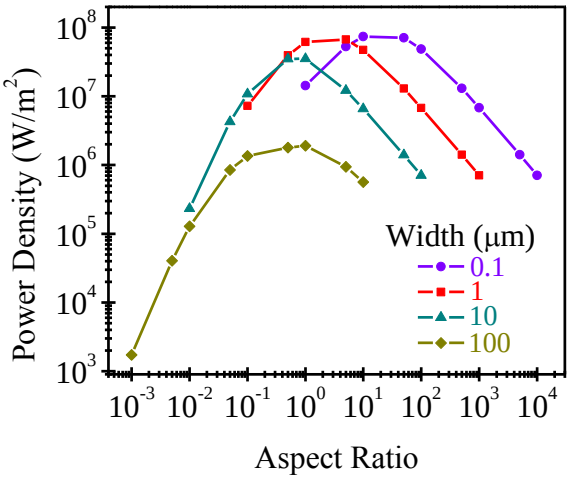

Figure 4.14 Power density as a function of TEG leg aspect ratio for a T_{TOP} of 1000 K.

in this simulation assume bulk SiGe material properties and nanowires have been observed to have decreased thermal conductivity, hence larger ZT.

Results suggest that 2D rotational symmetric simulations are a reasonable approximation for 3D simulations. 3D results show similar trend in PD vs. aspect ratio compared to 2D rotational symmetric results for Silicon TEGs where the maximum PD occurs for aspect ratios of ~10-100 (leg widths of 100 nm). PD and efficiency are larger for the SiGe TEGs due to the reduced thermal conductivity and larger ZT of Silicon Germanium compared to Silicon. A quantitative comparison would require 2D and 3D simulations of the same geometry and materials μTEGs. However, as the surface to volume

ratio increases, 3D simulations are expected to be required to properly capture the correct electronic and thermal transport.

5 TEG Efficiency Enhancement via Minority Carrier Extraction

5.1 Introduction

At elevated temperatures, minority carrier generation/recombination limits the performance of TEGs by reducing the Seebeck coefficient of the material. Reducing minority carrier generation and recombination would significantly improve TEG efficiency by increasing output power. We examine the role of minority carriers on the efficiency of μTEGs and demonstrate a μTEG design that can extract generated minority carriers using built in electric fields, utilizing them to enhance performance. These modified μTEG designs are compared to conventional TEG geometries for a variety of TEG leg dimensions (from 1 μm to 5 nm) analyzing the effects of scaling on minority carrier extraction.

5.2 Models and Parameters

For these simulations we have used a similar model as described in section 4.1.3 but with additional components. We have used the expanded recombination model that includes additional recombination mechanisms and added temperature dependent electron and hole masses. Appendix Chapter 7.3 discusses in greater detail the individual components of each part of the model used, as described the Sentaurus manual [67].

5.2.1 Mixed Mode

Previous TEG simulations (Chapter 4.1, 4.2) calculated the output power using a low voltage DC sweep applied across the TEG legs which was linearly extrapolated to calculate short circuit current, open circuit voltage, and maximum power. Upon further examination, it was found that a linear extrapolation of the IV data results in inaccurate calculations of TEG performance due to non-linear operation at high temperatures. A more

realistic method of calculating TEG performance requires sweeping a resistive load attached to the TEG legs and extracting the maximum power dissipated in the load. For these sets of simulations the previous power calculation method was replaced with a resistive load sweep from 0.1 to R_{MAX} using Sentaurus Mixed Mode (Figure 5.1a). R_{MAX} is adjusted so that a maximum power point is observed for all geometries and all T_{TOP}

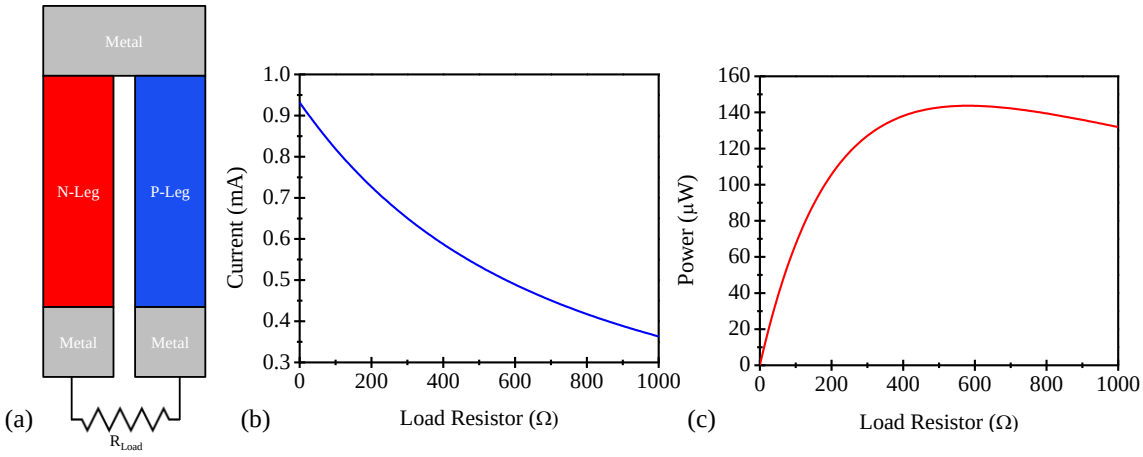

Figure 5.1 (a) Diagram of Mixed Mode simulation (b) Example of output current (b) and power (c).

(Figure 5.1b-c). Sentaurus Mixed Mode operation allows for spice circuits to be connected to electrical and thermal contacts and simulated in SDevice. An example of output current and power of ~140 μW is shown in Figure 5.1.

5.3 μTEG Geometry

Two different geometries will be utilized in these simulations; a conventional TEG (Figure 5.2a) (used as a baseline device) and what we call a ladder TEG (Figure 5.2) which has several intrinsic SiGe regions that bridge the n-type and p-type legs. The number of intrinsic regions vary depending upon the intrinsic region dimensions and leg height. For both geometries a thermal contact is defined along the top edge of the top copper contact while thermal contacts are placed along the bottom edge of both bottom metal contacts.

The top thermal contact temperature (T_{TOP}) is varied from 300 K to T_{Melt} (~1500 K for SiGe with x = 0.3) while the bottom thermal contacts are held at 300 K for all simulations. All other boundaries are assumed to be thermally insulating. Unlike previous simulations (Chapter 4.1, 4.2) there are no isolating oxide or heat transfer contacts. They

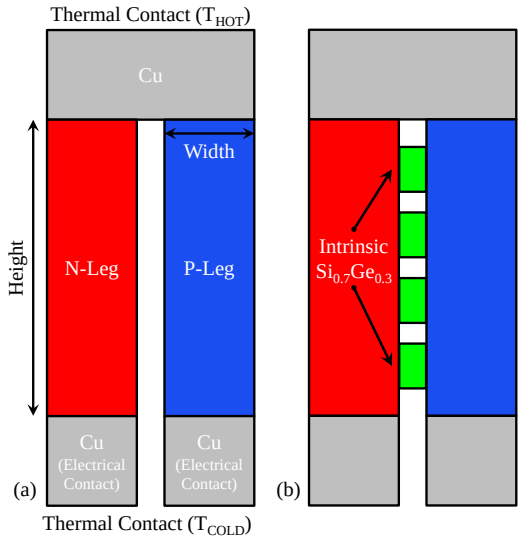

Figure 5.2 Diagram of conventional (a) and ladder (b) μTEGs.

were excluded to simplify simulations and reduce computational time but can be approximated by adding in an external thermal resistance to all of the thermal contacts. The bottom edge of each bottom metal contact are also electrical contacts (ideal Ohmic) which are connected to the external SPICE circuit.

5.4 Minority Carrier Transport

The addition of the intrinsic regions in the ladder TEG results in multiple PIN junctions forming from p to n legs. PIN junctions are commonly used in photovoltaic cells as it improves the quantum efficiency by improved electron-hole pair generation. A band diagram (at 300 K) for a generic PIN junction is shown in Figure 5.3a assuming a doping concentration of 1 x 10^{19} cm^{-3} for both p and n type sections. The ladder TEGs are designed with several PIN junctions to extract generated minority carriers and transport them to their

corresponding majority carrier leg (Figure 5.3b) using the built-in electric field formed by the PIN junction (generated hole in the n-type leg is transported to the p-type leg). The transported minority carrier will no longer recombine with a majority carrier but instead will contribute to the current density of its corresponding majority leg. Majority carriers are not expected to be transported by intrinsic regions due to the strong reverse electric field which would require considerable kinetic energy to overcome. The ability of the

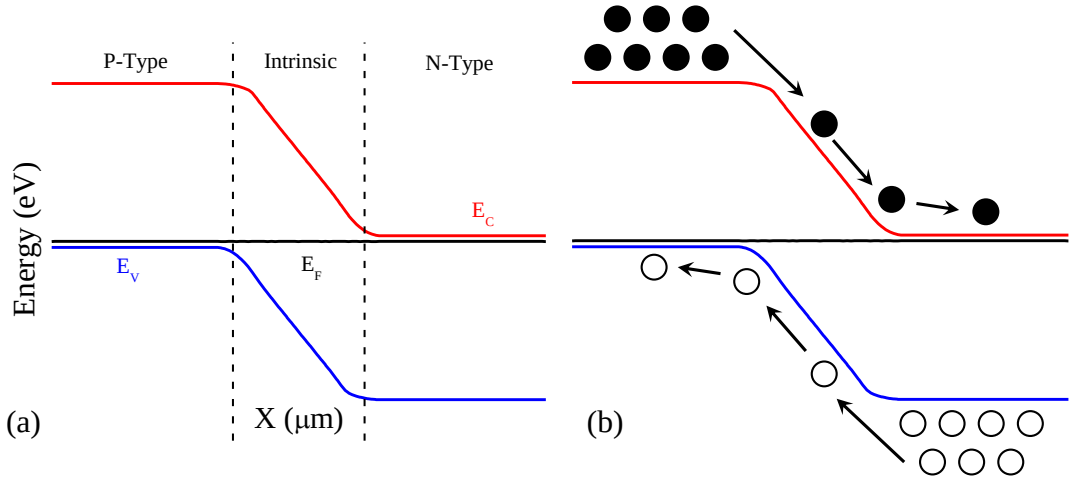

Figure 5.3 (a) Band diagram of a PIN diode assuming 1 x 10^{19} cm^{-3} doping concentration for n and p type. (b) Proposed method of extracting generated minority carriers from majority legs and transporting the minority carriers to their corresponding majority leg. Solid circles represent electrons and open circles represent holes.

intrinsic region to transport carriers will depend upon its dimensions as a shorter distance equates to a stronger built in field and decreased probability of recombination inside the intrinsic region. The intrinsic regions are separated into segments to reduce the heat flux penalty that is incurred by joining together the n and p legs. The goal of the intrinsic regions are to boost the maximum output power without increasing the heat flux substantially so that overall efficiency improves. The heat flux increase depends upon the number and

dimensions of the intrinsic regions, the vertical spacing between intrinsic regions, and the dimensions of the legs.

5.5 Results

A conventional and ladder TEG (Figure 5.4) were constructed with a leg height of 1μm and leg width of 250 nm where the ladder TEG has six intrinsic regions with dimension of 100 nm x 100 nm. The leg height and width dimensions were chosen based on previous work (Chapter 4.1, 4.2) where maximum power was observed for leg heights on the order of 1 μm with widths less than 500 nm. For these simulations the top contact

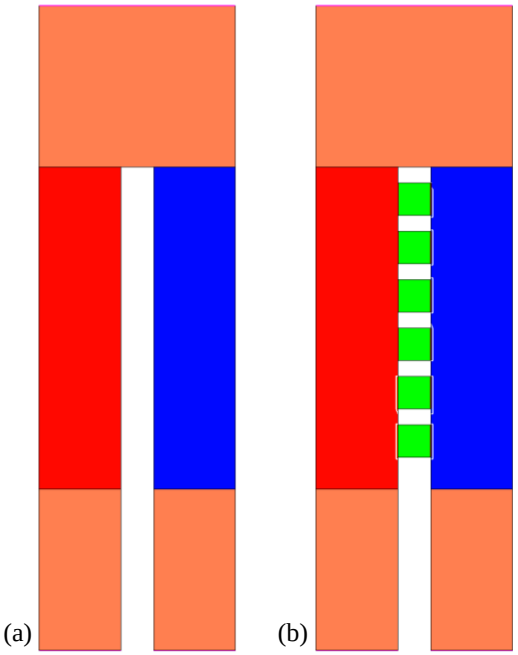

Figure 5.4 Conventional (a) and ladder (b) TEG images from simulation. Red is an n-type region, blue is a p-type region, green is an intrinsic region, and orange is a copper region.

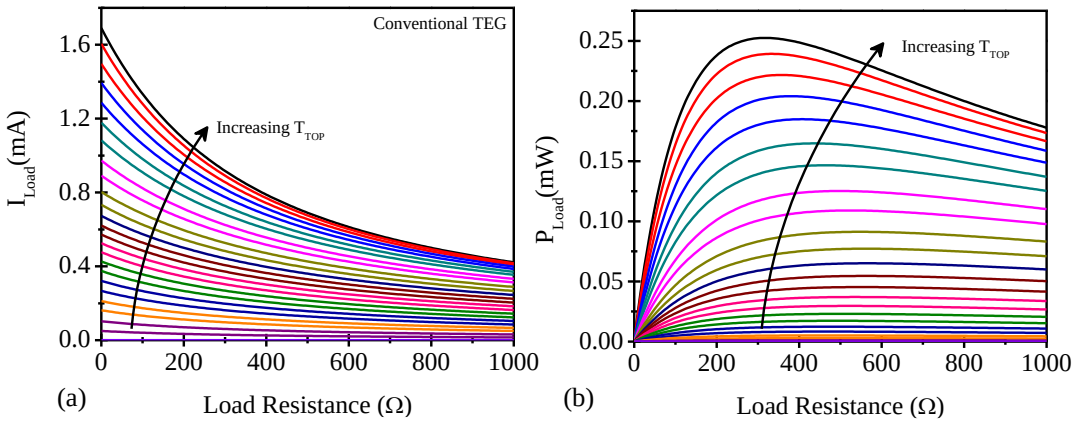

Figure 5.5 (a) Current and (b) output power through the load resistor as a function of load resistance for all T_{TOP} (conventional TEG).

temperature is swept from 300 K to 1500 K in increments of 50 K. At each increment, the current vs load resistance and heat flux are extracted. Current and output power vs. load resistance (Figure 5.5-b) follow expected behavior where the maximum power is observed when the TEG resistance equals the load resistance. At higher temperatures, load resistance corresponding to maximum power transfer decreases as TEG becomes less resistive due to increase in free carrier concentration. Similar results are observed for the ladder TEG.

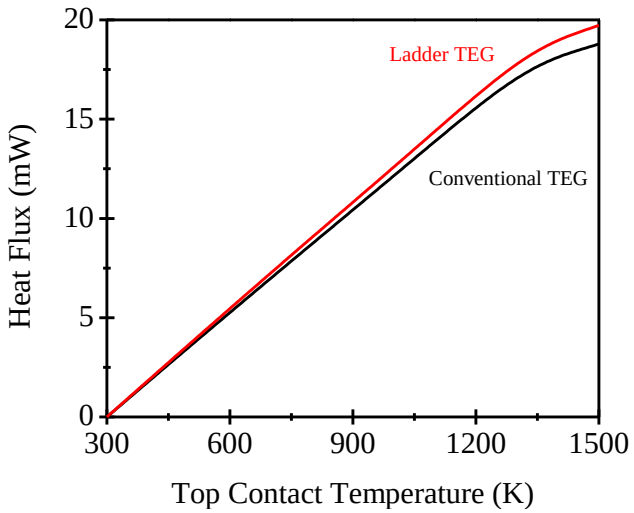

Figure 5.6 Heat flux as a function of T_{TOP} for conventional (black line) and ladder (red line) TEGs.

Heat flux (Figure 5.6) shows a linear behavior which is expected based on the constant thermal conductivity model used for Silicon Germanium. At lower temperatures, total thermal conductivity is mostly determined by the lattice thermal conductivity component. For Silicon Germanium, the lattice thermal conductivity is reduced (compared to pure Si or pure Ge) due to the alloying of Si and Ge for mole fractions of x = 0.2 to x = 0.8. As temperatures increases, the thermal conductivity is relatively temperature insensitive. However, the constant thermal conductivity model introduces error at higher temperatures where electronic thermal conductivity should increase total thermal conductivity (and also heat flux) due to the significant increase in free carrier concentration. For example, crystal silicon thermal conductivity increases from ~ 20 W/mK at 1650 K to 40 – 60 W/mK after melting (1687 K). A similar type of behavior is expected to occur Silicon Germanium.

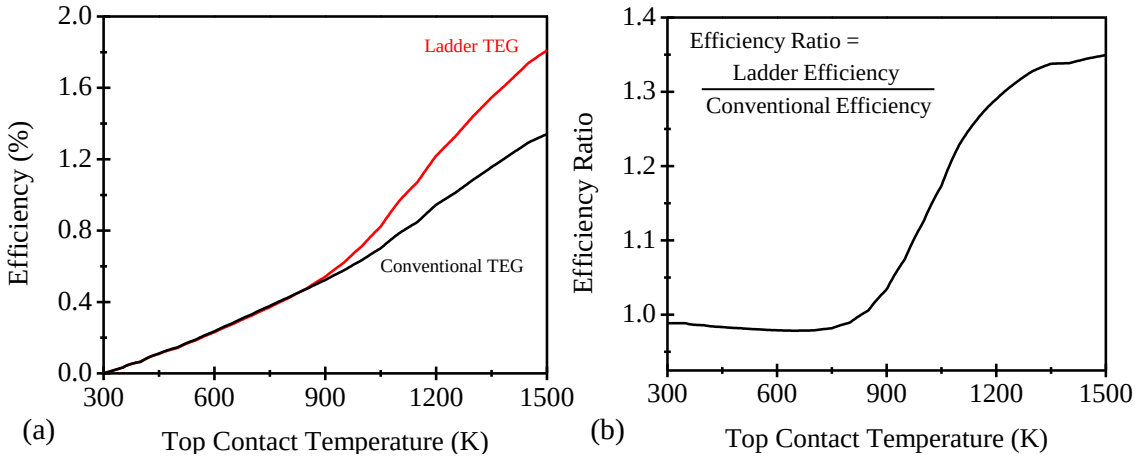

Figure 5.7 (a) Efficiency of ladder (red line) an conventional (black line) TEGs as a function of T_{TOP}. (b) Efficiency ratio as a function of T_{TOP}.

As expected, ladder TEG has larger heat flux compared to the conventional TEG but the overall increase is relatively small for this geometry. Efficiency (Figure 5.7a) is computed using the maximum power and heat flux data extracted. For temperatures above

~ 900 K, the ladder TEG has improved efficiency which peaks at ~1.8% at 1500 K, ~35% improvement vs. the conventional TEG. Another way to interpret the efficiency is to plot the efficiency ratio (Figure 5.7b), which is defined as the ladder TEG efficiency divided by the conventional TEG efficiency. Below ~ 900 K, the ladder TEG is slightly less efficient (efficiency ratio < 1) compared to the conventional TEG due to the small increase in heat flux (output power is ~ the same). At 900 K, the minority carrier concentration of $Si_{0.7}Ge_{0.3}$ approaches ~1 x 10^{18} cm^{-3} where the intrinsic regions start to capture enough of the diffusing, generated minority carriers to contribute to increased output power. When minority carrier concentration is lower, there is insufficient amount of minority carriers to capture and any that are captured are likely recombined inside the intrinsic region. As temperature increase, an increasing number of minority carriers are generated (along with an increase in the majority carrier concentration) and the intrinsic regions can capture a larger portion of the generated minority carriers.

The minority carrier capture can be seen by plotting the minority carrier current with vector arrows (Figure 5.8a-b). As expected, holes in both legs diffuse along the temperature gradient from hot to cold (top to bottom in this case). In the case of the ladder TEG, there is also some x-direction hole current through the intrinsic regions from the n leg to the p leg. However, at the top two intrinsic ladder "rungs" there is little to no hole current traversing from n to p leg as indicated by the vector arrows. Holes flow into

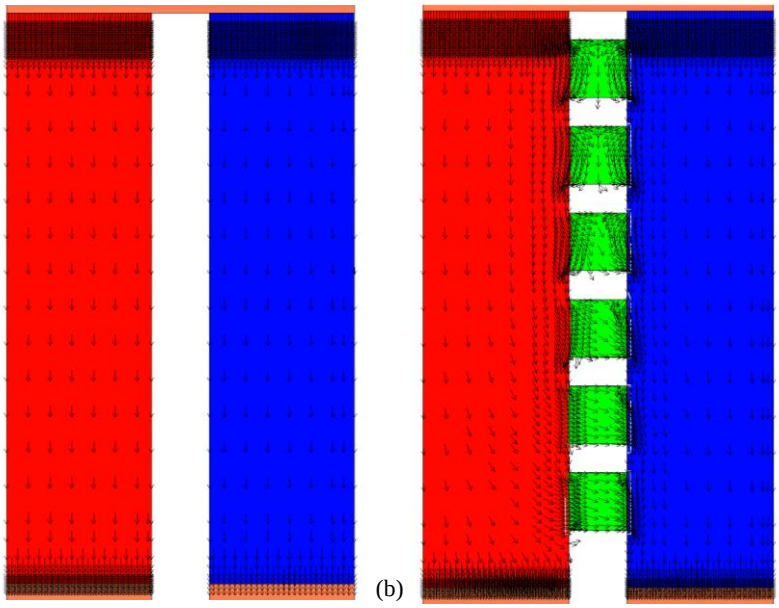

Figure 5.8 Simulation image of conventional (a) and ladder (b) TEGs showing vector arrows for hole current density. T_{TOP} is 1500 K.

the top two intrinsic regions from both the p-leg and the n-leg but do not cross and instead flow back out into their respective origin legs. It is not until the third intrinsic region that hole current from the n-leg reaches the p-leg where subsequent intrinsic regions show a greater amount of hole current flowing across.

The lack of hole current flowing through the top two intrinsic regions is a result of two factors. Firstly, as T_{TOP} increases, the built in electric field formed by the PIN junction diminishes resulting in less force being exerted on minority carriers. This can be observed by extracting the band diagrams across the ladder TEG rungs (Figure 5.9a). The PIN junction formed by intrinsic region near the top of ladder TEG has a nearly flat band diagram where minority carriers would experience little force from the electric field. Flattening of the band diagram is a result of band gap reduction and the p and n regions becoming ~intrinsic at higher temperatures. The electric field strength increases for PIN

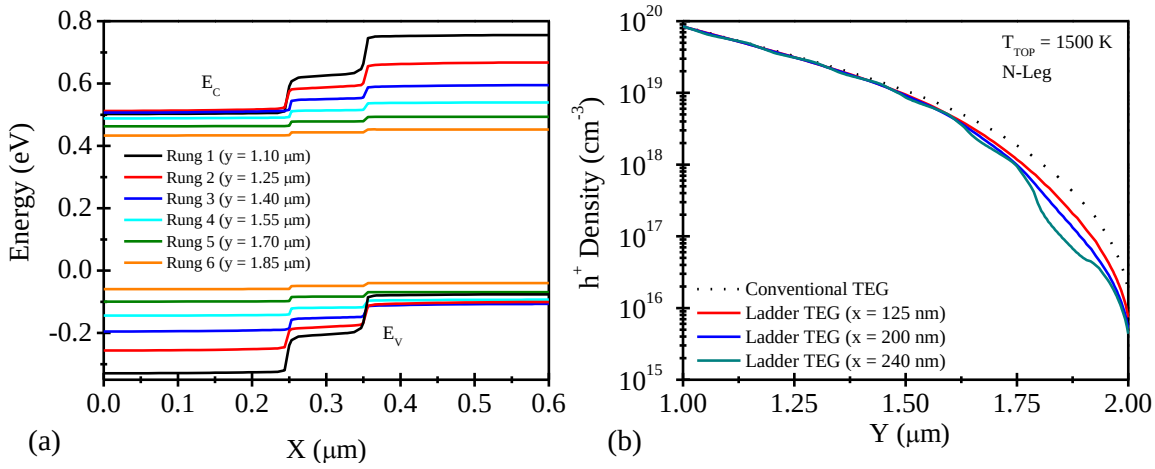

Figure 5.9 (a) Band diagrams across the ladder TEG intersecting the middle of all six intrinsic regions (y locations indicated on legend) for a T_{TOP} of 1500 K. Fermi levels were omitted for clarity. (b) Hole density along the length of the n-leg for conventional (dotted line) and for ladder TEG (red, blue, and green). Three different cuts were taken for the ladder TEG at different x positions (x = 125, 200, and 240 nm) to show the change in hole concentration along the width of the leg.

junctions further down the ladder where the temperature is lower. Secondly, the hole and electron density on either side of the top two intrinsic regions are nearly the same, so there is very little to no carrier gradient in the x direction. At or near the melting temperatures, the electron and hole density are approximately equal. Given that the band diagram is mostly flat, there will be littler carrier movement across the intrinsic region.

Minority carrier transfer across the intrinsic regions is shown by the vector arrows but can also been inferred by looking at the minority carrier concentration (Figure 5.9b) in the TEG legs. For the ladder TEG, three different cuts are shown at various x direction locations (100, 200, 240 nm) to show the variance in hole density along the width. At 1.5 μm (approximately where the third ladder intrinsic region begins), the hole density for the ladder starts to deviate from the conventional TEG for all three cuts. The hole density continues to decreases further down the n leg but is highly dependent upon the distance

away from the interface with the intrinsic region. Very close to the interface (x = 240 nm), the hole density is the smallest. This cut shows a wavy trend along the length of the leg due to the very close proximity to the interface. Further away from the interface, hole density increases, demonstrating the width dependency of the intrinsic regions ability to capture minority carriers. A similar type of behavior is observed for electrons in the p-leg. A T_{TOP} of 1500 K is the largest temperature gradient simulated and for smaller T_{TOP} the intrinsic regions on the top of the ladder do transfer minority carriers.

The efficiency improvement demonstrated by the ladder TEG can also be observed by extracting the open circuit voltage (V_{OC}) and effective Seebeck coefficient (V_{OC} divided by ΔT) and comparing those values to the conventional TEG. As discussed in the ZT introduction section, increasing the Seebeck coefficient improves the thermoelectric efficiency where ZT is proportional to S^2. A separate simulation was run where a large resistance (1 GΩ) was connected to p-leg and n-leg metal contacts while

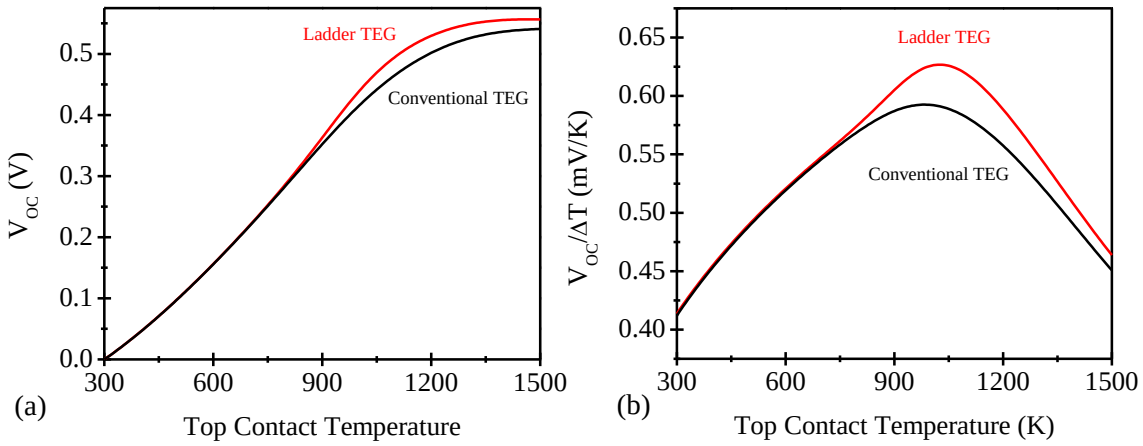

Figure 5.10 (a) Open circuit voltage and open circuit voltage divided by temperature gradient(b) for ladder (red line) an conventional (black line) TEGs as a function of T_{TOP}.

the T_{TOP} was swept from 300 to 1500 K in 50 K increments. A larger contact resistance is used to simulate an experimental opn-circuit Seebeck voltage measurement.

The ladder TEG exhibits enhanced V_{OC} and effective Seebeck coefficient (Figure 5.10a-b) starting at ~900 K which also coincides with the temperature where efficiency enhancement starts to be observed. The effective Seebeck coefficient decreases at high temperatures (for both ladder and conventional TEG) which is expected as normally reported Seebeck confidents also show a decrease at higher temperatures due to bipolar transport. Removing minority carriers enhances the effective Seebeck coefficient at higher temperatures as the Seebeck contribution from minority carriers is partly responsible for high temperature reduction in Seebeck coefficient. There is still a decrease in Seebeck voltage for the ladder TEG at higher temperature as not all minority carriers are removed by the PIN junctions. Furthermore, the reduction of band gap at higher temperatures is the same for both ladder and conventional TEGs which also contributes to reduced Seebeck

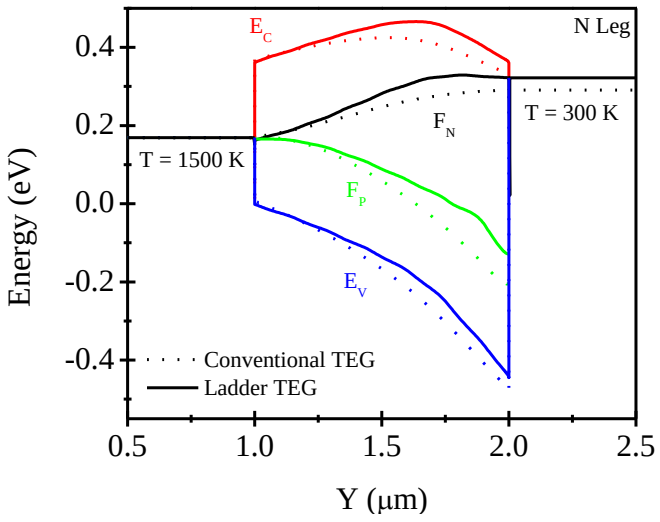

Figure 5.11 Band diagram of n-leg of ladder (solid lines) and conventional (dotted lines) TEGs for a T_{TOP} of 1500 K for a maximum power condition (load resistance corresponding to maximum output power). The band diagrams were centered in the middle of the n-leg (x = 125 nm).

coefficient.

Band diagrams (Figure 5.11) of the n-leg for the ladder (solid lines) and conventional (dotted lines) TEG were extracted at a T_{TOP} of 1500 K for a maximum power condition. Increase in electric potential (Seebeck effect), and reduction in minority carrier concentration (difference between F_N and F_P) is shown for the ladder TEG. Band gap reduction at elevated temperatures is shown but is underestimated where the temperature is at or near the melting point. It is expected that the band gap should be extremely small for a liquid semiconductor. However the default Sentaurus band gap model does not take this into account (resulting in error). Along with the very small band gap, free carrier concentration is expected to be on the order of 10^{22} cm^{-3} at the melting temperature. We estimate that the ladder TEG would exhibit even greater efficiency enhancement compared to the conventional TEG if a melting approximation was included. Due to the default Sentaurus model carrier generation is underestimated at or near the melting temperature.

5.6 TEG Leg Width Analysis

The intrinsic regions of the ladder TEG only collect a portion of the generated minority carriers from each leg as minority carriers that are located at the opposite end of a leg are unlikely to be captured by the electric field in the intrinsic region. Scaling the width of the legs should allow for more minority carriers to be extracted by the intrinsic region. A set of simulations was run where the width of the legs was scaled from 250 nm to 5 nm in several increments (250, 100, 50, 25, 10, and 5 nm) where maximum power and heat flux were extracted to calculate efficiency as a function of T_{TOP}. Leg height was 1 μm for both TEG designs and the number of intrinsic regions and intrinsic region dimensions

were constant as well (six, 100 nm x 100 nm respectively) for all ladder TEG simulations. Metal contact dimensions were scaled to accommodate change in leg width.

Conventional TEG exhibit increasing efficiency for increasing width for all T_{TOP} (Figure 5.12a). Ladder TEG shows increasing efficiency for increasing width for T_{TOP}

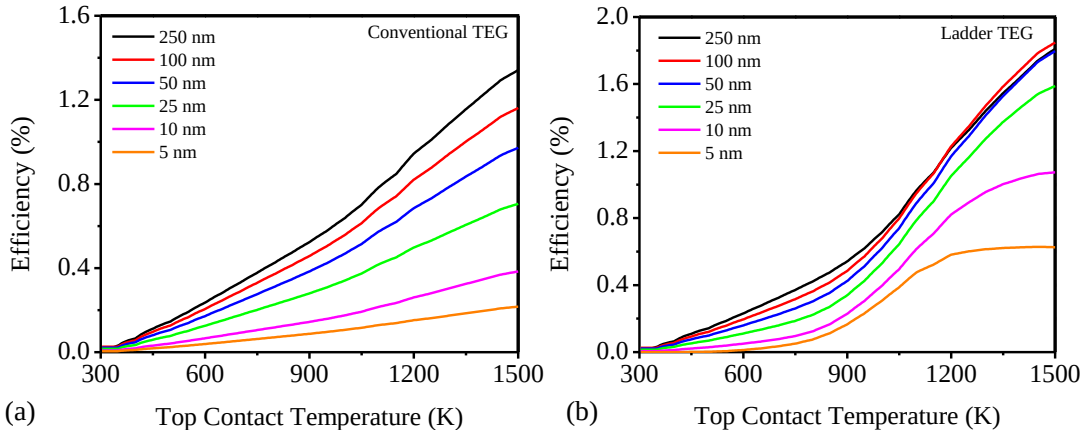

Figure 5.12 Efficiency as a function of T_{TOP} for conventional (a) and ladder (b) TEG at leg widths of 5, 10, 25, 50, 100, and 250 nm.

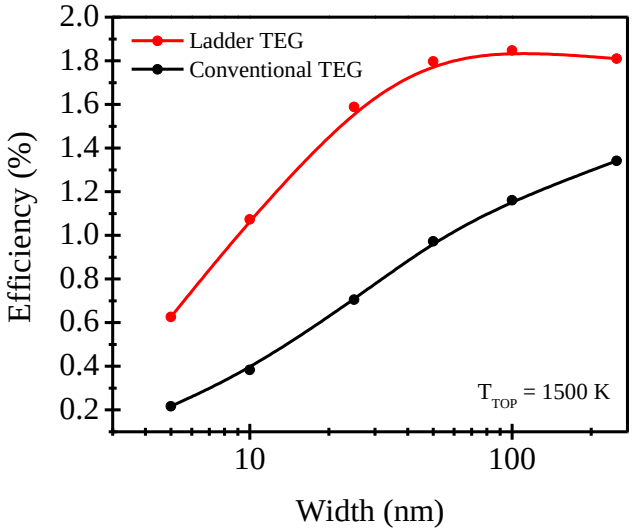

Figure 5.13 Efficiency of ladder (red) and conventional (black) as a function of leg width at a T_{TOP} of 1500 K.

< ~ 1300 K (Figure 5.12b). Above this, an optimum efficiency is observed for leg widths between 25 – 100 nm (Figure 5.13). Optimum height/width is a consistent observation

based on simulation results from our previously published work (Chapter 4.1, 4.2). For the conventional TEG efficiency an optimum width may be observed if larger widths were simulated. 5 nm leg width exhibits the worst overall efficiency due to extremely

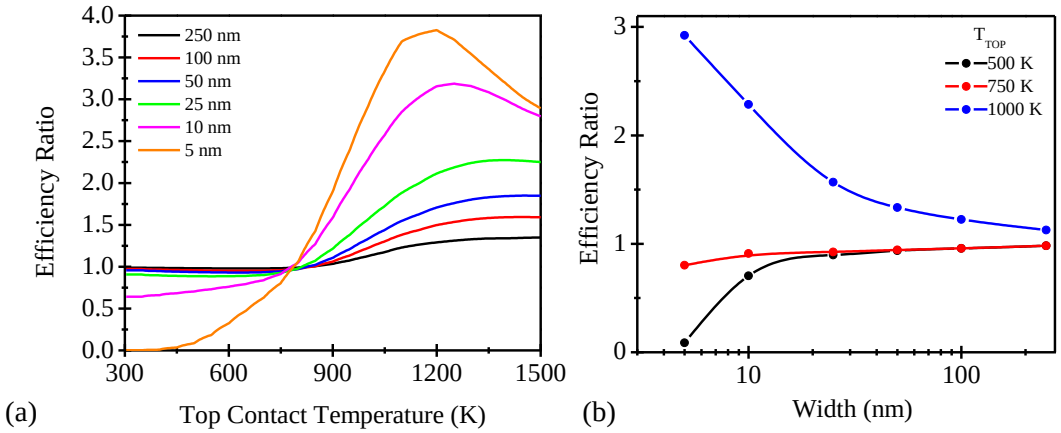

Figure 5.14 (a) Efficiency ratio as a function of T_{TOP} for TEG leg widths of 5, 10, 25, 50, 100, and 250 nm. (b) Efficiency ratio as a function of width for T_{TOP} = 500 K (black), 750 K (red), and 1000 K (blue).

large leg resistance (for a height of 1 μm) even though the heat flux is the lowest.

While the 5 nm leg width has the worst overall efficiency for either ladder or conventional TEG, it exhibits the largest efficiency ratio (Figure 5.14a). At higher temperatures (wherever the efficiency ratio is > 1), the efficiency ratio increases as the leg width decreases (For example, T_{TOP} = 1000 K, Figure 5.14b). However, at lower temperatures (T_{TOP} < ~750 K), efficiency ratio decreases as the leg width decreases. The decrease in efficiency ratio is due to the ladder TEGs very low output power below 750 K (Figure 5.15b). At ~700 K, the ladder TEG power drops below the conventional TEG and decreases by several orders of magnitude as the T_{TOP} decreases (Figure 3.23b). Above 700 K, the ladder TEG power overcomes the conventional TEG and at 1500 K is ~4-5 times larger (Figure 5.15a).

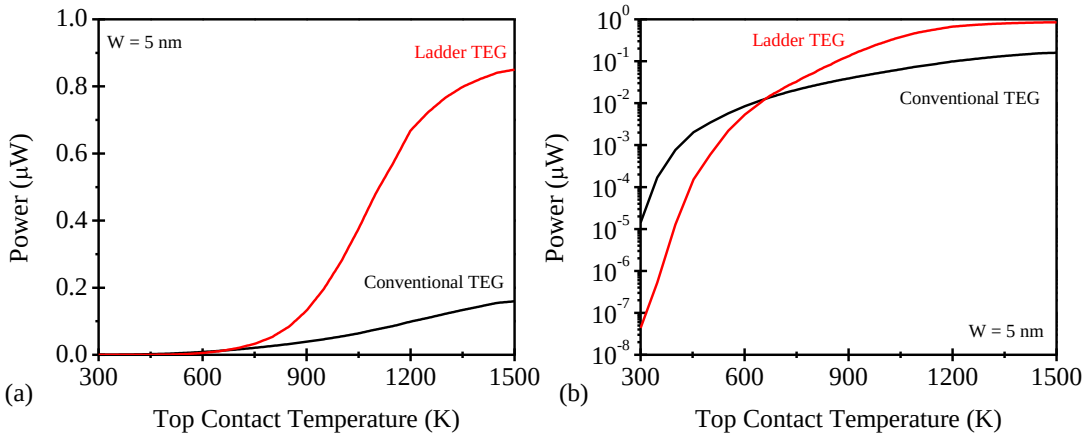

Figure 5.15 Power as a function of T_{TOP} for ladder (red) and conventional (black) TEGs at a leg width of 5 nm in linear (a) and log (b) scales.

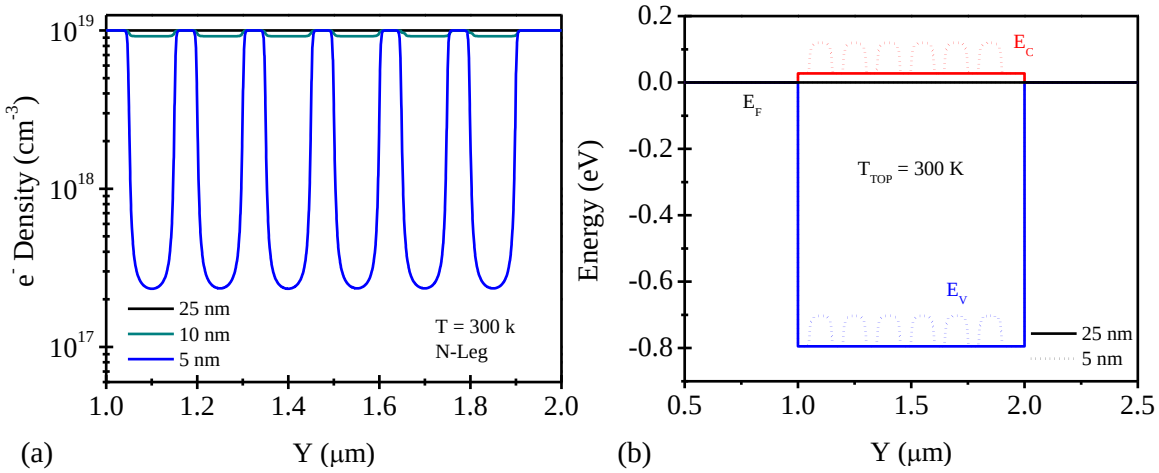

Figure 5.16 (a) Electron density along the length of the n-leg at 300 K for 25 nm (black), 10 nm (green), and 5 nm (blue). (b) Band diagram of n-leg for 5 nm (dotted) and 25 nm (solid) at a T_{TOP} of 300 K. All cuts were taken at half of the leg width.

The poor output power of the ladder TEG at lower temperatures is a result of depletion of the TEG legs due to the PIN junctions (Figure 5.16a). At 5nm leg width, significant depletion of majority carriers occurs wherever a PIN junction is formed along the length of the leg. 10 nm leg width exhibits a small amount of majority carrier depletion but it is no longer observed once the width is 25 nm. Depletion effects can also be observed in the band diagram along the length of the n-leg (Figure 5.16b). At 25 nm leg width, the

conduction and valence bands are flat which is expected at a T_{TOP} of 300 K. For 5 nm leg width, energy barriers in the conduction band and quantum wells in the valence band form wherever there is a PIN junction forming on the n-leg. This shows the depletion of majority carriers and accumulation of minority carriers, both of which are detrimental to device performance. As the T_{TOP} is increased to 350 K, electrons that would normally diffuse from the hot side and generate power are unable to flow due to the energy barriers in the

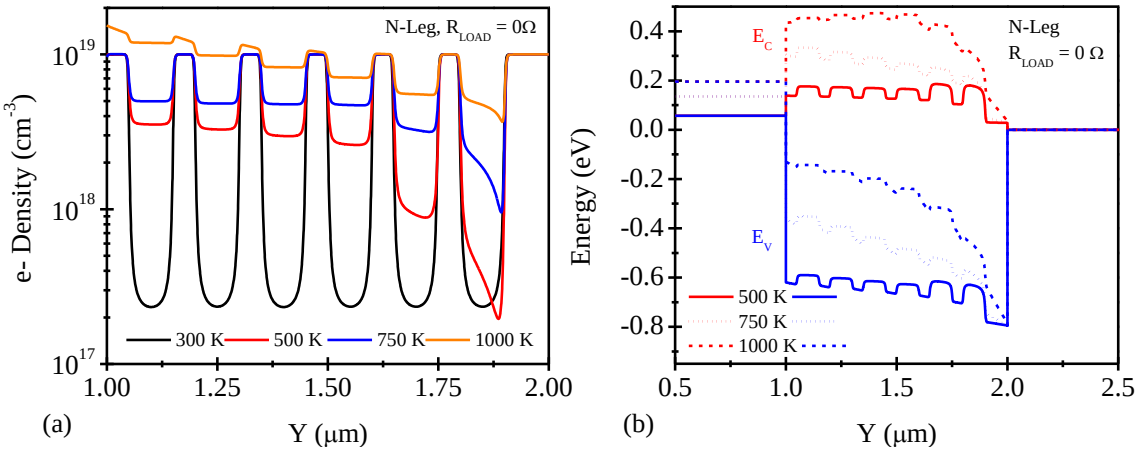

Figure 5.17 (a) Electron density along the length of the n-leg at 300 K (black), 500 K (red), 750 K (blue), and 1000 K (orange). (b) Band diagram along the length of the n-leg at 500 K (solid), 750 K (dotted), and 1000 K (dashed). Electron and hole quasi fermi levels are not shown for clarity. Load resistance is 0 Ω for both graphs. Leg width is 5 nm.

conduction band. Any electrons that have sufficient kinetic energy to overcome the barriers would likely to recombine with the excess minority carriers.

Depletion begins to decrease as the T_{TOP} reaches ~ 750 K where the ladder TEG output power overtakes the conventional TEG (Figure 5.15a). The resulting decrease in depletion as T_{TOP} increases is due to carrier generation in the intrinsic regions (Figure 5.17a) and at sufficiently high enough temperatures carrier generation in the n-leg (900 – 1000 K). At 500 K there are still significant energy barriers in the conduction band (Figure 5.17b) especially at the bottom of the leg where the temperature is lower. However at

higher temperatures, the energy barriers are reduced allowing for a significant current to flow.

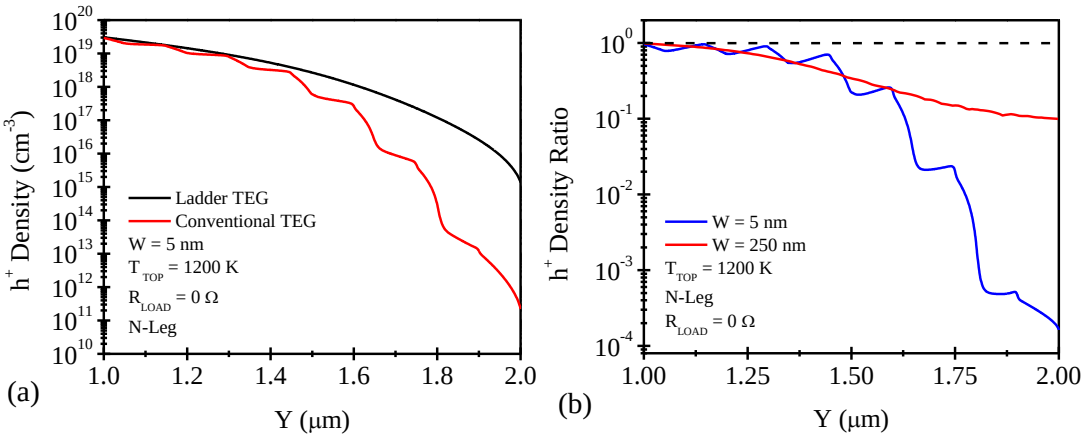

Figure 5.18 (a) Hole density along the length of the n-leg at a T_{TOP} of 1200 K for conventional (black) and ladder (red) TEGs. (b) Hole density ratio (ladder TEG hole density / conventional TEG hole density) for widths of 5 nm and 250 nm at a T_{TOP} of 1200 K in the N-leg.

Once the T_{TOP} > than 750 K, depletion is reduced enough that the ladder TEG outputs considerably more power than the conventional TEG. This is a result of considerable extraction of minority carriers (Figure 5.18a) which reduces recombination and once transported to their respective majority legs increases the current density. At a very narrow width, the intrinsic regions are more effective at reducing minority carriers (Figure 5.18b) compared to larger widths. At 250 nm, the ladder TEG reduces the minority carrier concentration by a factor of 10 at the bottom of the TEG but at 5 nm the reduction is 10^3-10^4. Cuts along the y-axis were taken at the midpoint along the width of the TEG leg. The jagged behavior of the hole density ratio for 5 nm is a result of extremely narrow leg width. It is also observed for other widths when extracting hole density very close (1-5 nm) to the intrinsic region interface. The reduction in minority carriers substantially

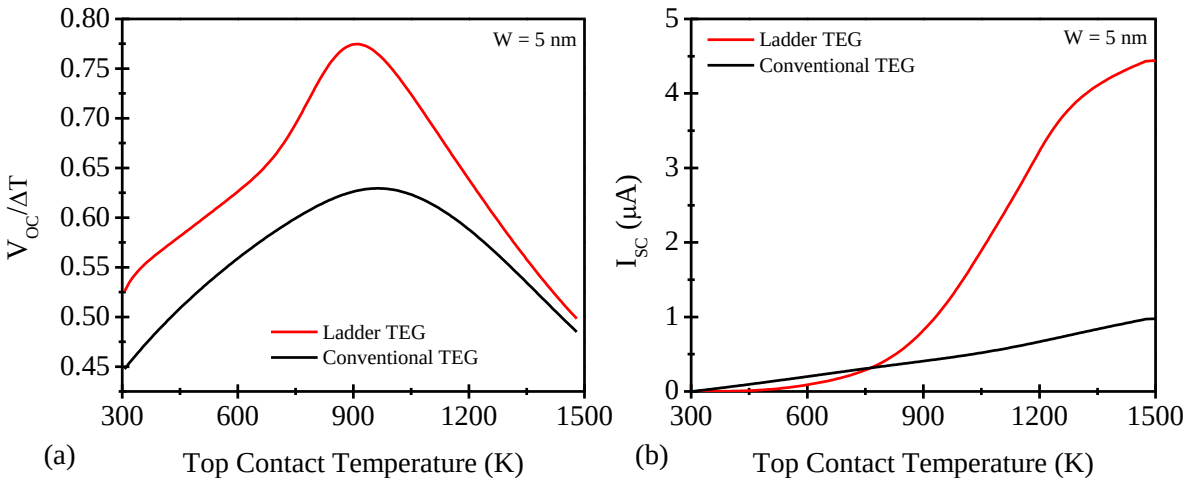

Figure 5.19 (a) Effective Seebeck coefficient ($V_{OC}/\Delta T$) (a) and short circuit current (I_{SC}) (b) as a function of T_{TOP} for ladder (red) and conventional (black) TEGs.

improves the effective Seebeck coefficient (Figure 5.19a) for the ladder TEG, showing far more enhancement than was seen for a leg width of 250 nm.

For a width of 5 nm, the transported minority carriers contribute significantly to the current density of their respective majority carrier leg. The short circuit current (Figure 5.19b) is much larger for the ladder TEG compared to the conventional TEG at $T_{TOP} > \sim$ 900 K. The improvement in short circuit current is also observed by extracting the electron current density along the length of the n-leg (Figure 5.20a) where the ladder TEG shows an increases in electron current density wherever a PIN junction is formed. Each intrinsic region contributes to the total current density in a step-wise fashion where it is almost an order of magnitude larger at the bottom of the leg for the ladder TEG compared to the conventional TEG. For larger widths, adding the transported minority carriers to their respective majority carrier leg results in a small increase in the majority current density. At a width of 250 nm, the electron current density in the n-leg for the ladder TEG increases along the length of the leg but only exceeds the conventional TEG electron current density by a factor of 1.3 at the bottom of the leg (Figure 5.20b).

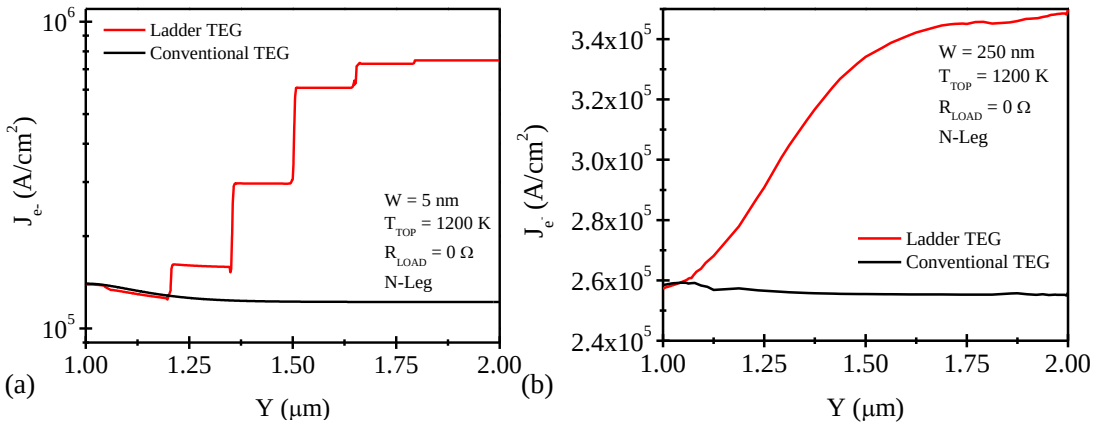

Figure 5.20 Electron current density along the length of the n-leg for widths of 5 nm (a) and 250 nm (b) at a T_{TOP} = 1200 K. Ladder TEG (red), conventional TEG (black)

Depletion is detrimental to TEG performance and effectively eliminates the use of the ladder TEG geometry (for leg widths less than 25 nm) at temperatures below 700 – 800 K. One possible method to reduce depletion is to change the PIN junction into a PN

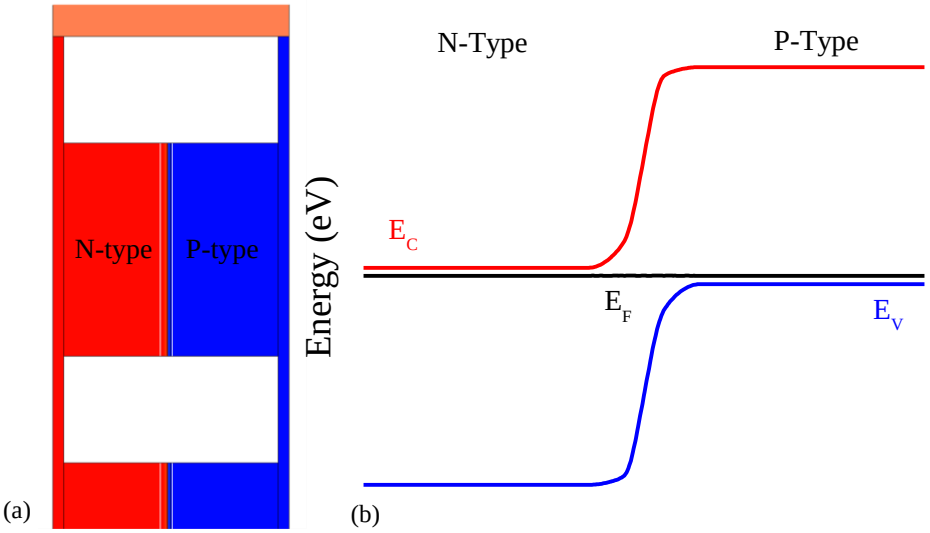

Figure 5.21 (a) PN junction based ladder TEG with doping concentration of 10^{19} cm^{-3}. Red indicates n-type and blue indicates p-type. (b) Band diagram across the middle of a ladder rung for PN junction TEG at 300 K. White lines near PN junction indicate depletion region edges.

junction. Instead of an intrinsic region bridging the P-leg and N-leg of the TEG, a PN junction is formed by extending a small section of each leg, meeting in the middle. (Figure 5.21a). The resulting PN junction energy band profile (Figure 5.21b) can transport minority carriers in a similar fashion as the PIN junction based TEGs. The formation of the PN junction in the center of the ladder rung does result in some depletion but it only extends to a small region outside of the PN junction interface, and there is no observable depletion of majority carriers in the TEG legs.

Without any depletion in the TEG legs, the PN junction based ladder TEG has improved efficiency at lower T_{TOP} (Figure 5.22) and still exhibits the same improved efficiency at higher T_{TOP} that is observed for a PIN junction based ladder TEG. At T_{TOP} < 750 K, the PN junction based ladder TEG has more power versus the PIN junction based ladder TEG but slightly lower power at very high T_{TOP}. Efficiency ratio (Figure 5.23) of PN junction based ladder TEG is larger than 1 at lower T_{TOP} as the output power is large enough to overcome heat flux penalty. Due to the lower output power at higher T_{TOP}, the

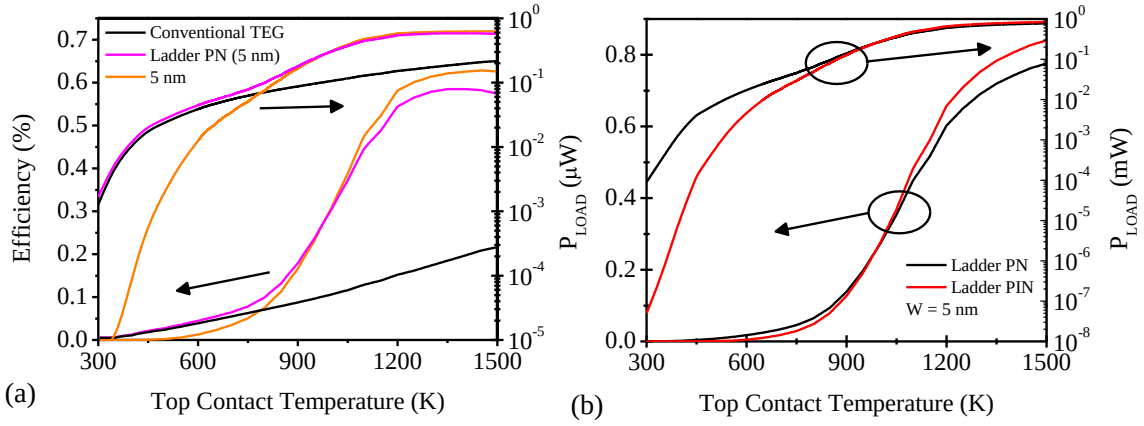

Figure 5.22 (a) Efficiency of ladder TEG with PIN (orange) and with PN (magenta) and conventional TEG (black) as a function of T_{TOP} in linear and log scale. (b) Power for ladder TEG with PIN (red) and with PN (black) as a function of T_{TOP} in linear and log scale.

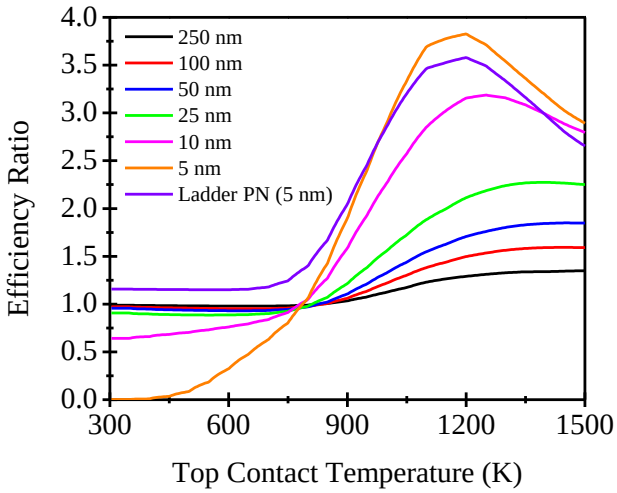

Figure 5.23. Efficiency ratio as a function of T_{TOP} for TEG leg widths of 5, 10, 25, 50, 100, and 250 nm and PN junction based TEG.

efficiency ratio of PN junction based ladder TEG is lower than the PIN junction based ladder TEG.

5.7 PN vs PIN Junction TEGs – Solid Junction TEGs

As shown in the previous section, PN junctions can be used instead of PIN junctions for the ladder TEG to achieve similar efficiency enhancement. PN junctions are advantageous as they will not suffer from dopant migration which is problematic for the proposed PIN junction design above. At elevated temperatures, dopants in the p and n type regions can diffuse into the intrinsic region and this may reduce the performance of the PIN based ladder TEGs. PN junction based ladder TEGs may be more resistant to dopant migration vs. PIN junction as the doping concentration is approximately constant in the p and n regions. Sentaurus physics models do not take into account dopants migrating at higher temperatures and thus introduce a potential source of error for the previous simulations.

In addition to the ladder TEG design utilized in Chapter 5.6, a solid (continuous) junction design (solid TEG) is also employed (Figure 5.24) where the p and n regions are connected along the entire length of the TEG legs. The benefit of this design is that it allows for maximum extraction of minority carriers compared to the ladder geometry. However, careful consideration must be taken as a continuous interface between the legs will also increase heat flux, potentially reducing overall efficiency even if output power is improved.

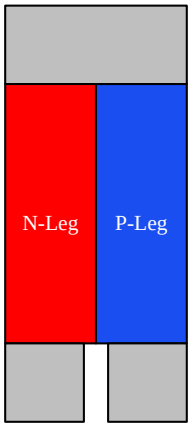

Figure 5.24 PN Junction TEG diagram.

Five different geometries were created for the initial comparison simulations (Figure 5.25-e); a conventional TEG (control device), two ladder designs (PN and PIN junction, and two continuous designs (PIN and PN junction) in an attempt to have a more fair comparison between PIN and PN junction designs. As shown in Chapter 5.6, the dimensions of the TEG leg are one of the factors that control efficiency. For this comparison we have tried to minimize any geometric variations between designs so that only the junction type determines the efficiency.

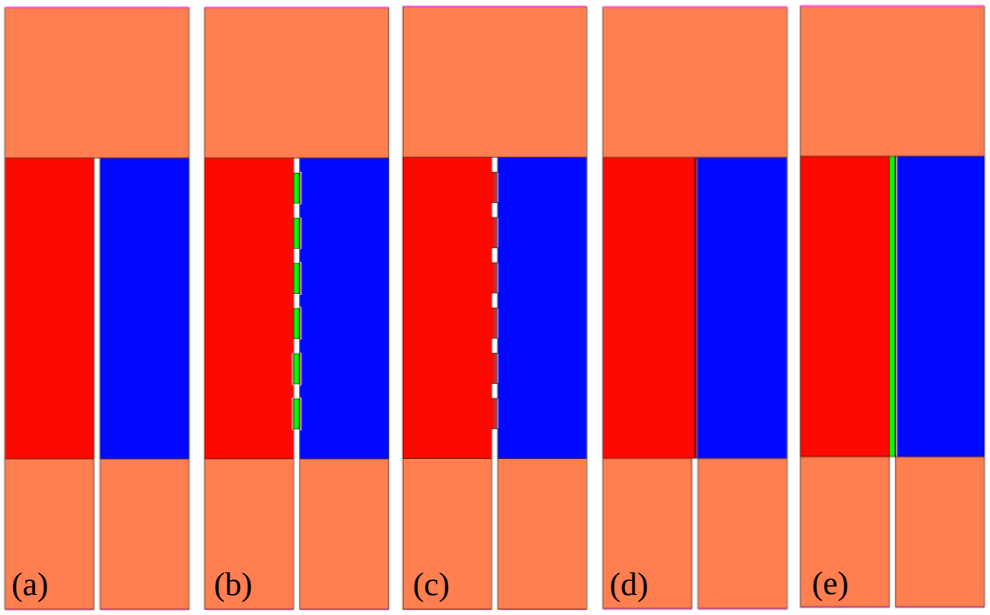

Figure 5.25 Simulation images of conventional (a), ladder PIN (b), ladder PN (c), solid PN (d) and solid PIN (e). Leg width is 290 nm for conventional, ladder PIN and PN, and solid PIN. For solid PN leg width is 300 nm. Intrinsic regions are 20 nm x 100 nm (L x H) for the ladder PIN TEG. Rungs on the PN ladder are 20 nm x 100 nm (L x H) and at the same locations as the PIN ladder intrinsic regions.

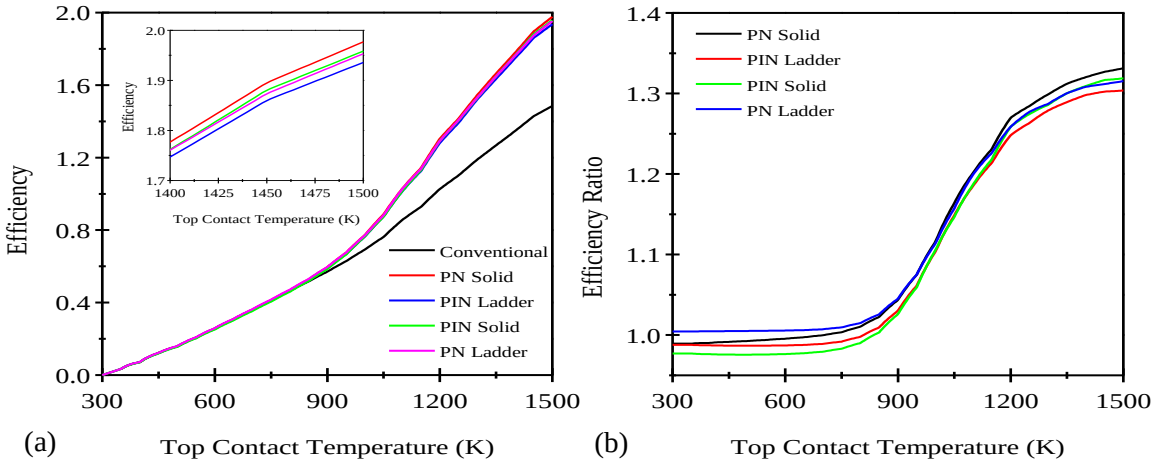

Figure 5.26 Efficiency (a) and efficiency ratio (b) as a function of T_{TOP} for all five geometries tested.

Efficiency and efficiency ratio were extracted for all five geometries (Figure 5.26a-b) where the PN and PIN junction designs exhibit very similar efficiency enhancement. The solid PN geometry has the largest efficiency enhancement for $T_{TOP} > 900$ K but is only a small fraction better than other three junction based designs in this temperature range. The ladder PN has efficiency ratio larger than 1 for all temperatures simulated, something that has not been achieved for any PIN based TEG. The output power increase at $T_{TOP} < 900$ K is sufficiently large to outweigh the increase in heat flux allowing the ladder PN TEG to outperform the conventional TEG as a result.

Ladder PN and solid PN geometries demonstrate similar minority carrier extraction as observed in ladder PIN simulations (Figure 5.27a-b). Minority carriers are attracted by the built-in field formed by the PN interface resulting in a decrease in minority carriers. Similarly to the ladder PIN TEGs, there is little minority carrier current flow near the top of the TEG legs when the temperature is sufficiently large (T = 1200 K for the images shown in Figure 5.27a-b). The built-in field decreases as the temperature across the junction increases.

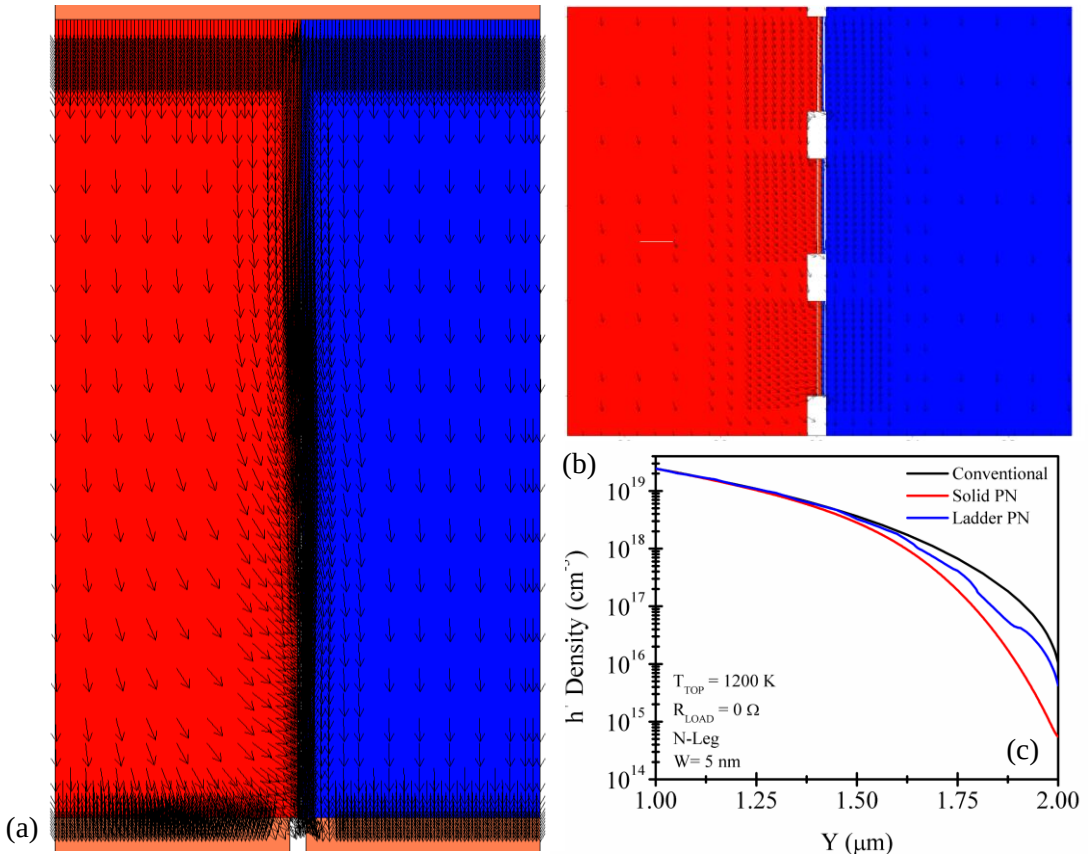

Figure 5.27 Hole current density shown via vector arrows for solid PN (a) and ladder PN (b) TEGs at a T_{TOP} of 1200 K. Darker areas are a result of heavy meshing and clumping of vector arrows. (c) Hole density in the n-leg for conventional (black), solid PN (red), and ladder PN (blue) TEGs at a T_{TOP} of 1200 K.

The solid PN TEG is more effective at collecting minority carriers compared to the ladder TEG (Figure 5.27c) which is expected due to increased junction area. However, the solid PN TEG has larger heat flux.

PN junction based TEGs offer the same possibility of efficiency enhancement as PIN junction based TEGs. However, simulations run with larger intrinsic region dimensions (L x H = 100 nm x 100 nm) resulted in lower efficiency enhancement at higher temperatures especially if doping concentration of ladder rungs was greater than TEG legs. In this case, the increased doping concentration results in increased recombination of

majority and minority carriers inside of the ladder rungs as SRH recombination is proportional to doping concentration. Although built in field strength can be larger with a highly doped PN junction, this benefit is offset by the increase in recombination.

5.8 Ladder TEG Fabrication Outlook

Fabricating the ladder TEG geometry shown in this work is a considerable challenge given the leg dimensions and design complexity. Simulated geometries used single-crystal semiconductors with ideal doping concentration distribution throughout the structure and dimensions as small as 5 nm. Further, the segmented rungs of the ladder structure were separated by vacuum layers (although simulations could have been done with oxide in between) which would be extremely difficult to fabricate.

Ladder TEGs could possibly be fabricated using nanorods (NRs) coated with nanocrystals of suitable semiconductors for given intended temperature ranges of the TEGs. Figure 5.28a-f shows example ZnO NRs grown by chemical bath deposition [82]. Such NRs are attractive due to low fabrication cost, low temperature growth, and

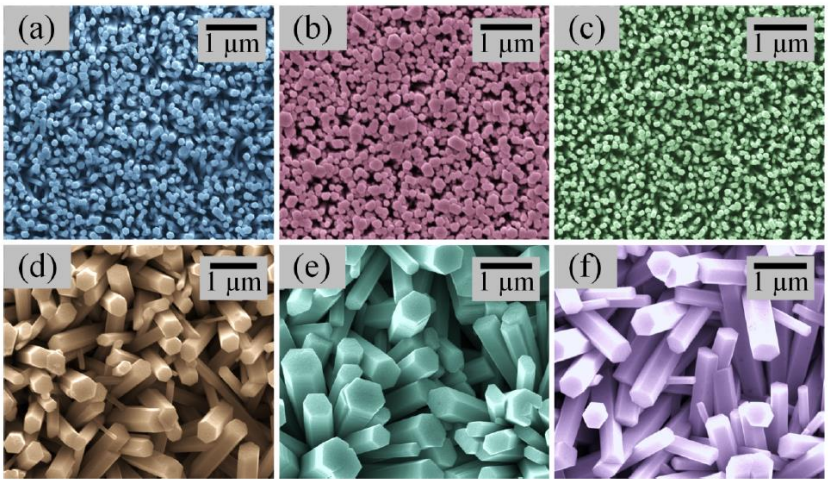

Figure 5.28 (a) False colored scanning electron microscope images of ZnO nanorods with average diameter of (a) ~100 nm (b) ~150 nm, (c) ~100 nm, (d) ~400 nm, (e) ~600 nm, and (f) ~500 nm. Figure from [82].

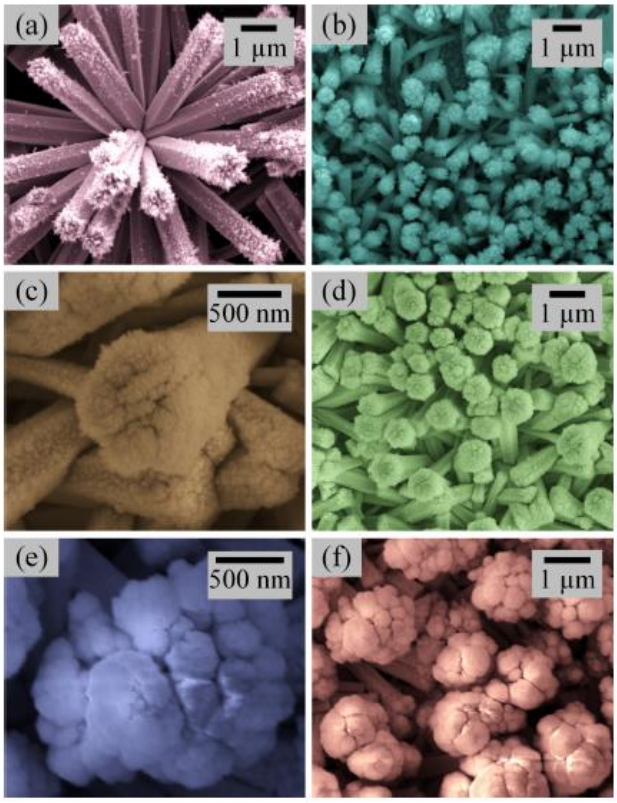

Figure 5.29 False colored scanning electron micrographs of ZnO nanostructures sputtered over the ZnO nanorods. A variety of different crystalline structures form during the sputtering process. Figure from [82].

compatibility with various substrates.

NRs can be grown with high packing density with vertical alignment where nanocrystals (Figure 5.29a-f.) can be grown around the outside of the NR using voltage pulse induced sputtering[82]. In this example, depending upon the pulse duration and amplitude, a variety of nanostructures were observed along the outside of the NRs. Nanocrystals or other nanostructures deposited on the NRs could function as the intrinsic regions of the PIN junction (or similarly to the PN junction interface) extracting minority carriers from the TEG legs to improve efficiency. Future studies on the thermoelectric

properties of the NRs and nanocrystals would be required to realize the possibility of NR based ladder TEGs.

6 Conclusion

Improving the efficiency of TEGs requires advances in material engineering as well as innovative TEG designs. Modeling TEG operation is a key component to developing better TEG designs and characterizing device performance over a wide range of temperatures. Semiconductor devices can be modeled using an effective media approximation or a drift-diffusion equation. Effective media approximations use a simpler approach to current continuity whereas a drift diffusion approach incorporates semiconductor band structure, electrons and hole density, and generation/recombination. Phase change memory cell operation is commonly simulated using an effective media approximation while most semiconductor devices (such as the RingFET) are modeled using a drift-diffusion approach. Finite element software such as COMSOL multi-physics and ANSYS are typically utilized for effective media approximation simulations while Synopsys Sentaurus is an industry standard semiconductor modeling software. In this work we simulate the operation of μTEGs using Synopsys Sentaurus as it has the most robust semiconductor models as well as a dedicated library of material parameters.

Using the Synopsys Sentaurus thermodynamic model, we have studied the effects of scaling the TEG leg height and width, and temperature gradient on power density for single crystal Si and SiGe TEGs using 2D and 3D simulations. Temperature dependent material parameters are critical to model TEG performance and have often been neglected. Efficiency and power density were extracted for a range of legs widths (W = 0.1 to 5000 μm), heights (H = 0.5 to 1000 μm), and operating temperatures. TEGs can be designed to have optimum power generation depending upon the desired application by appropriate combinations of temperature difference, W_{LEG}, and H_{LEG}. The efficiency of the μTEGs

increases as the aspect ratio (height/width) increases. For the narrowest widths, the efficiency saturates at aspect ratios ~100-1,000 suggesting that nanowires, which are expected to have lower thermal conductivities than the bulk values used in this work, are viable candidates for future thermoelectric devices.

The role of minority carriers on TEG performance is examined using TEG designs which utilize built-in electric fields to extract generated minority carriers and transport them to a corresponding majority carrier area. A SiGe TEG designed with a number of intrinsic SiGe regions bridging the legs (ladder TEG) were compared to a conventional TEG. The intrinsic regions form a PIN junction from leg to leg with the goal of extracting minority carriers and transporting them to their respective majority carrier leg. Once minority carrier generation becomes significant, the ladder TEG is able to reduce minority carrier density resulting in improved Seebeck effect and increased current and power. Ladder TEG has up to 30-40% efficiency improvements over the conventional TEG with peak efficiencies approaching 2%.

If the width of the ladder TEG legs are decreased, the intrinsic regions are more effective at capturing minority carriers resulting in larger efficiency ratios as widths decrease. However, ladder TEGs lower temperature performance may suffer if the leg widths are scaled down to where the intrinsic regions deplete majority carriers in the legs. Depletion can be mitigated by using PN junctions instead of PIN junctions. PN junction based TEGs exhibit similar minority carrier transport mechanisms as PIN junction based TEGs without the drawback of dopant migration. Overall results show that controlling minority carrier movement can be used to enhance μTEG efficiency.

7 Appendix

7.1 LabView Data Sorting Program

Extracting the maximum power from the current vs. resistance data exported from the Inspect tool in Sentaurus is difficult due to the formatting of the output text file. A LabView program was created to sort the data from the output text file and calculate the maximum power from the sorted current vs. resistance data. The program will output a new text file with the maximum power as a function of T_{TOP}.

Figure 7.1 shows an image of the front panel of the LabView data sorting program. All 25 datasets (corresponding to all of T_{TOP} simulated from 300 K to 1500 K) are extracted from the Inspect tool in Sentaurus into a single text file. The LabView program imports the text file, separates the 25 datasets into individual subsets for each T_{TOP} (based on location in the text file which is consistent for all simulations), and computes the maximum power for each subset. The maximum powers at each T_{TOP} are then recombined into a single array which is outputted in a text file.

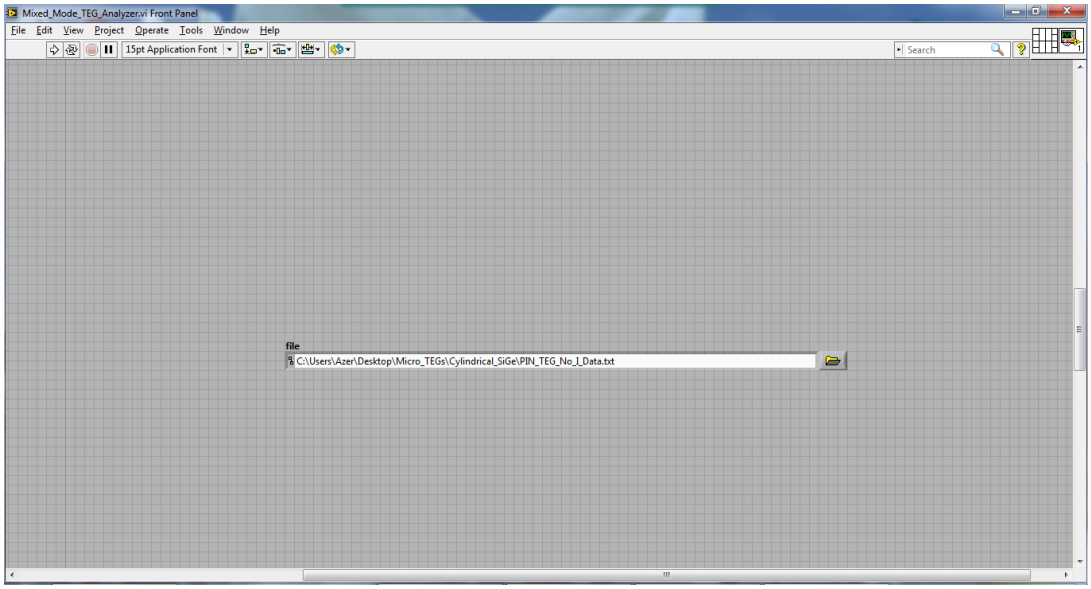

Figure 7.1. Image of data sorting program front panel in LabView

7.2 Sentaurus SDE and SDevice Code

7.2.1 SDE Code – Conventional TEG, 250 nm width

```
;-----------------------------------------------------------------------
; Setting parameters

(define W    @Width@)
(define H    @Height@)

(define DopN "ArsenicActiveConcentration")
(define DopP  "BoronActiveConcentration")

(define PDop  @P_Doping_Concentration@ )   ; [1/cm3]
(define NDop @N_Doping_Concentration@ )    ; [1/cm3]

;-----------------------------------------------------------------------
; Overlap resolution: New replaces Old
(sdegeo:set-default-boolean "ABA")

;-----------------------------------------------------------------------
 ;Creating bottom left metal contact region
(sdegeo:create-rectangle
  (position    0.0  2.0  0.0 )
  (position    0.25 2.5 0.0 )
  "Copper" "R.M1"
)

 ;Creating bottom right metal contact region
(sdegeo:create-rectangle
  (position    0.35  2.0  0.0 )
  (position    0.6  2.5 0.0 )
  "Copper" "R.M2"
)

 ;Creating top metal contact region
(sdegeo:create-rectangle
  (position    0  0.5  0.0 )
  (position    0.6 1 0.0 )
  "Copper" "R.M3"
)

 ;Creating n-type leg region
(sdegeo:create-rectangle
  (position    0  1  0.0 )
  (position    0.25 2 0.0 )
```

```
  "SiliconGermanium" "R.NLeg"
)

 ;Creating p-type leg region
(sdegeo:create-rectangle
  (position    0.35 1  0.0 )
  (position    0.6 2 0.0 )
  "SiliconGermanium" "R.PLeg"
)

;-----------------------------------------------------------------
; Contact declarations
(sdegeo:define-contact-set "Anode"
  4.0  (color:rgb 0.0 1.0 0.0 ) "##")

(sdegeo:define-contact-set "Cathode"
  4.0  (color:rgb 0.0 1.0 0.0 ) "##")

(sdegeo:define-contact-set "Top"
  4.0  (color:rgb 0.0 1.0 0.0 ) "##")

;-----------------------------------------------------------------
; Contact settings
(sdegeo:define-2d-contact
 (find-edge-id (position 0.125 2.5 0.0))
 "Anode")

 (sdegeo:define-2d-contact
 (find-edge-id (position 0.5 2.5 0.0))
 "Cathode")

(sdegeo:define-2d-contact
 (find-edge-id (position 0.5 0.5 0.0))
 "Top")

;-----------------------------------------------------------------
; Saving BND file
(sdeio:save-tdr-bnd (get-body-list) "n@node@_bnd.tdr")

;-----------------------------------------------------------------
; Profiles:
; N Leg
(sdedr:define-constant-profile "Const.NLeg"
 DopN NDop )
(sdedr:define-constant-profile-region  "PlaceCD.NLeg"
 "Const.NLeg" "R.NLeg" )
```

```
; P Leg
(sdedr:define-constant-profile "Const.PLeg"
 DopP PDop )
(sdedr:define-constant-profile-region  "PlaceCD.PLeg"
 "Const.PLeg" "R.PLeg" )

;-----------------------------------------------------------------------
; Meshing Strategy:

; N Leg
(sdedr:define-refinement-size "Ref.NLeg"
   (/ H 200.0)  (/ W 30.0)
  (/ H 200.0)  (/ W 30.0))
;(sdedr:define-refinement-function "Ref.Substrate"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-region "NLeg"
 "Ref.NLeg" "R.NLeg" )

 ; P Leg
(sdedr:define-refinement-size "Ref.PLeg"
  (/ H 200.0)  (/ W 30.0)
  (/ H 200.0)  (/ W 30.0))
;(sdedr:define-refinement-function "Ref.Substrate"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-region "PLeg"
 "Ref.PLeg" "R.PLeg" )

  ; Bottom Left Metal Contact
(sdedr:define-refinement-size "Ref.M1"
  (/ H 15.0)  (/ W 15.0)
  (/ H 15.0)  (/ W 15.0))
;(sdedr:define-refinement-function "Ref.Substrate"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-region "M1"
 "Ref.M1" "R.M1" )

   ; Bottom Right Metal Contact
(sdedr:define-refinement-size "Ref.M2"
  (/ H 15.0)  (/ W 15.0)
  (/ H 15.0)  (/ W 15.0))
;(sdedr:define-refinement-function "Ref.Substrate"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-region "M2"
 "Ref.M2" "R.M2" )
```

```
   ; Top Metal Contact
(sedr:define-refinement-size "Ref.M3"
  (/ H 15.0)  (/ W 15.0)
  (/ H 15.0)  (/ W 15.0))
;(sedr:define-refinement-function "Ref.Substrate"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-region "M3"
 "Ref.M3" "R.M3" )

     ; Mesh Refinement 1
(sedr:define-refinement-window "RWin.Act"
 "Rectangle"
 (position   0.00  0.99   0.0)
 (position   0.25  1.06   0.0))
(sedr:define-refinement-size "Ref.SiAct"
  (/ 1 200.0)  (/ 1 200.0)
  (/ 1 200.0)  (/ 1 200.0))
(sedr:define-refinement-function "Ref.SiAct"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiAct"
 "Ref.SiAct" "RWin.Act" )

   ; Mesh Refinement 2
(sedr:define-refinement-window "RWin.ActX"
 "Rectangle"
 (position   0.35  0.99   0.0)
 (position   0.6  1.06   0.0))
(sedr:define-refinement-size "Ref.SiActX"
  (/ 1 200.0)  (/ 1 200.0)
  (/ 1 200.0)  (/ 1 200.0))
(sedr:define-refinement-function "Ref.SiActX"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX"
 "Ref.SiActX" "RWin.ActX" )

     ; Mesh Refinement 3
(sedr:define-refinement-window "RWin.Act1"
 "Rectangle"
 (position   0.00  1.97   0.0)
 (position   0.25  2.01   0.0))
(sedr:define-refinement-size "Ref.SiAct1"
  (/ 1 200.0)  (/ 1 200.0)
  (/ 1 200.0)  (/ 1 200.0))
(sedr:define-refinement-function "Ref.SiAct1"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiAct1"
```

```
 "Ref.SiAct1" "RWin.Act1" )

   ; Mesh Refinement 4
(sdedr:define-refinement-window "RWin.ActX1"
 "Rectangle"
 (position   0.35  1.97   0.0)
 (position   0.6  2.01   0.0))
(sdedr:define-refinement-size "Ref.SiActX1"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sdedr:define-refinement-function "Ref.SiActX1"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiActX1"
 "Ref.SiActX1" "RWin.ActX1" )

   ;-----------------------------------------------------------------------
; Save CMD file
(sdedr:write-cmd-file "n@node@_msh.cmd")

;-----------------------------------------------------------------------
; Build Mesh
(system:command "snmesh n@node@_msh")
```

7.2.2 SDE Code – Ladder TEG, 250 width

```
;-----------------------------------------------------------------------
; Setting parameters

(define W    @Width@)
(define H    @Height@)

(define DopN "ArsenicActiveConcentration")
(define DopP  "BoronActiveConcentration")

(define PDop  @P_Doping_Concentration@ )   ; [1/cm3]
(define NDop @N_Doping_Concentration@ )    ; [1/cm3]

;-----------------------------------------------------------------------
; Overlap resolution: New replaces Old
(sdegeo:set-default-boolean "ABA")

;-----------------------------------------------------------------------
  ;Creating bottom left metal contact region
(sdegeo:create-rectangle
  (position    0.0  2.0  0.0 )
  (position    0.25 2.5 0.0 )
```

```
  "Copper" "R.M1"
)

 ;Creating bottom right metal contact region
(sdegeo:create-rectangle
  (position    0.35  2.0  0.0 )
  (position    0.6  2.5 0.0 )
  "Copper" "R.M2"
)

 ;Creating top metal contact region
(sdegeo:create-rectangle
  (position    0  0.5  0.0 )
  (position    0.6 1 0.0 )
  "Copper" "R.M3"
)

 ;Creating n-type leg region
(sdegeo:create-rectangle
  (position    0  1  0.0 )
  (position    0.25 2 0.0 )
  "SiliconGermanium" "R.NLeg"
)

 ;Creating p-type leg region
(sdegeo:create-rectangle
  (position    0.35 1  0.0 )
  (position    0.6 2 0.0 )
  "SiliconGermanium" "R.PLeg"
)

 ;Creating intrinsic region 1
(sdegeo:create-rectangle
  (position    0.25 1.05  0.0 )
  (position    0.35 1.15 0.0 )
  "SiliconGermanium" "R.ILeg"
)

 ;Creating intrinsic region 2
(sdegeo:create-rectangle
  (position    0.25 1.2  0.0 )
  (position    0.35 1.3 0.0 )
  "SiliconGermanium" "R.ILeg2"
)

 ;Creating intrinsic region 3
```

```
(sdegeo:create-rectangle
  (position    0.25 1.35  0.0 )
  (position    0.35 1.45 0.0 )
  "SiliconGermanium" "R.ILeg3"
)

 ;Creating intrinsic region 4
(sdegeo:create-rectangle
  (position    0.25 1.5 0.0 )
  (position    0.35 1.6 0.0 )
  "SiliconGermanium" "R.ILeg4"
)

 ;Creating intrinsic region 5
(sdegeo:create-rectangle
  (position    0.25 1.65 0.0 )
  (position    0.35 1.75 0.0 )
  "SiliconGermanium" "R.ILeg5"
)

 ;Creating intrinsic region 6
(sdegeo:create-rectangle
  (position    0.25 1.80 0.0 )
  (position    0.35 1.90 0.0 )
  "SiliconGermanium" "R.ILeg6"
)
;-----------------------------------------------------------------
; Contact declarations
(sdegeo:define-contact-set "Anode"
  4.0  (color:rgb 0.0 1.0 0.0 ) "##")

(sdegeo:define-contact-set "Cathode"
  4.0  (color:rgb 0.0 1.0 0.0 ) "##")

(sdegeo:define-contact-set "Top"
  4.0  (color:rgb 0.0 1.0 0.0 ) "##")

;-----------------------------------------------------------------
; Contact settings
(sdegeo:define-2d-contact
 (find-edge-id (position 0.125 2.5 0.0))
 "Anode")

 (sdegeo:define-2d-contact
 (find-edge-id (position 0.5 2.5 0.0))
 "Cathode")
```

```
(sdegeo:define-2d-contact
 (find-edge-id (position 0.5 0.5 0.0))
 "Top")

;-----------------------------------------------------------------
; Saving BND file
(sdeio:save-tdr-bnd (get-body-list) "n@node@_bnd.tdr")

;-----------------------------------------------------------------
; Profiles:
; - N Leg
(sdedr:define-constant-profile "Const.NLeg"
 DopN NDop )
(sdedr:define-constant-profile-region  "PlaceCD.NLeg"
 "Const.NLeg" "R.NLeg" )

; ; - P Leg
(sdedr:define-constant-profile "Const.PLeg"
 DopP PDop )
(sdedr:define-constant-profile-region  "PlaceCD.PLeg"
 "Const.PLeg" "R.PLeg" )

;-----------------------------------------------------------------
; Meshing Strategy:

; N Leg
(sdedr:define-refinement-size "Ref.NLeg"
   (/ H 200.0)  (/ W 30.0)
  (/ H 200.0)  (/ W 30.0))
;(sdedr:define-refinement-function "Ref.Substrate"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-region "NLeg"
 "Ref.NLeg" "R.NLeg" )

 ; P Leg
(sdedr:define-refinement-size "Ref.PLeg"
  (/ H 200.0)  (/ W 30.0)
  (/ H 200.0)  (/ W 30.0))
;(sdedr:define-refinement-function "Ref.Substrate"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-region "PLeg"
 "Ref.PLeg" "R.PLeg" )

  ; Bottom Left Metal Contact
(sdedr:define-refinement-size "Ref.M1"
```

```
  (/ H 15.0)  (/ W 15.0)
  (/ H 15.0)  (/ W 15.0))
;(sedr:define-refinement-function "Ref.Substrate"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-region "M1"
 "Ref.M1" "R.M1" )

   ; Bottom Right Metal Contact
(sedr:define-refinement-size "Ref.M2"
  (/ H 15.0)  (/ W 15.0)
  (/ H 15.0)  (/ W 15.0))
;(sedr:define-refinement-function "Ref.Substrate"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-region "M2"
 "Ref.M2" "R.M2" )

   ; Top Metal Contact
(sedr:define-refinement-size "Ref.M3"
  (/ H 15.0)  (/ W 15.0)
  (/ H 15.0)  (/ W 15.0))
;(sedr:define-refinement-function "Ref.Substrate"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-region "M3"
 "Ref.M3" "R.M3" )

  ; I Leg 1
(sedr:define-refinement-size "Ref.ILeg"
  (/ H 50.0)  (/ W 30.0)
  (/ H 50.0)  (/ W 30.0))
;(sedr:define-refinement-function "Ref.ILeg"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-region "ILeg"
 "Ref.ILeg" "R.ILeg" )

  ; I Leg 2
(sedr:define-refinement-size "Ref.ILeg2"
  (/ H 50.0)  (/ W 30.0)
  (/ H 50.0)  (/ W 30.0))
;(sedr:define-refinement-function "Ref.ILeg2"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-region "ILeg2"
 "Ref.ILeg2" "R.ILeg2" )

   ; I Leg 3
(sedr:define-refinement-size "Ref.ILeg3"
  (/ H 50.0)  (/ W 30.0)
```

```
  (/ H 50.0)  (/ W 30.0))
;(sdedr:define-refinement-function "Ref.ILeg3"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-region "ILeg3"
 "Ref.ILeg3" "R.ILeg3" )

    ; I Leg 4
(sdedr:define-refinement-size "Ref.ILeg4"
  (/ H 50.0)  (/ W 30.0)
  (/ H 50.0)  (/ W 30.0))
;(sdedr:define-refinement-function "Ref.ILeg4"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-region "ILeg4"
 "Ref.ILeg4" "R.ILeg4" )

     ; I Leg 5
(sdedr:define-refinement-size "Ref.ILeg5"
  (/ H 50.0)  (/ W 30.0)
  (/ H 50.0)  (/ W 30.0))
;(sdedr:define-refinement-function "Ref.ILeg5"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-region "ILeg5"
 "Ref.ILeg5" "R.ILeg5" )

      ; I Leg 6
(sdedr:define-refinement-size "Ref.ILeg6"
  (/ H 50.0)  (/ W 30.0)
  (/ H 50.0)  (/ W 30.0))
;(sdedr:define-refinement-function "Ref.ILeg6"
 ;"DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-region "ILeg6"
 "Ref.ILeg6" "R.ILeg6" )

    ; Mesh Refinement 1
(sdedr:define-refinement-window "RWin.Act"
 "Rectangle"
 (position   0.00  0.99   0.0)
 (position   0.25  1.06   0.0))
(sdedr:define-refinement-size "Ref.SiAct"
  (/ 1 200.0)  (/ 1 200.0)
  (/ 1 200.0)  (/ 1 200.0))
(sdedr:define-refinement-function "Ref.SiAct"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiAct"
 "Ref.SiAct" "RWin.Act" )
```

```
   ; Mesh Refinement 2
(sedr:define-refinement-window "RWin.ActX"
 "Rectangle"
 (position   0.35  0.99   0.0)
 (position   0.6  1.06   0.0))
(sedr:define-refinement-size "Ref.SiActX"
  (/ 1 200.0)  (/ 1 200.0)
  (/ 1 200.0)  (/ 1 200.0))
(sedr:define-refinement-function "Ref.SiActX"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX"
 "Ref.SiActX" "RWin.ActX" )

     ; Mesh Refinement 3
(sedr:define-refinement-window "RWin.Act1"
 "Rectangle"
 (position   0.00  1.97   0.0)
 (position   0.25  2.01   0.0))
(sedr:define-refinement-size "Ref.SiAct1"
  (/ 1 200.0)  (/ 1 200.0)
  (/ 1 200.0)  (/ 1 200.0))
(sedr:define-refinement-function "Ref.SiAct1"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiAct1"
 "Ref.SiAct1" "RWin.Act1" )

   ; Mesh Refinement 4
(sedr:define-refinement-window "RWin.ActX1"
 "Rectangle"
 (position   0.35  1.97   0.0)
 (position   0.6  2.01   0.0))
(sedr:define-refinement-size "Ref.SiActX1"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sedr:define-refinement-function "Ref.SiActX1"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX1"
 "Ref.SiActX1" "RWin.ActX1" )


    ; Mesh Refinement 5
(sedr:define-refinement-window "RWin.ActX2"
 "Rectangle"
 (position   0.23  1.05   0.0)
 (position   0.27  1.15   0.0))
(sedr:define-refinement-size "Ref.SiActX2"
```

```
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sdedr:define-refinement-function "Ref.SiActX2"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiActX2"
 "Ref.SiActX2" "RWin.ActX2" )

    ; Mesh Refinement 6
(sdedr:define-refinement-window "RWin.ActX3"
 "Rectangle"
 (position   0.33  1.05   0.0)
 (position   0.36  1.15   0.0))
(sdedr:define-refinement-size "Ref.SiActX3"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sdedr:define-refinement-function "Ref.SiActX3"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiActX3"
 "Ref.SiActX3" "RWin.ActX3" )

     ; Mesh Refinement 7
(sdedr:define-refinement-window "RWin.ActX4"
 "Rectangle"
 (position   0.23  1.20   0.0)
 (position   0.27  1.30   0.0))
(sdedr:define-refinement-size "Ref.SiActX4"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sdedr:define-refinement-function "Ref.SiActX4"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiActX4"
 "Ref.SiActX4" "RWin.ActX4" )

    ; Mesh Refinement 8
(sdedr:define-refinement-window "RWin.ActX5"
 "Rectangle"
 (position   0.33  1.20   0.0)
 (position   0.36  1.30   0.0))
(sdedr:define-refinement-size "Ref.SiActX5"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sdedr:define-refinement-function "Ref.SiActX5"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiActX5"
 "Ref.SiActX5" "RWin.ActX5" )
```

```
     ; Mesh Refinement 9
(sedr:define-refinement-window "RWin.ActX6"
 "Rectangle"
 (position   0.23  1.35   0.0)
 (position   0.27  1.45   0.0))
(sedr:define-refinement-size "Ref.SiActX6"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sedr:define-refinement-function "Ref.SiActX6"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX6"
 "Ref.SiActX6" "RWin.ActX6" )

    ; Mesh Refinement 10
(sedr:define-refinement-window "RWin.ActX7"
 "Rectangle"
 (position   0.33  1.35   0.0)
 (position   0.36  1.45   0.0))
(sedr:define-refinement-size "Ref.SiActX7"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sedr:define-refinement-function "Ref.SiActX7"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX7"
 "Ref.SiActX7" "RWin.ActX7" )

      ; Mesh Refinement 11
(sedr:define-refinement-window "RWin.ActX8"
 "Rectangle"
 (position   0.23  1.5   0.0)
 (position   0.27  1.6   0.0))
(sedr:define-refinement-size "Ref.SiActX8"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sedr:define-refinement-function "Ref.SiActX8"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX8"
 "Ref.SiActX8" "RWin.ActX8" )

    ; Mesh Refinement 12
(sedr:define-refinement-window "RWin.ActX9"
 "Rectangle"
 (position   0.33  1.5   0.0)
 (position   0.36  1.6   0.0))
(sedr:define-refinement-size "Ref.SiActX9"
  (/ 1 100.0)  (/ 1 100.0)
```

```
  (/ 1 100.0)  (/ 1 100.0))
(sedr:define-refinement-function "Ref.SiActX9"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX9"
 "Ref.SiActX9" "RWin.ActX9" )

    ; Mesh Refinement 13
(sedr:define-refinement-window "RWin.ActX10"
 "Rectangle"
 (position   0.23  1.65   0.0)
 (position   0.26  1.75   0.0))
(sedr:define-refinement-size "Ref.SiActX10"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sedr:define-refinement-function "Ref.SiActX10"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX10"
 "Ref.SiActX10" "RWin.ActX10" )

    ; Mesh Refinement 14
(sedr:define-refinement-window "RWin.ActX11"
 "Rectangle"
 (position   0.33  1.65   0.0)
 (position   0.36  1.75   0.0))
(sedr:define-refinement-size "Ref.SiActX11"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sedr:define-refinement-function "Ref.SiActX11"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX11"
 "Ref.SiActX11" "RWin.ActX11" )

     ; Mesh Refinement 15
(sedr:define-refinement-window "RWin.ActX12"
 "Rectangle"
 (position   0.23  1.80   0.0)
 (position   0.26  1.90   0.0))
(sedr:define-refinement-size "Ref.SiActX12"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sedr:define-refinement-function "Ref.SiActX12"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX12"
 "Ref.SiActX12" "RWin.ActX12" )

    ; Mesh Refinement 16
```

```
(sedr:define-refinement-window "RWin.ActX13"
 "Rectangle"
 (position   0.33  1.80   0.0)
 (position   0.36  1.90   0.0))
(sedr:define-refinement-size "Ref.SiActX13"
  (/ 1 100.0)  (/ 1 100.0)
  (/ 1 100.0)  (/ 1 100.0))
(sedr:define-refinement-function "Ref.SiActX13"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RefPlace.SiActX13"
 "Ref.SiActX13" "RWin.ActX13" )


   ;-----------------------------------------------------------------------
; Save CMD file
(sedr:write-cmd-file "n@node@_msh.cmd")

;-----------------------------------------------------------------------
; Build Mesh
(system:command "snmesh n@node@_msh")
```

7.2.3 SDevice Code

```
!(
set DG
"eQuantumPotential"
set EQN0
"Poisson eQuantumPotential hQuantumPotential Temperature"
set EQNS
"Poisson eQuantumPotential hQuantumPotential Electron Hole Temperature"
)!

Device "TEG" {

File {
   * input files:
   Grid=   "@tdr@"
   Parameter="@parameter@"
   * output files:
   Plot=   "@tdrdat@"
   Current="@plot@"
}

Electrode {
   { Name="Anode"    Voltage= 0.0 }
   { Name="Cathode"  Voltage= 0.0 }
```

```
}

Thermode {
  { Name="Top"      Temperature=300 SurfaceResistance = 0.00001}
  { Name="Anode"   Temperature=300 SurfaceResistance = 0.00001}
  { Name="Cathode"   Temperature=300 SurfaceResistance = 0.00001}
}

Physics{
  Thermodynamic
  EffectiveIntrinsicDensity( OldSlotboom )
  AnalyticTEP
}

Physics(Material="SiliconGermanium"){
  MoleFraction(xFraction=0.3)
  eQuantumPotential
  hQuantumPotential
  Mobility(
    PhuMob
   HighFieldSaturation
    Enormal
  )
  Recombination(
    SRH(DopingDependence ExpTempDependence ElectricField (Lifetime = Schenk
DensityCorrection = Local))
    Band2Band(Model=NonlocalPath)
    Auger(WithGeneration)
  )
}

}

File {
  Output= "@log@"
}

Insert= "PlotSection_des.cmd"

System {

Thermal (Ta Tb)
Set (Tb = 300)
Initialize (Ta = 300)

 "TEG" TEG ("Anode" = out "Cathode" = 0,"Top" = Ta "Cathode" = Tb "Anode" = Tb)
```

```
  Resistor_pset rload (out 0 ) {resistance = 0.1}

  Plot "n@node@_sys_des.plt" (i(TEG, out) p(rload, "resistance"))

}

Insert= "MathSection_des.cmd"

Solve {
*- Creating initial guess:
   Coupled(Iterations= 100 LineSearchDamping= 1e-4){ Poisson !(puts $DG)! }
   Coupled { !(puts $EQN0)! }
   Coupled { !(puts $EQNS)! }

        Quasistationary(
     InitialStep= 1e-2 Increment= 1.35
     MinStep= 1e-5 MaxStep= 0.02
     Goal { Node=Ta Value=@Temp@}
   )
     { Coupled { !(puts $EQNS)! }}

*- Vg sweep
   NewCurrentFile="IdVg_"
   Quasistationary(
     DoZero
     InitialStep= 1e-3 Increment= 1.5
     MinStep= 1e-5 MaxStep= 0.02
     Goal { Parameter = rload."resistance" Value=@rload@ }
   ){ Coupled { !(puts $EQNS)! }
     CurrentPlot( Time=(Range=(0 1) Intervals= 200)  )
   }
}
```

7.3 Sentaurus Models

7.3.1 Thermodynamic Current Density Model

The thermodynamic model utilizes a modified drift-diffusion model to compute electron and hole current density. The generalized drift-diffusion model defines electron and hole current density as[83]:

$$\overrightarrow{J_n} = \mu_n\left(\mathrm{n}\nabla \mathrm{E}_C - 1.5nk\nabla T ln(m_n)\right) + D_n\left(\nabla n - nln(\gamma_n)\right)$$

$$\overrightarrow{J_p} = \mu_p\left(\mathrm{p}\nabla \mathrm{E}_V + 1.5pk\nabla T ln\left(m_p\right)\right) + D_p\left(\nabla p - pln\left(\gamma_p\right)\right)$$

where μ_p and μ_n are hole and electron mobility, n and p are electron and hole density, E_C and E_V are the conduction and valence band edges, k is the Boltzmann constant, m_n and m_p are electron and hole mass, T is temperature, and D_n and D_p are the electron and hole diffusivities. γp and γp are equal to 1 for Boltzmann statistics but for Fermi statistics they are equal to:

$$\gamma_n = \frac{n}{N_C}e^{-\left(\frac{E_{FN}-E_C}{kT}\right)}, \gamma_p = \frac{p}{N_V}e^{-\left(\frac{E_V-E_{FP}}{kT}\right)}$$

where N_C and N_V are electron and hole density of states, and E_{FN} and E_{FP} are the electron and hole quasi fermi levels. Sentaurus assumes that electron and hole diffusivities are defined by the Einstein relation:

$$D_n = kT\mu_n,\ D_p = kT\mu_p$$

and given this the electron and hole current density equations can be simplified to:

$$\overrightarrow{J_n} = -nq\mu_n\nabla\varphi_n,\ \overrightarrow{J_p} = -pq\mu_p\nabla\varphi_p$$

where φ_n and φ_p are the electron and hole quasi fermi potentials and q is electron charge.

The quasi fermi potentials account for both the drift and diffusion components and are computed from the electron and hole density:

$$\varphi_n = \frac{ln\left(\frac{n}{N_C}\right)kT + E_C}{-q}, \varphi_p = \frac{-ln\left(\frac{p}{N_V}\right)kT + E_V}{-q}$$

The thermodynamic model expands the electron and hole current densities to include a thermoelectric current term:

$$\overrightarrow{J_n} = -nq\mu_n(\nabla\varphi_n + P_n\nabla T), \quad \overrightarrow{J_p} = -nq\mu_p\left(\nabla\varphi_p + P_p\nabla T\right)$$

where P_n and P_p are electron and hole thermoelectric powers (Seebeck coefficients). Sentaurus can calculate P_n and P_p using two different methods. The default method uses experimental data (Figure 7.2) measured for silicon from 250 to 500 K with doping concentrations from 1 x 10^{14} to 1 x 10^{19} cm^{-3}.

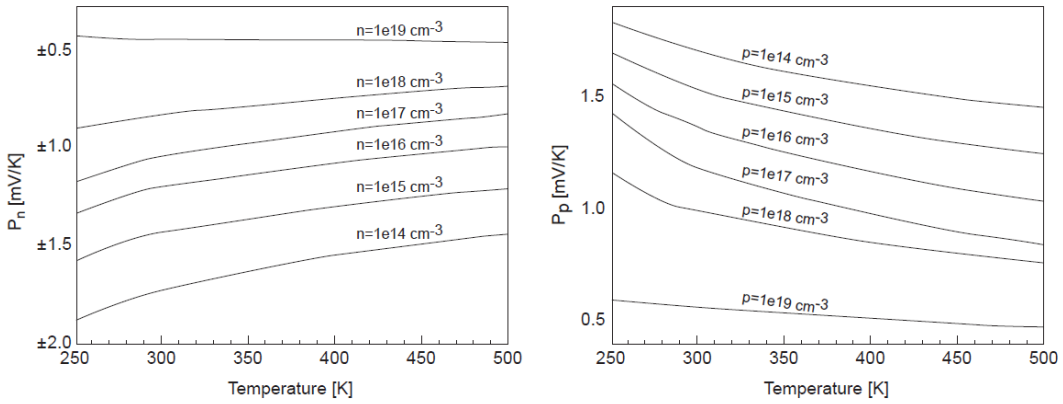

Figure 7.2 Experimental thermoelectric powers (Pn and Pp)

Outside of this temperature range, P_n and P_p are linearly extrapolated as temperature increases. This method is not viable for high temperature simulations as experimental observations show that P_n and P_p decrease faster at higher temperatures. The alternative

method uses an analytic function which is dependent upon density of states and carrier concentration and is valid for non-degenerate semiconductors:

$$P_P = \frac{k}{q}\left[\frac{3}{2} + ln\left(\frac{N_V}{p}\right)\right], P_N = -\frac{k}{q}\left[\frac{3}{2} + ln\left(\frac{N_C}{n}\right)\right]$$

Figure 7.3 shows Seebeck coefficients extracted from Sentaurus simulations using the analytical P_n and P_p model as a function of temperature and doping concentration. At higher temperatures the Seebeck coefficient decreases as the material becomes more intrinsic and the minority carrier Seebeck contribution offsets the majority carriers. For these simulations the analytical method was used to compute P_n and P_p as temperatures will range from 300 K to the melting temperature.

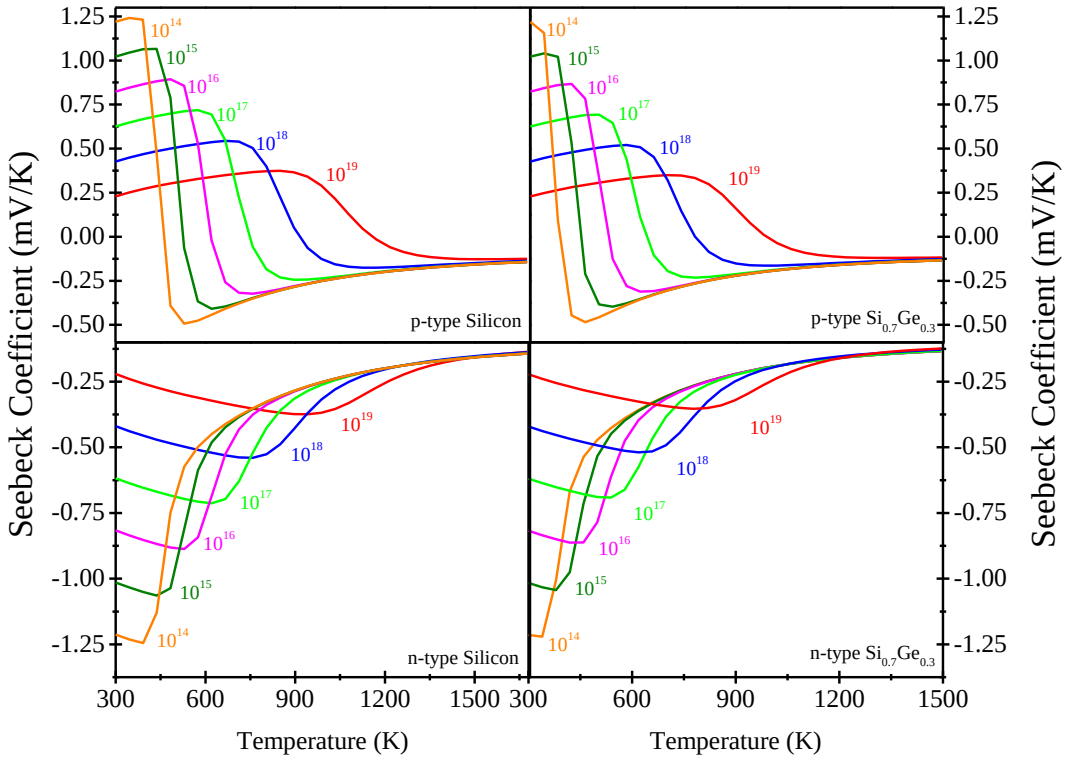

Figure 7.3 Seebeck coefficients extracted from Sentaurus simulations using analytical P_n and P_p model.

7.3.2 Thermodynamic Heat Equation

The thermodynamic model uses a Fourier heat equation to solve for the lattice temperature:

$$\frac{\delta}{\delta_t}C_p - \nabla \cdot \kappa \nabla T = -\nabla \cdot \left[(P_n T + \phi_n)\overrightarrow{J_n} + (P_p T + \phi_p)\overrightarrow{J_p}\right] - \left(E_C + \frac{3}{2}kT\right)\nabla \cdot \overrightarrow{J_n} - \left(E_v - \frac{3}{2}kT\right)\nabla \cdot \overrightarrow{J_p} + qR_{net}(E_C - E_V + 3kT)$$

where C_p is lattice heat capacity, k is thermal conductivity, and R_{net} is the net recombination/generation rate.

The left side of this equation describes the total heat flux in the system,

$$\frac{\delta}{\delta_t}C_p - \nabla \cdot \kappa \nabla T$$

C_p is defined by the following function:

$$C_p = A + BT + CT^2 + DT^3$$

where A, B, C, and D are coefficients. The default model for Silicon is temperature dependent (non-zero B, C, and D) but for other materials only the A coefficient is defined. Thermal conductivity is a lumped phonon/electronic thermal conductivity model which has a temperature dependent function with the following form:

$$\kappa = \frac{1}{a + bT + cT^2}$$

where a, b, and c are coefficients. Figure 7.4 shows examples of heat capacity and thermal conductivity for silicon and $Si_{0.7}Ge_{0.3}$. Silicon C_p and κ are temperature dependent and are based on measurements done on pure silicon samples. Silicon

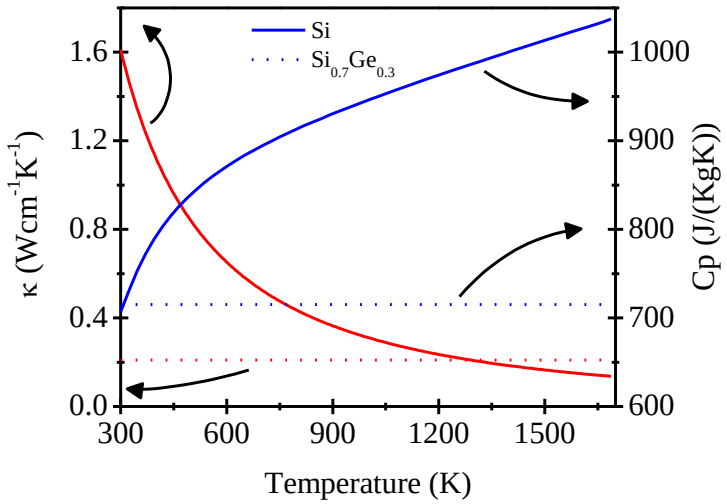

Figure 7.4 Thermal conductivity and lattice heat capacity for $Si_{0.7}Ge_{0.3}$ and Silicon as a function of temperature.

Germanium κ and C_p are mole fraction dependent and based on measurements but constant values are assumed (no temperature dependence).

The right side of the thermodynamic heat equation accounts for all of the sources of heat in the system. The first term,

$$-\nabla \cdot \left[(P_n T + \phi_n)\overrightarrow{J_n} + (P_p T + \phi_p)\overrightarrow{J_p}\right]$$

describes the contributions from Joule and Thermoelectric (Thomson, and Peltier) heating. Joule heating from electrons and holes is proportional to the current density and irrespective of current direction,

$$H_{JOULE} = \frac{\left|\overrightarrow{J_n}\right|^2}{qn\mu_n} + \frac{\left|\overrightarrow{J_p}\right|^2}{qp\mu_p}$$

Joule heating arises when electrons and holes are accelerated by an electric field, collide with the semiconductor lattice, and release kinetic energy to the lattice (phonons). This kinetic energy is observed as an increase in the lattice temperature. Electron and hole joule

heat are positive and sum together. The Thermoelectric heat component is comprised of two different components, Thomson and Peltier Heat,

$$H_{THERMOELECTRIC} = -\overrightarrow{J_n} \cdot T\nabla P_n - \overrightarrow{J_p} \cdot T\nabla P_n$$

Thomson heat occurs when a current is passed through a spatial gradient of Seebeck coefficient (often as a result of a temperature gradient) resulting in an exchange of energy between the lattice and charge carriers. Peltier heat is the result of current passing through the interface of two materials that have different Seebeck coefficients where carriers transfer heat from one material to the other. The magnitude of Peltier heating is proportional to the current density though the interface and the difference in Seebeck coefficients and temperature at the interface of the two materials,

$$Q = (\pi_1 - \pi_2) \cdot J$$

where π_1 and π_2 are the Peltier coefficients for the two respective materials. The Peltier coefficients are defined as,

$$\pi_1 = S_1 \cdot T_1, \pi_2 = S_2 \cdot T_2$$

S_1, S_2, T_1 and T_2 are Seebeck coefficients and temperature for each respective material. Extracting the Peltier Heat from the Thermoelectric heat equation yields,

$$H_{PELTIER} = -T\left(\frac{\delta P_n}{\delta n}\overrightarrow{J_n} \cdot \nabla \mathrm{n} + \frac{\delta P_p}{\delta p}\overrightarrow{J_p} \cdot \nabla \mathrm{p}\right)$$

The second and third terms of the thermodynamic heat equation calculates the electronic-convective heat

$$\left(E_C + \frac{3}{2}kT\right)\nabla \cdot \overrightarrow{J_n} - \left(E_v - \frac{3}{2}kT\right)\nabla \cdot \overrightarrow{J_p}$$

Electronic convective heat describes the energy transfer between carriers and the lattice as carriers move through a temperature profile.

The last term of the thermodynamic equation describes the heat generated or absorbed due to recombination and generation of electrons and holes,

$$qR_{net}(E_C - E_V + 3kT)$$

This process results in an energy transfer between electron-hole pairs and the lattice where energy is added to the system by recombination and subtracted by generation. Sentaurus computes this energy transfer using the following formula,

$$H_{REC} = qR_{net}\left(\phi_p - \phi_n + T(P_p - P_n)\right)$$

The thermal energy from recombination process is very critical for TEG simulations at high temperatures where minority carrier generation is significant and subsequently there is considerable recombination.

7.3.3 Intrinsic Carrier Concentration and Band Gap Models

The intrinsic carrier concentration is a temperature dependent function that is determined by the electron and hole density of states and the band gap. It is defined as:

$$n_i(T) = \sqrt{N_c(T) \cdot N_V(T)} \cdot e^{\frac{-E_G(T)}{2kT}}$$

where the $N_c(T)$ and $N_v(T)$ are the electron and hole density of states, $E_G(T)$ is the band gap, k is the Boltzmann constant and T is temperature. The electron and hole density of states and the band gap are temperature dependent and are written as:

$$N_C(T) = N_C(300\ K) \cdot \left(\frac{m_n(T)}{m_o}\right)^{\frac{3}{2}} \cdot \left(\frac{T}{300\ K}\right)^{\frac{3}{2}}$$

$$N_V(T) = N_V(300\ K) \cdot \left(\frac{m_p(T)}{m_o}\right)^{\frac{3}{2}} \cdot \left(\frac{T}{300\ K}\right)^{\frac{3}{2}}$$

$$E_G(T) = E_G(0) + \Delta E_G(N_{D,}N_A) - \frac{\alpha T^2}{T + \beta}$$

where m_o is the free electron mass, $m_n(T)$ is the effective electron mass, $m_p(T)$ is the effective hole mass, $\Delta E_G(N_D, N_A)$ is the doping induced bandgap narrowing, $E_G(0)$ is the bandgap at 0 K, and α and β are numerical parameters that describe the temperature dependent band gap narrowing. The effective electron and hole mass are defined as:

$$M_n(T) = 6^{\frac{2}{3}} \cdot \left(\frac{\left(m_o \cdot \gamma \frac{E_G(0)}{E_G(T)} \right)^2}{m_l} \right)^{\frac{1}{3}}$$

$$M_p(T) = \left(\frac{a + bT + cT^2 + dT^3 + eT^4}{1 + fT + gT^2 + hT^3 + iT^4} \right)^{\frac{2}{3}}$$

where a,b,c,d,e,f,g,h,i and γ are coefficients, and m_l is a numerical parameter.

These models are well calibrated for lower temperatures but at higher temperatures they underestimate the electron and hole density and overestimate the band gap. Figure 7.5 shows band gap and intrinsic carrier concentration for Silicon and Silicon Germanium (x = 0.3) as a function of temperature which are extracted from Sentaurus 2D simulations. The maximum temperature shown in each graph is the melting temperatures (T = 1687 K

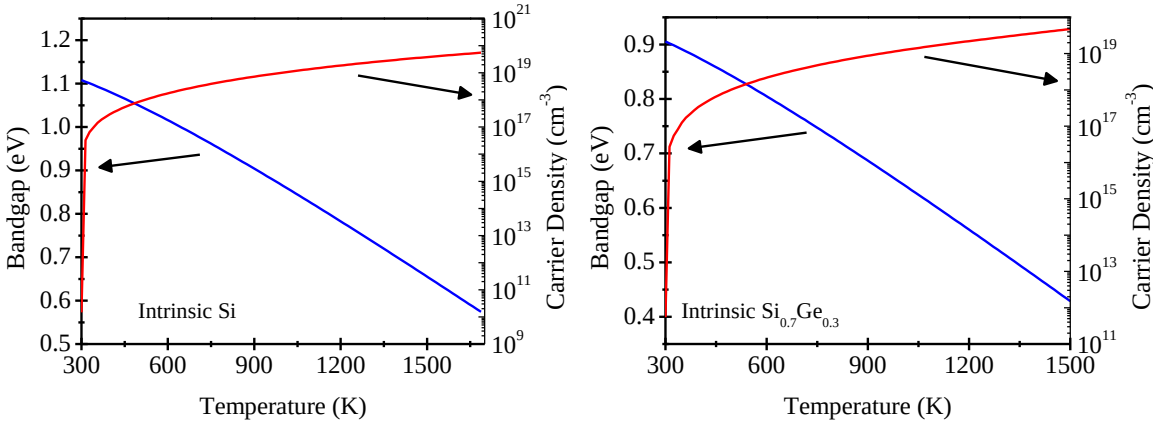

Figure 7.5 Band gap and intrinsic carrier concentration as a function of temperature for Silicon (a) and $Si_{0.7}Ge_{0.3}$ (b)

for Si, and T = 1485 K for $Si_{0.7}Ge_{0.3}$) for the corresponding material. At melting peak carrier concentration is around approximately 1 x 10^{20} cm^{-3}, much lower than expected.

For TEG simulations at high temperatures where significant carrier generation is expected, output power will be inaccurately calculated as minority carrier generation/recombination rates, thermoelectric effects (Seebeck, Peltier, and Thomson), and current density are underestimated. Given the limitations of the standard Sentaurus models, we have developed an approach to approximate semiconductor behavior at high temperatures.

7.3.4 Density Gradient Approximation

A quantum correction model is included in these simulations that adjusts the electron and hole densities when device dimensions approach quantum mechanical length scales. This is achieved by adding a potential Λ_n and Λ_p to the electron and hole density equations,

$$n = N_C F_{1/2}\left(\frac{E_{Fn}-E_C-\Lambda_n}{kT}\right),\ p = N_V F_{1/2}\left(\frac{\Lambda_p-E_V-E_{Fp}}{kT}\right)$$

where $F_{1/2}$ is the Fermi function. Λ_n is defined as,

$$\Lambda_n = -\frac{\hbar^2\gamma}{12m_n}\left[\nabla\cdot\alpha(\zeta\nabla\beta E_{Fn}-\nabla\beta\bar{\phi})+\frac{1}{2}(\zeta\nabla\beta E_{Fn}-\nabla\beta\bar{\phi})\cdot\alpha(\zeta\nabla\beta E_{Fn}-\nabla\beta\bar{\phi})\right]$$

where ħ is the reduced Planck's constant, $\beta = \frac{1}{kT}$, $\bar{\phi} = E_C + kTln\left(\frac{N_C}{N_{REF}}\right) + \Lambda_n$ α is a symmetric matrix and ζ is a coefficient. For holes, Λ_p is an analogous function.

7.3.5 Recombination Models

The net recombination/generation rate is determined by three different types of recombination mechanism; Shockley-Read-Hall (SRH), Auger, and Band to Band Recombination,

$$R_{NET} = R_{SRH} + R_{AUGER} + R_{BANDTOBAND}$$

The carrier lifetimes τ_p and τ_n determine the average time it takes for a carrier to recombine and are calculated from the three different recombination mechanisms,

$$\frac{1}{\tau_{p,n}} = \frac{1}{\tau_{pSRH,nSRH}} + \frac{1}{\tau_{pAUGER,nAUGER}} + \frac{1}{\tau_{pB2B,nB2B}}$$

where τ_{pSRH} and τ_{nSRH} are the SRH recombination lifetimes, τ_{pAUGER} and τ_{nAUGER} are the Auger recombination lifetimes, and τ_{pB2B} and τ_{nB2B} are the band to band recombination lifetimes (n and p denoting electrons and holes respectively).

SRH recombination (also sometimes referred to as trap-assisted recombination) results when an electron and hole recombine at an energy level (known as a trap) within the band gap. Traps occur due to structural defects in the lattice or from impurities (via doping). SRH recombination is defined as

$$R_{SRH} = \frac{np - {n_i}^2}{\tau_{pSRH}(n + n_1) + \tau_{nSRH}(p + p_1)}$$

where n_1 and p_1 are defined as,

$$n_1 = n_i e^{\left(\frac{E_{TRAP}}{kT}\right)}, p_1 = n_i e^{\left(\frac{-E_{TRAP}}{kT}\right)}$$

E_{TRAP} is the energy difference between the defect level and intrinsic level. In the case of SRH, τ_{pSRH} and τ_{nSRH} are doping and temperature dependent with the following form,

$$\tau_{pSRH,nSRH} = \tau_{dop} \frac{f(T)}{1 + g_c}$$

where τ_{dop} is the carrier lifetime doping dependence, $f(T)$ is the carrier lifetime temperature dependence, and g_c is a parameter. As doping concentration increases, the minority carrier lifetimes significantly decrease and this behavior is modeled by τ_{dop}

$$\tau_{dop} = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_A + N_D}{N_{ref}}\right)^{\gamma}}$$

where τ_{min} and τ_{max} are the minimum and maximum carrier lifetimes, N_{REF} and γ are fitting parameters. An exponential temperature dependence is used to describe increasing carrier lifetimes with increasing temperature,

$$f(T) = e^{C\left(\frac{T}{300K} - 1\right)}$$

where C is a parameter.

Auger recombination occurs when the energy from an electron-hole recombination is given to a third particle (hole or electron) which excites the particle to a higher energy state. The excited particle eventually falls back down to the band edge after giving its energy back to the lattice through collisions. Auger recombination is generally observed when carrier density is sufficiently large enough that the probability of carrier-carrier energy exchange is significant. The rate of Auger recombination is defined as,

$$R_{Auger} = (C_n(T)n + C_P(T)p)(np - {n_i}^2)$$

where C_n and C_p are the Auger coefficients. C_n and C_p are temperature and injection level dependent and are written as,

$$C_n = \left(A_n + B_n\left(\frac{T}{T_0}\right) + C_n\left(\frac{T}{T_0}\right)^2\right)\left[1 + H_n e^{\left(-\frac{n}{N_O}\right)}\right], \quad C_p = \left(A_p + B_p\left(\frac{T}{T_0}\right) + C_p\left(\frac{T}{T_0}\right)^2\right)\left[1 + H_p e^{\left(-\frac{p}{P_O}\right)}\right]$$

where T_0 is 300 K, A_n, B_n, C_n, A_p, B_p, C_p, H_n and H_p are coefficients. Extracting the Auger carrier lifetimes from the Auger recombination rate yields,

$$\tau_{pAUGER} = \frac{1}{C_p p^2 + C_n np}, \quad \tau_{nAUGER} = \frac{1}{C_n n^2 + C_p np}$$

A band to band recombination-generation model is included to describe band to band tunneling effects which is modelled as a generation or recombination process. When the electric field is small, band to band tunneling is negligible. However, when steep PN junctions are formed with sufficiently highly doped regions band to band tunneling can be significant. The band to band model is written as

$$R_{B2B} = A * \left(\frac{np - {n_i}^2}{(n + n_i) + (p + n_i)}\right) * \left(\frac{F}{1V/cm}\right)^P e^{-\frac{BE_G(T)^{\frac{3}{2}}}{E_G(300\,K)^{\frac{3}{2}} * F}}$$

where A, B and P are coefficients, and F is electric field.

7.3.6 Mobility Model

A Phillips Unified mobility model is used in these simulations to take into account the temperature dependent electron and hole mobility as well as mobility degradation from impurity scattering and carrier to carrier scattering. The effective carrier mobility is split into two components,

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_L} + \frac{1}{\mu_D}$$

where μ_L is the temperature dependent component (phonon scattering) and μ_D is the impurity and carrier -carrier scattering component. The phonon scattering component μ_L decreases carrier mobility with increasing temperature and is defined for electrons (μ_{Ln}) and holes (μ_{Lp}) as,

$$\mu_{Ln} = \mu_{n,max}\left(\frac{T}{300\,K}\right)^{-\theta n}, \mu_{Lp} = \mu_{p,max}\left(\frac{T}{300\,K}\right)^{-\theta p}$$

where θn and θp are coefficients and $\mu_{n,max}$ and $\mu_{p,max}$ are the room temperature intrinsic electron and hole mobilities. The impurity and carrier-carrier scattering component μ_D

captures the reduction in mobility due to doping concentration providing a model for acceptor and donor scattering as well as electron-hole scattering effects. In the case of electrons, μ_D is written as,

$$\mu_{Dn} = \mu_{n,N}(T)\left(\frac{N_{n,sc}}{N_{n,eff}}\right)\left(\frac{N_{n,ref}}{N_{n,sc}}\right)^{\alpha_n} + \mu_{n,c}\left(\frac{n+p}{N_{n,eff}}\right)$$

where $\mu_{n,N}$ and $\mu_{n,c}$ are the temperature dependent terms, α_n is a coefficient, $N_{n,sc}$ and $N_{n,eff}$ are the doping dependent terms. The temperature dependence of impurity scattering is proportional to $T^{\frac{3}{2}}$ and the total amount of ionized impurities. $\mu_{n,N}$ and $\mu_{n,c}$ are defined as,

$$\mu_{n,N}(T) = \frac{{\mu_{n,max}}^2}{\mu_{n,max} - \mu_{n,min}}\left(\frac{T}{300\ K}\right)^{3\alpha_n - 1.5}, \qquad \mu_{n,c}(T) = \frac{\mu_{n,max} \cdot \mu_{n,min}}{\mu_{n,max} - \mu_{n,min}}\left(\frac{300K}{T}\right)^{0.5}$$

The doping dependent terms $N_{n,sc}$ and $N_{n,eff}$ are defined as

$$N_{n,sc} = N_D + N_A + p,\ N_{n,eff} = N_D + G(P_n)N_A + f_e\frac{p}{F(P_n)}$$

where $G(P_n)$ and $F(P_n)$ describe the minority impurity and electron-hole scattering respectively. An analogous approach to impurity and carrier-carrier scattering is taken for holes.

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