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Narrow Channel Accumulated Body MOSFETs: Design, Modeling and Experimental Verification

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University of Connecticut, 2015

Current leakage on a planar field effect transistor (FET) channel's side surfaces is more significant as the channel width decreases. Traps and positive fixed charges at the interface of Silicon and the isolation dielectric (STI) are mainly responsible for this. An accumulated body approach introduces a side-gate structure surrounding the body of the transistor, which can be used to accumulate the body in narrow structures to suppress the leakage. A separately controlled top gate is used for transistor action.

In this work, the fabrication process and electrical behavior of short and narrow-channel (10 nm scale) bulk Si accumulated body MOSFETs are analyzed through three-dimensional numerical studies. Results are verified experimentally with devices fabricated at IBM Watson Research Labs using conventional CMOS processes.

Simulation results show suppression of leakage currents by 10^6 times for no side-interface charges and by 10^{10} times for an interface positive fixed charge density of 10^{12} cm^{-2}. The threshold voltage (V_T) can be dynamically controlled by the side-gate through accumulation of the body. For simulated structures of W x L = 10 nm x 15 nm, V_T shift per a negative volt of side-gate bias ($\Delta V_T/\Delta V_{side}$) is more than 0.3 V/V. For experimental devices of effective W x L = 15 x 27 nm, $\Delta V_T/\Delta V_{side}$ ratio is more than 1 V/V. Reliable high temperature (> 600 K) operation and improvement in subthreshold

slope and drain induced barrier lowering is also shown in simulations and in experimental structures.

Various steady-state and AC analyses are also conducted to characterize the effect of the side-gate and its relation to other terminals. One such relationship exists between the side-gate and the substrate, where the capacitive coupling of the side-gate enhances the depletion effect of substrate biasing. It is shown through simulations, and verified through experiments, that although the mechanisms of V_T control by the side-gate and substrate biasing are different, they enhance the effect of each other.

Furthermore, the effect of line edge roughness on active area of the MOSFET is analyzed through numerical analysis and it is shown that the side-gate of an accumulated body MOSFET helps direct the current towards the center of the channel.

Narrow Channel Accumulated Body MOSFETs:

Design, Modeling and Experimental Verification

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Narrow Channel Accumulated Body MOSFETs:

Design, Modeling and Experimental Verification

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My parents, Adviye and Ziyaeddin, with their unending love, courage and endurance, have led me to have an excellent education, and better yet, led me to become the man I am. I will be eternally grateful to them. My siblings and their families have been great support as well, by sharing their PhD experiences and love with me. My sister Zeynep, who lived in New York City for about a year with her family, has been always welcoming in my overnight trips to IBM. My brother, who moved to Boston with his family during my studies, provided a warm second home for me.

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presence, has been a safe haven within worldly troubles. Also throughout years, many have shown me their sincere brotherly love and although space would not permit to list them, I will be eternally grateful for their companionship.

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1 Introduction

Accumulated body MOSFETs incorporate a side-gate structure that surrounds the body of a planar bulk MOSFET like a guard ring to provide electrostatic control of the body (Figure 1.1). Being independent from the transistor gate, the side-gate can be biased to accumulate the FET body to achieve an electrostatic doping effect. Initial experiments with SiN-based shallow trench isolation (STI) [1] showed reduced leakage currents and improved subthreshold characteristics, and that the threshold voltage (V_T) of narrow channel accumulated body FETs can be dynamically controlled by the side-gate voltage (V_{side}) in a wide range [1, 2].

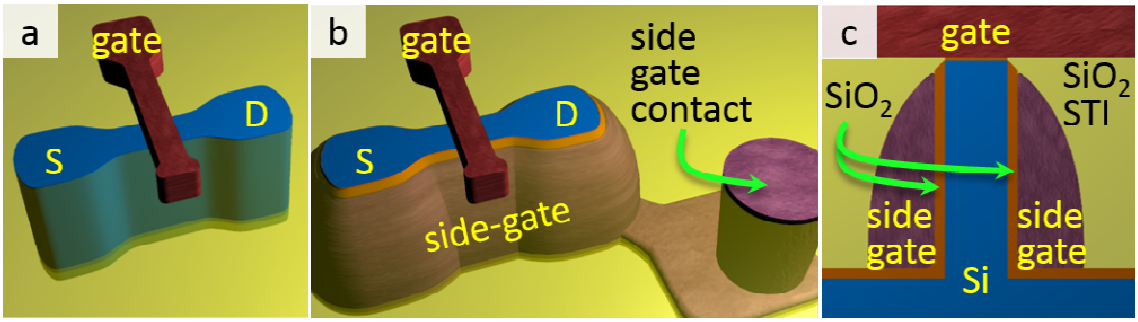


Figure 1.1. Conceptual drawings of (a) conventional bulk Si narrow channel MOSFET with STI, (b) an accumulated body MOSFET with polysilicon side-gate and the side-gate contact via from the top of STI, (c) cross-section along the channel width of an accumulated body MOSFET.

In narrow channel devices, observed V_T control and reduced short channel effects have been attributed to accumulation of the whole body [2]. However, a 3D model of accumulated body FETs has been missing to explain how the side-gate and the channel interact and how the planar nature of the channel is impacted. Computational part of this

dissertation, at 10-nm regime, highlights the significant increase in source barrier height by accumulation of the body of narrow devices and suppression of the edge effects caused by positive interface fixed charges.

Experimentally, it has not been clear if the advantages that the side-gate gave were only for a shallow trench isolation scheme with positive fixed charges, such as Si_3N_4. Some experiments on polysilicon STI fillings with > 1 μm gate lengths have been in the literature, showing some of the effects seen at accumulated body MOSFETs [3-6]. Experimental portion of this dissertation, along with verifying several effects seen in computational study, is the first demonstration of short and narrow bulk silicon accumulated body n-channel FETs with SiO_2 side-gate dielectric and STI and p+ polysilicon side-gates (Figure 1.2).

Chapter 4 of this dissertation discussing the fabrication of devices addresses major issues in integrating side-gate to conventional CMOS flow by introducing certain techniques. Experimental study also provides a set of processes that can readily be plugged in as a module in CMOS MOSFET fabrication flow.

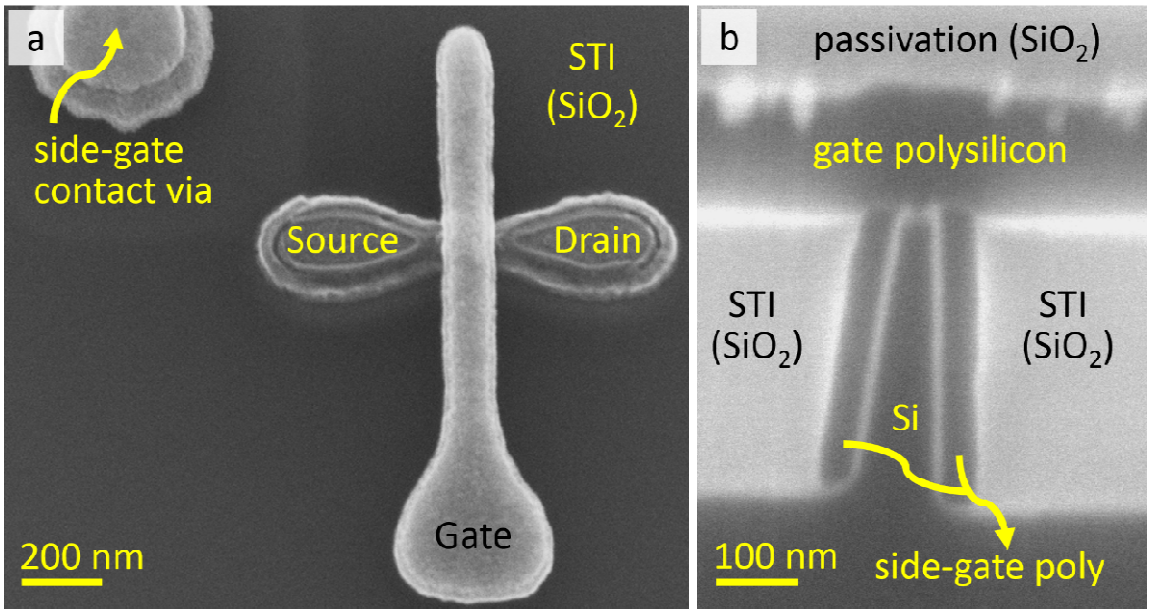


Figure 1.2. SEM micrograph of (a) a long accumulated body FET after silicidation, showing the contacts. (b) cross-section of the channel of a narrow FET ($W_{estimated}$ = 25 nm).

2 Numerical Analysis of Accumulated Body MOSFETs

Modern MOSFET geometries, such as FinFET and tri-gate FETs, have been introduced to increase packing density and reduce short-channel effects [7][8]. The Si fins serving as the body in these devices are controlled by a gate from two or three surfaces. This allows better electrostatic control as well as higher current drive for the same footprint [8] and eliminates the problems associated with defects and fixed charges at the interface of Si and shallow trench isolation (STI), which lead to peripheral leakage currents in narrow planar FETs [9-11], that are used in certain applications such as SRAM cells [12]. Tri-gate FETs, FinFETs and planar FETs can be fabricated using silicon on insulator or bulk approaches. Bulk devices do not suffer as much from problems associated with self-heating and charge-trapping, as they are thermally and electrically anchored to the substrate. While body contacts can be used to electrostatically control the threshold voltage (V_T) of planar devices, 3D geometries are very insensitive to substrate bias as their body is mostly controlled by the gate. Double-gate approaches, using two independently controlled gates sandwiching the body of the device, have been demonstrated earlier for dynamic V_T control or multi-input operation [13-16].

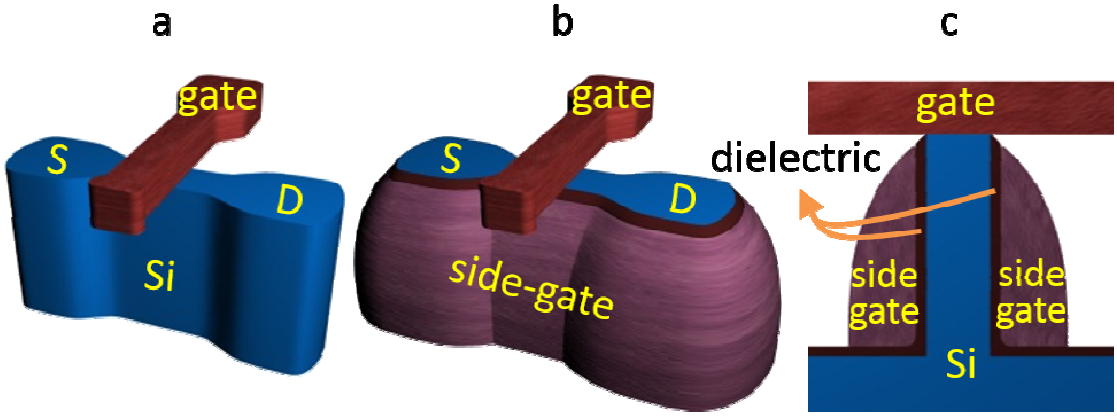


Figure 2.1 Schematics of (a) conventional bulk silicon narrow channel MOSFET (b) an accumulated body MOSFET with polysilicon surrounding gate and (c) cross-section along the channel width of an accumulated body MOSFET.

Integration of an independently controlled side-gate surrounding the body of the FET (Figure 2.1) enables an alternative approach to suppress leakage currents, realize electrostatic V_T control and multi-input functionality [17, 18]. In this geometry, the side-gate is used to accumulate the side-interfaces, passivating the interface defects and countering the impact of positive fixed charges for nFETs. This approach has been shown to suppress leakage currents to < 50 fA at ~ 70 nm gate length using Si_3N_4 as side-dielectric and STI [18] (Figure 2.2).

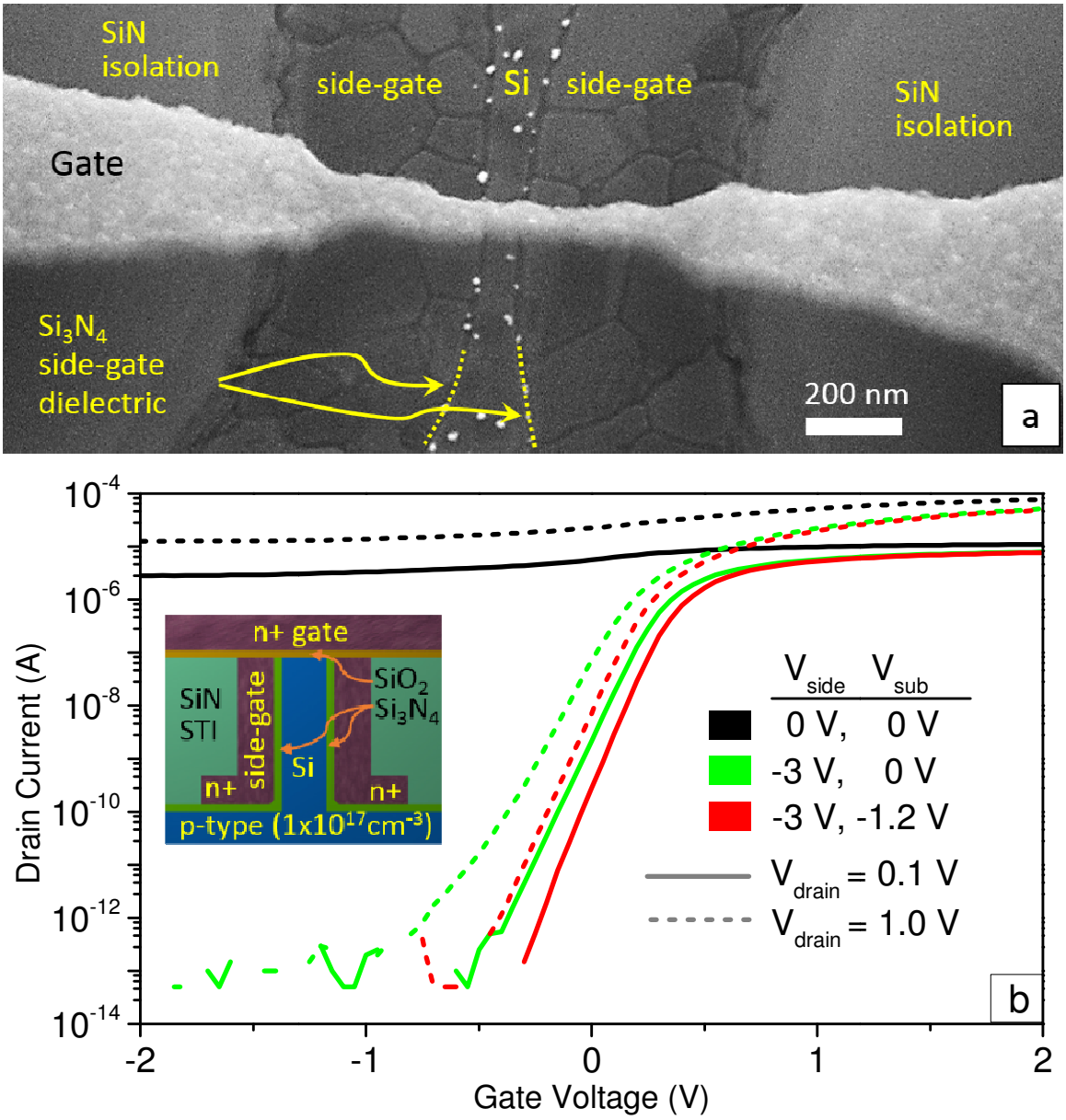


Figure 2.2. (a) SEM micrograph and (b) transfer characteristics of an accumulated body nMOSFET [18] showing suppression of leakage currents and short channel effects. A Si_3N_4 / $Si_{3+x}N_4$ bi-layer is used as STI fill material. W = 68 nm, L = 78 nm, t_{ox} = 4 nm, $t_{side\text{-}dielectric}$ = 19 nm, body $N_A = 3x10^{17}$ cm^{-3}.

In narrow channel devices, significant V_T control and reduced short channel effects have been observed, attributed to accumulation of the whole body [2]. In this section, a 3D model of accumulated body FETs is presented to explain how the side-gate

and the channel interact and how the planar nature of the channel is impacted. At 10-nm scale, we explore effects such as the increase in source barrier height by accumulation of the body of narrow devices and suppression of the edge effects caused by positive interface fixed charges.

2.1 Sentaurus Platform

Sentaurus is a Technology Computer Aided Design (TCAD) tool developed by Synopsys. Sentaurus is capable of simulating a wide range of electronic devices from transistors to solar cells to LEDs.

Sentaurus is a compilation of some of the best simulation tools in the industry / academia. This fact, however, brings about complexities in terms of differences in scripting languages for each tool as well as possible interfacing problems in addition to issues caused by the fact that it only runs on Linux systems.

Different components of this suite as well as a brief guide on running these tools are given in Appendix (7.1)

2.2 Simulation of Device Fabrication

Simulated structures are bulk Si planar n-channel MOSFETs ($N_A = 1x10^{18}$ cm^{-3}) with channel widths (W) of 10 nm and 30 nm, and gate lengths (L) of 15 nm, 40 nm and 50 nm. Highly-doped polysilicon side-gate is separated from the body by 16 nm of SiO_2. Gate SiO_2 thickness (t_{ox}) is 2.8 nm. The structures were generated using process simulations [19] as summarized in Figure 2.3.

Source and drain regions are generated with low-energy arsenic implantation to form low drain doping (LDD) extension, followed by Si_3N_4 spacer formation and a high energy arsenic implantation. The LDD has a ~30 nm junction depth and a peak doping level of $1.25x10^{20}$ cm^{-3}, whereas the high energy implants have a junction depth of ~185 nm and a peak doping level of $4x10^{20}$ cm^{-3}. In addition, between the LDD extension and source/drain implantation processes, four Boron halo implantation steps with $0.5x10^{13}$ cm^{-2} dose, and 20 keV energy with four rotations are simulated. After the ion implantation process simulation (Figure 2.3f), the gate and side-gate polysilicon are assigned uniform doping values of $1x10^{20}$ cm^{-3}. This improves convergence for electrical device simulations.

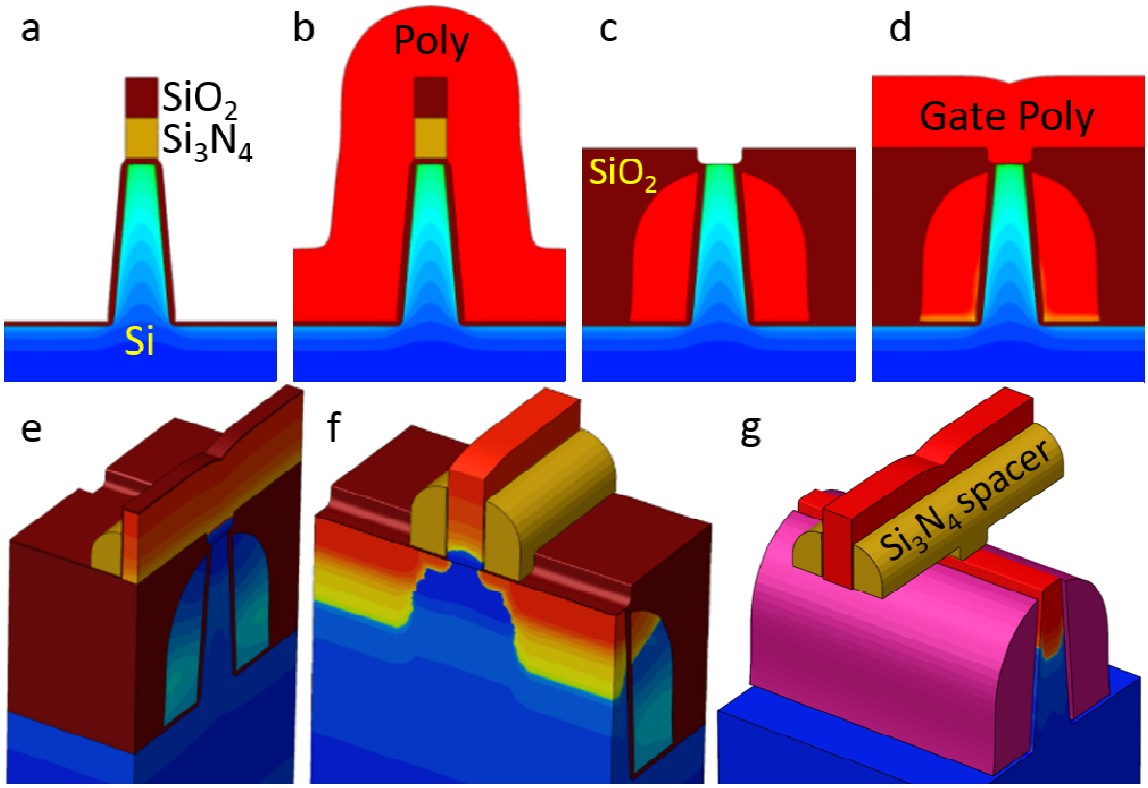


Figure 2.3. Process simulation steps for the accumulated body MOSFET. (a) 400-nm-tall Si mesa ($1x10^{18}$ cm^{-3} Boron doped) is defined under a SiO_2, Si_3N_4 hard mask. 16 nm SiO_2 is grown on the

side surfaces to serve as the side-gate dielectric. (b) side-gate polysilicon (n+ or p+) is deposited. (c) side-gate is formed using a spacer reactive ion etching (RIE) process; the trench is then filled with SiO_2, followed by polishing and removal of the Si_3N_4 hard mask. (d) 2.8 nm SiO_2 top gate dielectric is grown and top gate polysilicon is deposited. (e) 2D structure is extruded into 3D; Si_3N_4 spacer formation. (f) Source/drain ion implantation (half device shown). (g) Complete device structure after gate and side-gate are assigned constant doping of $1x10^{20}$ cm^{-3} (STI not shown).

On a more detailed level, the simulation approach is a 2D-3D hybrid. The simulation, as explained above, starts with a 2D process simulation up to nitride spacer definition (Figure 2.3 a-d shows a mirrored version). Then Sentaurus Structure Editor is used for extrusion of the 2D structure and for adding emulated nitride spacers, followed by a Sentaurus Mesh step to enhance process simulations. 3D Sentaurus Process is used for halo and source/drain ion implantation. Afterwards, Sentaurus Structure Editor is used to assign uniform doping for side-gate and the gate, and to cut the bottom portion of the device. Sentaurus Mesh is called once more for a final meshing, which is used in Sentaurus Device for Electrical Characteristics simulations.

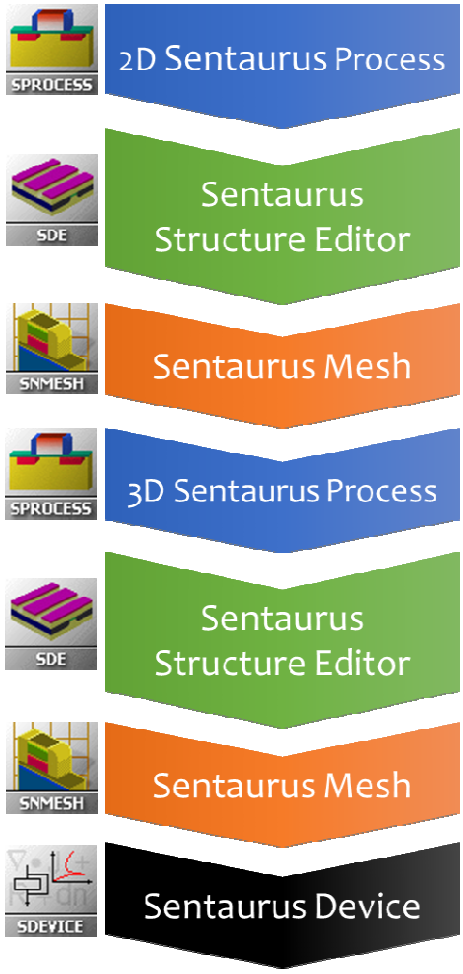


Figure 2.4. Flow of different Sentaurus tools used for the numerical analysis.

2.3 Simulation of Electrical Characteristics

Steady-state device simulations are conducted using quantum-corrected drift-diffusion models in Synopsys Sentaurus Device [19]. The Poisson and current continuity equations are solved self-consistently to find the current and potential throughout the device [19]. The Modified Local Density Approximation method [19, 20] is used to account for quantum confinement effects in narrow channels and the Philips unified mobility model [21] is used with mobility degradation due to doping and electric field [21, 22]. Shockley-Read-Hall recombination model is used for generation-recombination

processes. Lattice temperature of 300 K and no interface positive fixed charges are assumed except when noted otherwise.

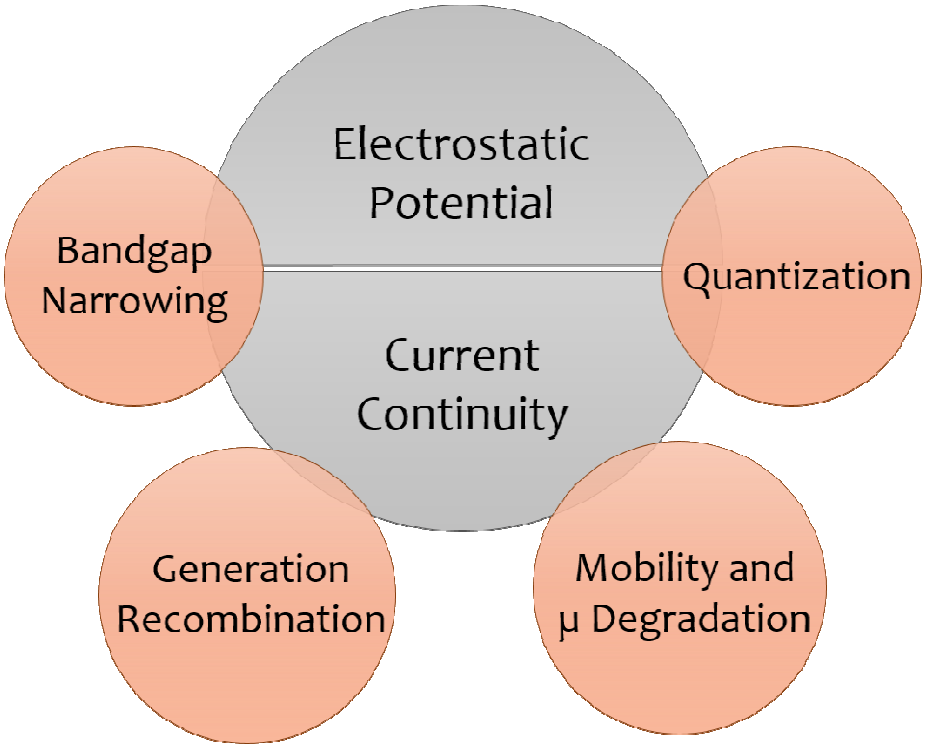


Figure 2.5. Schematic showing various components of physics considered in Sentaurus Device for the numerical analysis.

2.4 Channel and Body Electrostatics

The off-current and V_T of a MOSFET are directly related to the source energy barrier. This barrier may be lower in the edges of the active region, near the Si-SiO_2 interface, due to positive fixed charges and edge effects [9], leading to increased leakage currents. In an accumulated body nMOSFET, a negatively biased side-gate attracts majority carriers from the body, accumulating the Si-STI interfaces; with sufficient bias, the whole body can be accumulated starting from the narrower sections of the device (Figure 2.6).

Accumulation of the interfaces and body increases the source barrier height in the channel starting at the edges. This effect decreases leakage currents and drain induced barrier lowering (DIBL), and increases the V_T (Figure 2.7).

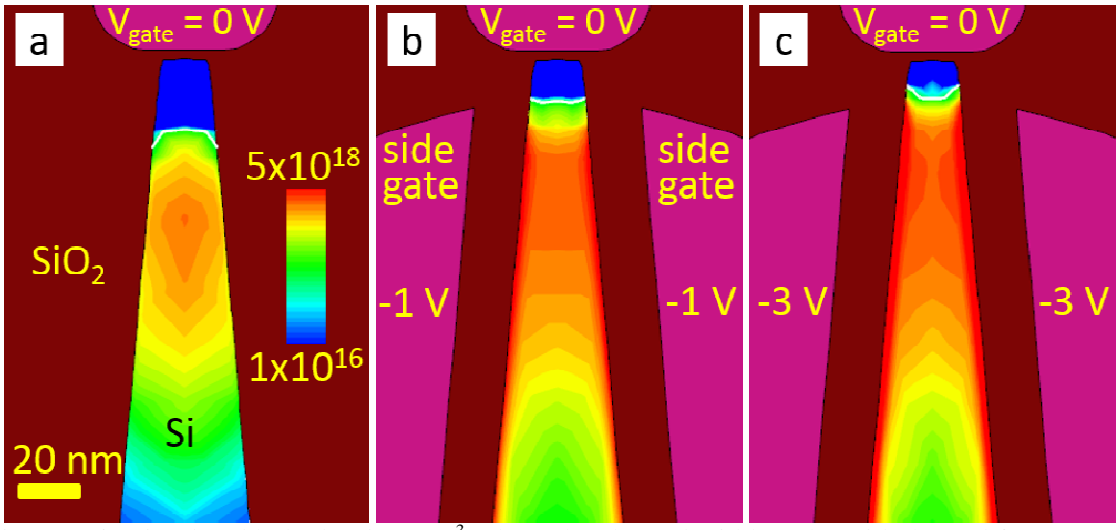


Figure 2.6. Simulated hole density (cm^{-3}) along the channel width at the mid-channel for (a) a conventional nMOSFET, (b) (p+ side-gate) accumulated body nMOSFET with V_{side} = -1 V, (c) same accumulated body FET with V_{side} = -3 V showing accumulation extending to whole width in narrower portions. V_{drain} = 1 V, V_{gate}, V_{sub} = 0 V, W = 15 nm, L = 50 nm.

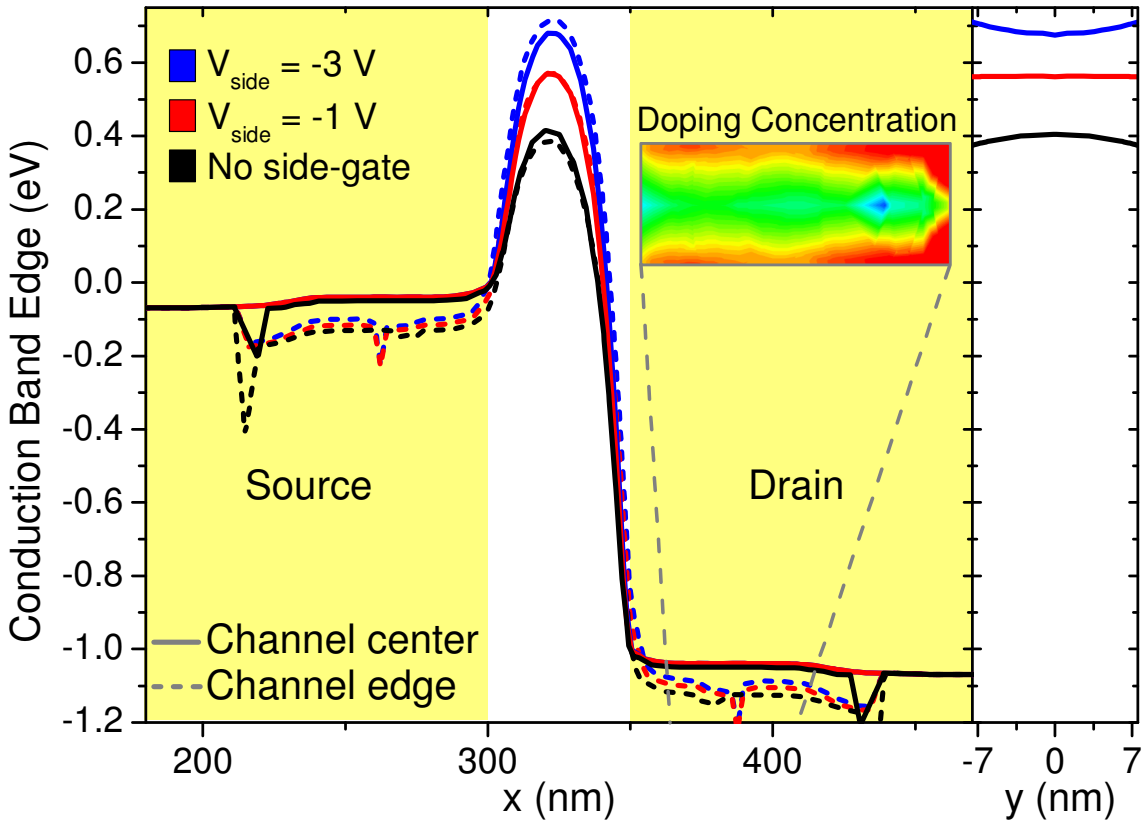


Figure 2.7. Conduction band edge energy level along the channel length (x) and width (y) at V_{gate} = 0 V. Energy barrier goes up when side-gate bias is applied on the p-type side-gate. The edges accumulate more than the center of the channel as a result of the side-gate bias. V_{drain} = 1 V, V_{sub} = 0 V, W = 15 nm, L = 50 nm, cut taken 5 nm below channel top surface. Higher edge barriers at the source and drain are due to a small non-uniformity in the LDD extension doping along the width of the channel (higher doping on the edges, an artifact of geometry reflection. See inset (red: 1.3×10^{20}, green: 1.2×10^{20} cm^{-3})). The energy barrier spikes within source and drain are associated with reduced meshing at these locations.

This accumulation can be controlled by the side-gate bias, as well as by work function engineering of the side-gate. Figure 2.8 shows the transfer characteristics for two extreme cases achievable by saturated doping of the polysilicon side-gate as n+ and p+. An n+ side-gate causes depletion at the body-STI interface at V_{side} = 0 V, which leads to

severe performance degradation due to very high off-current. In the case of a p+ side-gate, however, off-current improvement is observed even at V_{side} = 0 V due to side-gate's higher work function (Figure 2.8).

Smaller foot-print fixed-V_T devices can be fabricated without a side-gate contact and the V_T can be set by adjusting the work function of the side-gate.

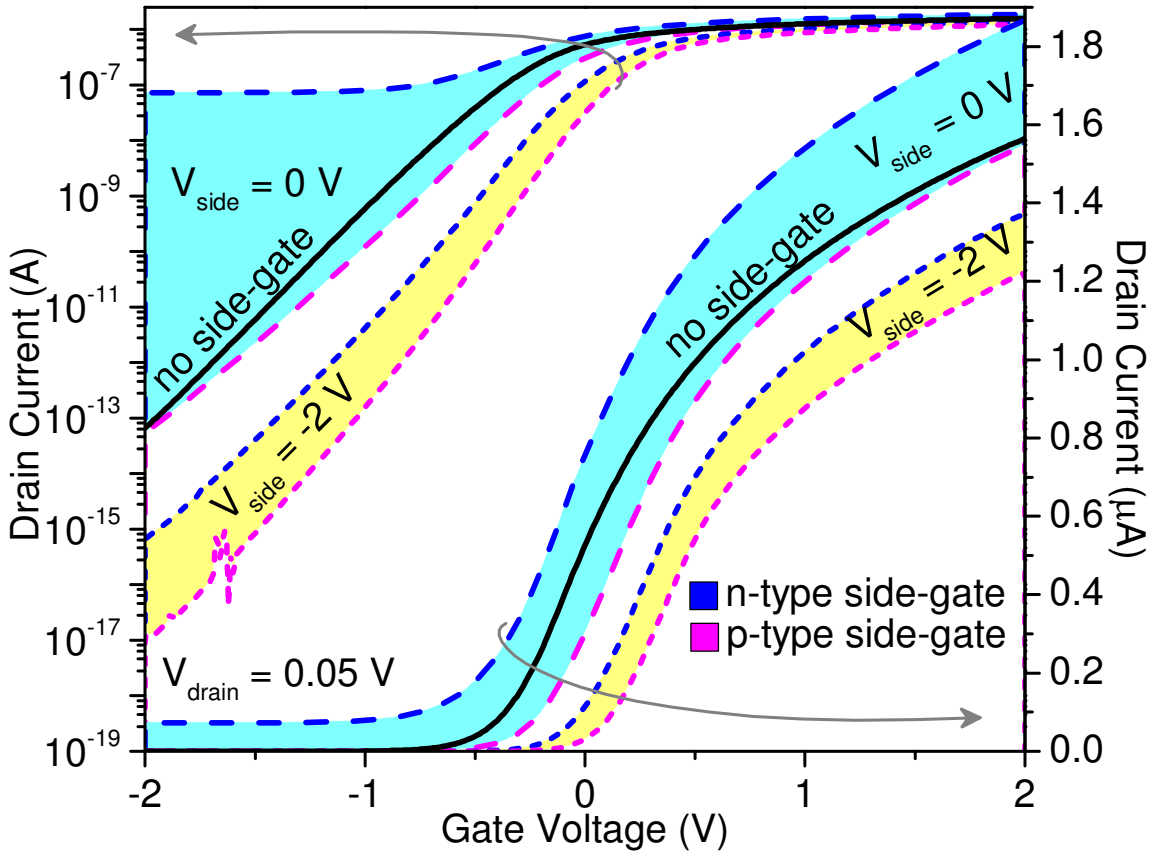


Figure 2.8. Transfer characteristics for n-type and p-type polysilicon side-gate (highly doped $1x10^{20}cm^{-3}$) accumulated body MOSFETs (V_{side} = 0 V and V_{side} = -2 V); and for a conventional MOSFET (no side-gate). V_{drain} = 50 mV, V_{sub} = 0 V, W = 10 nm, L = 15 nm. For the case where V_{side} = 0 V, the n-type side-gate device shows a drastically degraded off-current compared to the conventional MOSFET due to the depletion the side-gate causes at the side interfaces. Cyan and yellow shadings show the difference between n+ and p+ side-gates for V_{side} = 0 V and V_{side} = -2 V respectively.

2.5 Electrical Characteristics

Transfer characteristics for an nFET with W = 10 nm and L = 15 nm with a p+ side-gate show the suppression of leakage currents, leading to an improved SS, and a shift in V_T obtained with increasing negative side-gate bias (Figure 2.9). As expected, and also observed experimentally, V_T shift sensitivity ($\Delta V_T/V_{side}$) decreases with increasing side-gate bias [1]. The average V_T shift for the device in Figure 2.9 is ~0.3 V per volt applied to the side-gate. For the same device, SS decreases by ~20% per volt applied to the side-gate and DIBL decreases by ~30% for these devices (Figure 2.10). At a width of 30 nm, the effect of the side-gate is much smaller and only becomes significant in the presence of interface positive fixed charges.

Above threshold, however, increased side-gate bias leads to stronger confinement of carriers due to the enhanced vertical field, increasing the surface roughness scattering and degrading the current drive (Figure 2.9 and Figure 2.11). For higher drain voltages, where carriers are not as strongly confined to the surface channel, accumulation provided by the side-gate has a positive effect, keeping the channel from over-broadening after pinch-off (Figure 2.11 and Figure 2.12) [23].

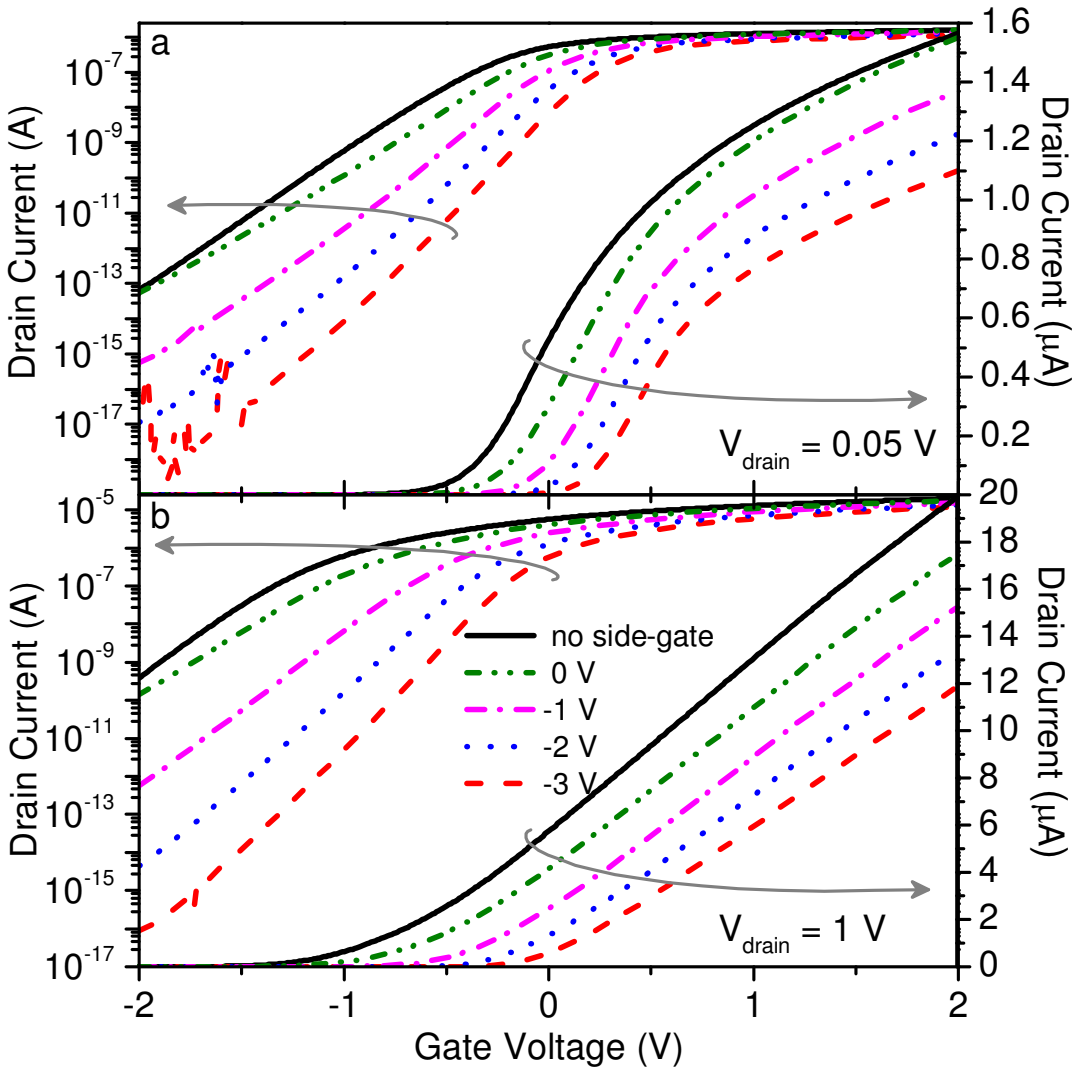


Figure 2.9. Transfer characteristics for a conventional (no side-gate) and a (p+ side-gate) accumulated body nMOSFET for (a) V_{drain} = 50 mV and (b) V_{drain} = 1 V, showing V_T shift and off current reduction. V_{sub} = 0 V, W = 10 nm, L = 15 nm.

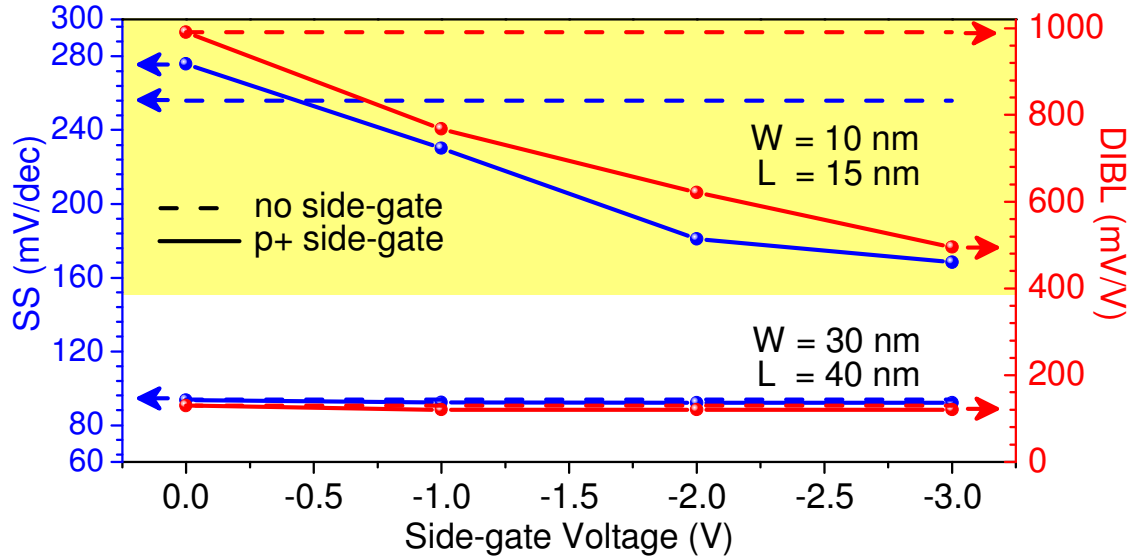


Figure 2.10. Subthreshold slope (SS) (blue, left axis) and DIBL (red, right axis) for a narrow and short (top) and for a wider and longer (bottom) nMOSFET. Sensitivity to the side-gate voltage degrades for wider devices. Dashed lines correspond to conventional nMOSFETs. SS is extracted at V_{drain} = 1 V, V_{sub} = 0 V. DIBL is calculated as $V_{T\text{-}lin} - V_{T\text{-}sat} / 0.95$ (V_{drain} = 0.05 V for $V_{T\text{-}lin}$, 1 V for $V_{T\text{-}sat}$).

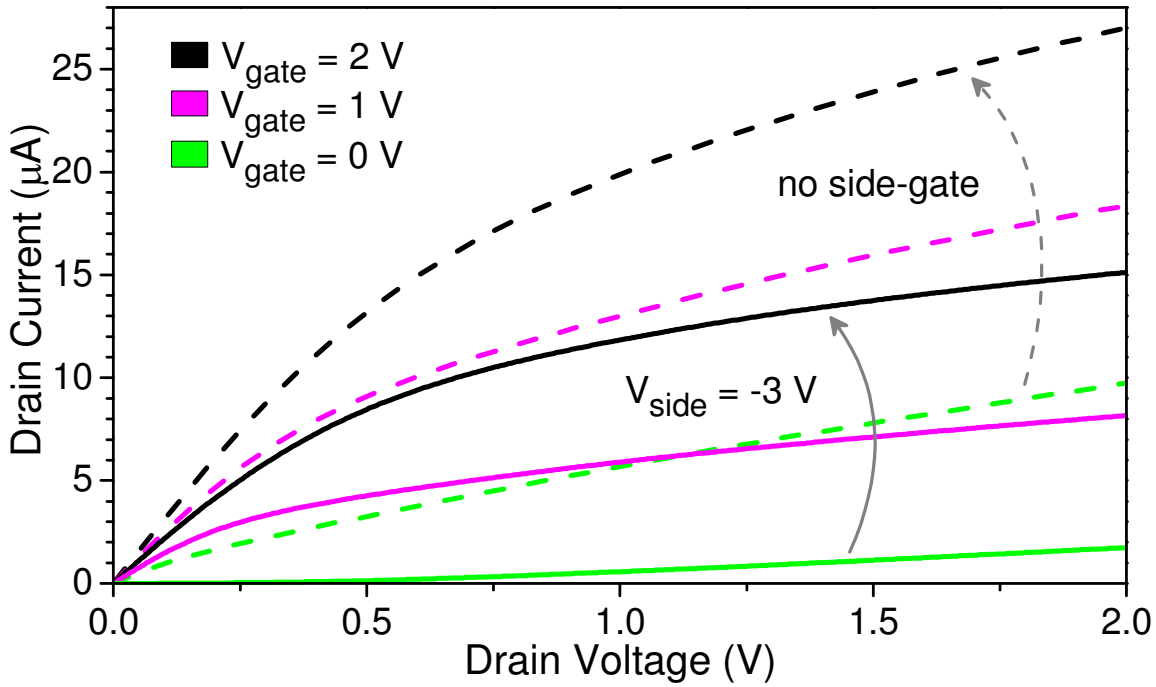


Figure 2.11. Output characteristics of conventional (dashed) and (p+ side-gate) accumulated body nMOSFETs with a -3 V side-gate bias (solid). V_{sub} = 0 V, W = 10 nm, L = 15 nm.

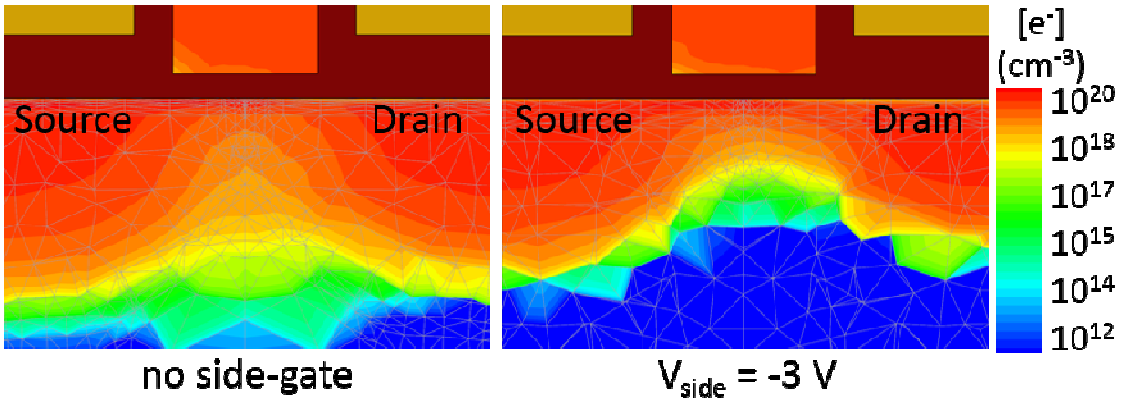


Figure 2.12. Electron density in the center of the channel at high V_{drain} for a conventional (left) and an accumulated body FET (right). V_{drain} = 2 V, W = 10 nm, L = 15 nm, V_{gate} = 2 V, V_{sub} = 0 V.

2.6 Side-gate vs. Substrate Biasing

Substrate biasing has been traditionally used for dynamic V_T control for bulk Si MOSFETs. For an nMOSFET, V_T can be increased by applying a negative bias on the substrate. However, this also yields to widening of the depletion regions, aggravating short channel effects; and increased drain to substrate field results in leakage by band-to-band tunneling. Moreover, V_T sensitivity to substrate is a strong function of channel doping and degrades for MOSFETs with low body-doping [24-26].

Side-gate biasing, on the other hand, provides capacitive coupling to the body through a relatively thick dielectric with minimal tunneling leakage current and increased coupling to the substrate (i.e. reduced depletion depth) by accumulation of the body. For a narrow device, the V_T shift achieved by the side-gate bias is significantly stronger than what is achievable by the substrate bias (Figure 2.13). Both biasing schemes, however, can be combined to achieve an even stronger V_T tuning. In narrow channel devices, the

body can be completely depleted by the side-gate to substrate capacitor (Figure 2.14b). As V_{side} approaches V_{sub} (Figure 2.14c), side-gate starts accumulating parts of the body, increasing the coupling to the substrate and effectively providing electrostatic doping.

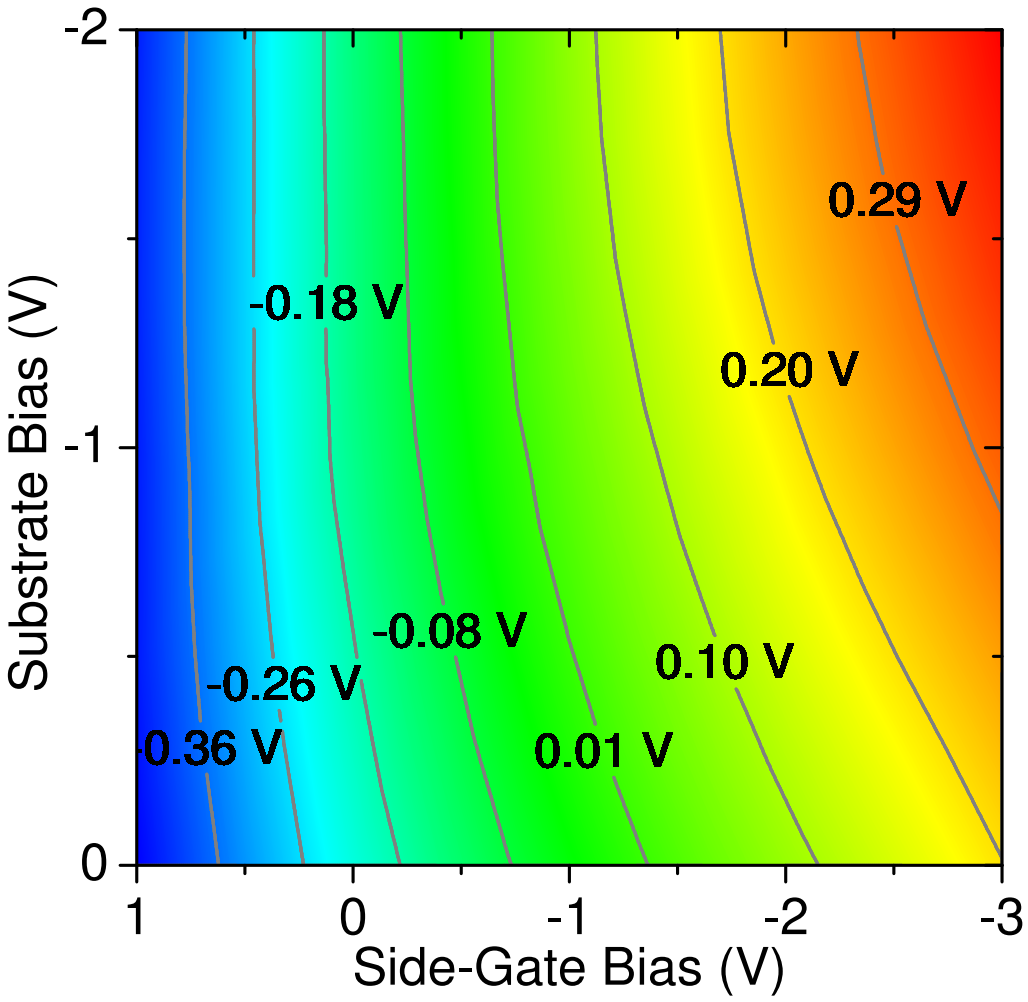


Figure 2.13. Sensitivity of V_T to side-gate bias, substrate bias and their combination. V_{drain} = 0.05 V, W = 10 nm, L = 15 nm.

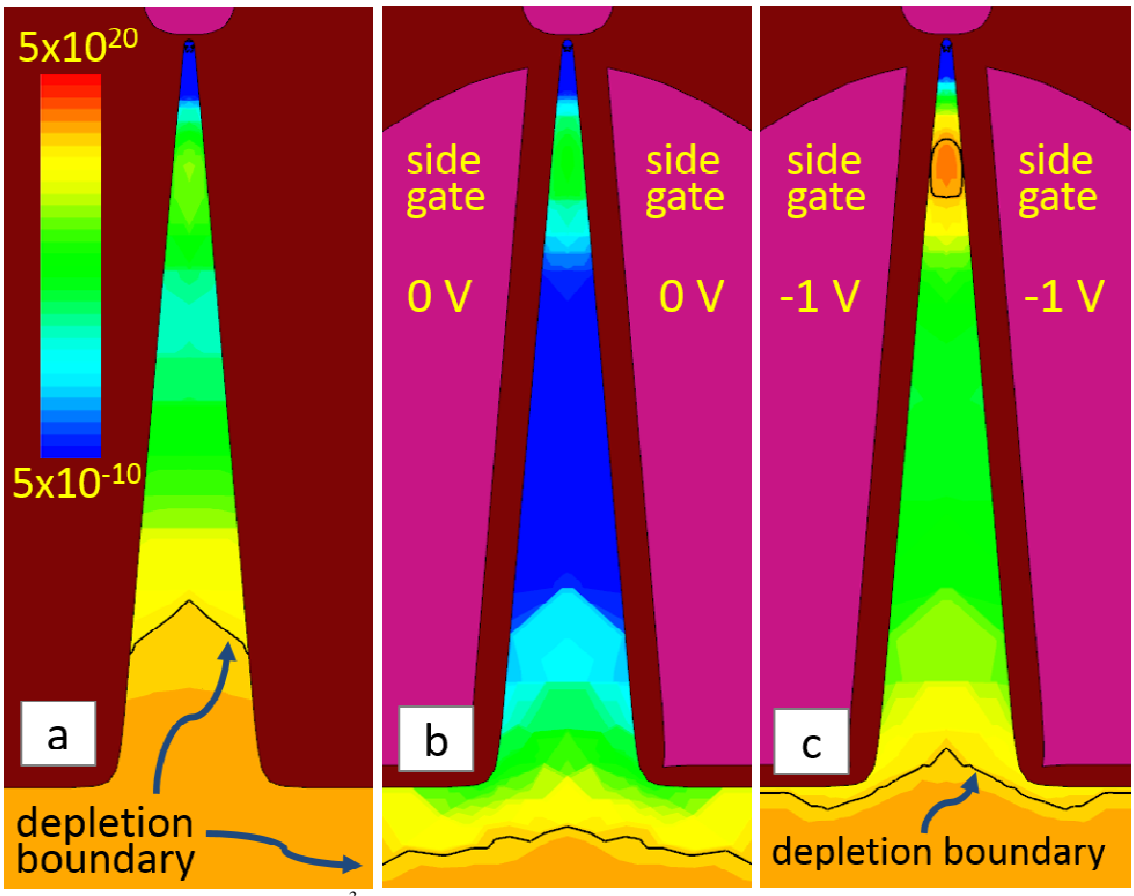


Figure 2.14. Hole density (cm^{-3}) when V_{sub} = -2 V for (a) conventional FET (b) p+ side-gate at V_{side} = 0 V, (c) V_{side} = -1 V. The side-gate to substrate capacitance helps the substrate bias deplete the whole body. W = 10 nm, L = 15 nm, V_{gate} = 2 V, V_{drain} = 0.05 V.

2.7 Comparison to FinFET and Wide Planar MOSFETs

To understand how accumulated body FETs fit into the current technology trends, a comparative numerical analysis with FinFETs and wide planar FETs is also conducted. When a FinFET is formed by replacing the gate of a narrow and short FET (W = 10 nm, L = 15 nm) (Figure 2.15), it is seen that FinFET provides superior electrostatic control of the channel resulting in better subthreshold characteristics. This effect, however, exists at

the expense of sensitivity to substrate bias and a V_T that cannot be changed dynamically because of this loss of sensitivity.

Analysis of a wide (W = 100 nm) planar FET with a short gate length (L = 15 nm) shows, on the other hand, degraded off current and short channel characteristics with a min/max current ratio of ~10^2 which fares far less than the ~10^{10} ratio achieved by the accumulated body FET (Figure 2.15).

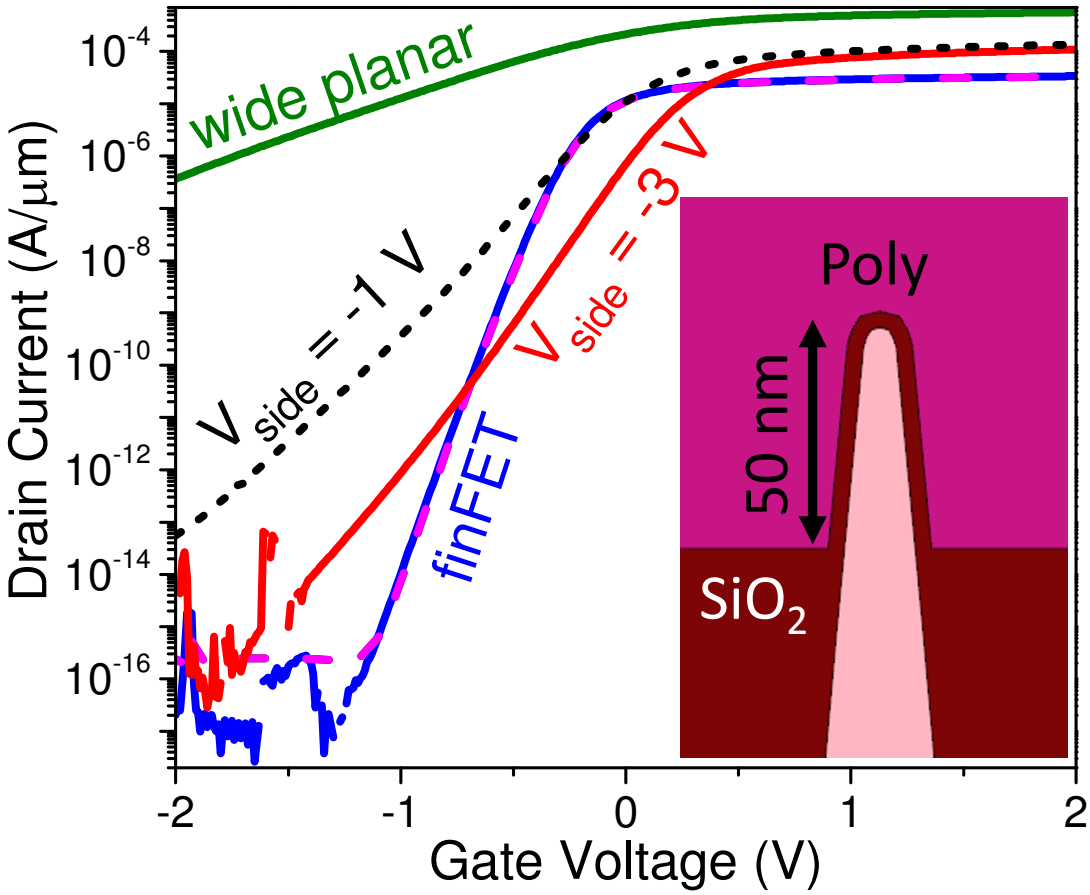


Figure 2.15. Normalized transfer curve comparing a FinFET (W_{fin} = 10 nm), a wide planar FET (W = 100 nm) and an accumulated body FET (W = 10 nm), showing limited FinFET response to substrate bias of -2 V (magenta), and low on/off ratio of the wide FET. Inset shows the cross-section of the FinFET. L = 15 nm, V_{drain} = 0.05 V.

2.8 High Temperature Characteristics

High temperature behavior of accumulated body MOSFETs is investigated taking temperature into account for mobility degradation and increased generation rate in the Philips Unified Mobility and in Shockley-Read-Hall recombination models respectively.

At higher temperatures, increased thermal carrier generation leads to increased off current and degraded SS in FETs. A negative side-gate bias suppresses off current and improves SS by accumulating the body [27].

The results indicate that, even at high temperatures (e.g. at 600 K), where conventional MOSFETs fail to properly turn off, an accumulated body MOSFET with V_{side} = -3 V shows an I_{max}/I_{min} ratio of over 3 orders of magnitude (Figure 2.16).

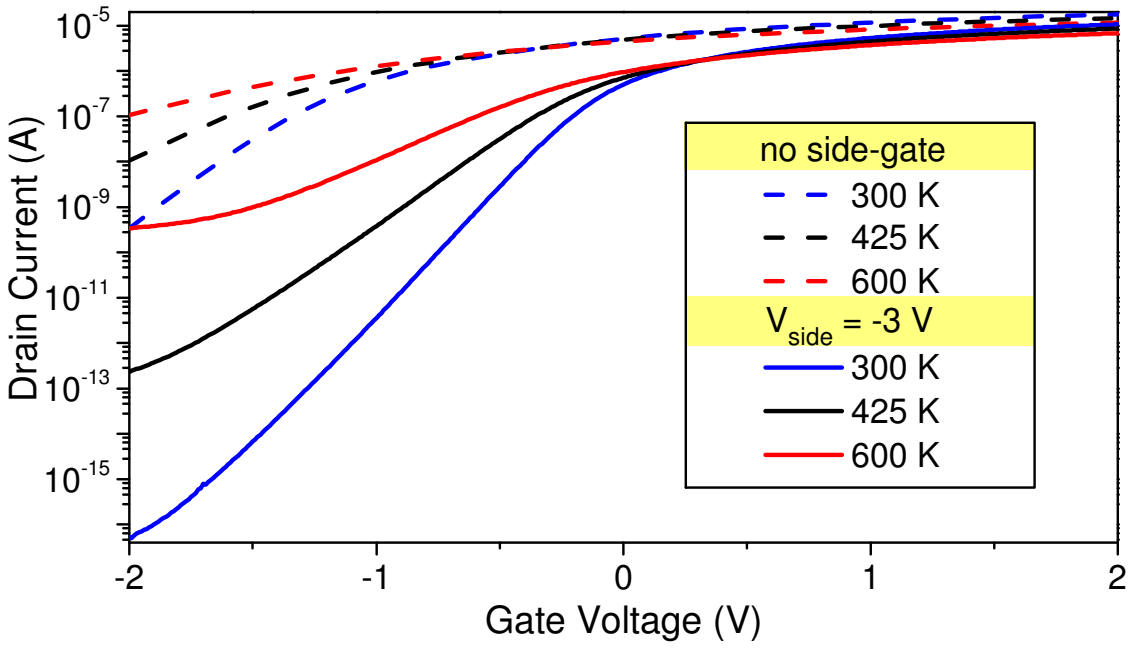


Figure 2.16. Temperature sensitivity of the transfer characteristics. V_{drain} = 1 V, V_{sub} = 0 V, W = 10 nm, L = 15 nm, p+ side-gate.

2.9 Characteristics under Imposed Interface Positive Fixed Charges

A side-gate structure is also useful in passivating the positive fixed charges on the Si-SiO_2 interface of body and STI, suppressing the leakage currents at the side interfaces. These interfaces are prone to have more defects and fixed charges due to damage from the reactive ion etch process used to define the Si fin and the low-temperature STI dielectric deposition [9]. Although different techniques, such as hydrogenation of dangling bonds at the Si surface have been used to alleviate the fixed charge problem [11], it remains an issue for scaled nMOSFETs.

A negative bias on the side-gate can be used to passivate the defects and to compensate for the positive fixed charges. To analyze this effect, we have simulated devices with an imposed positive fixed charge sheet of $1x10^{12}$ e^-/cm^{-2} at the Si-SiO_2 interfaces. The results show an improvement in I_{max}/I_{min} ratio by 10^4-10^{10} times for V_{side} = 0 to -3 V, mainly due to suppression of leakage currents (Figure 2.17). The improvements in the off-current (Figure 2.18) are in line with the experimental characteristics for an accumulated body FET with SiN-based dielectric (Figure 2.2). Hence, passivation of the side interfaces with side-gate biasing can enable the use of alternative dielectric materials for isolation for various applications. For example, accumulated body MOSFETs can be monolithically integrated with micro/nano-fluidic systems using a Si_3N_4 STI so that a sacrificial silicon dioxide layer can be used to form tunnels and removed afterwards in buffered oxide etch, for highly sensitive chemical and biological sensors [2].

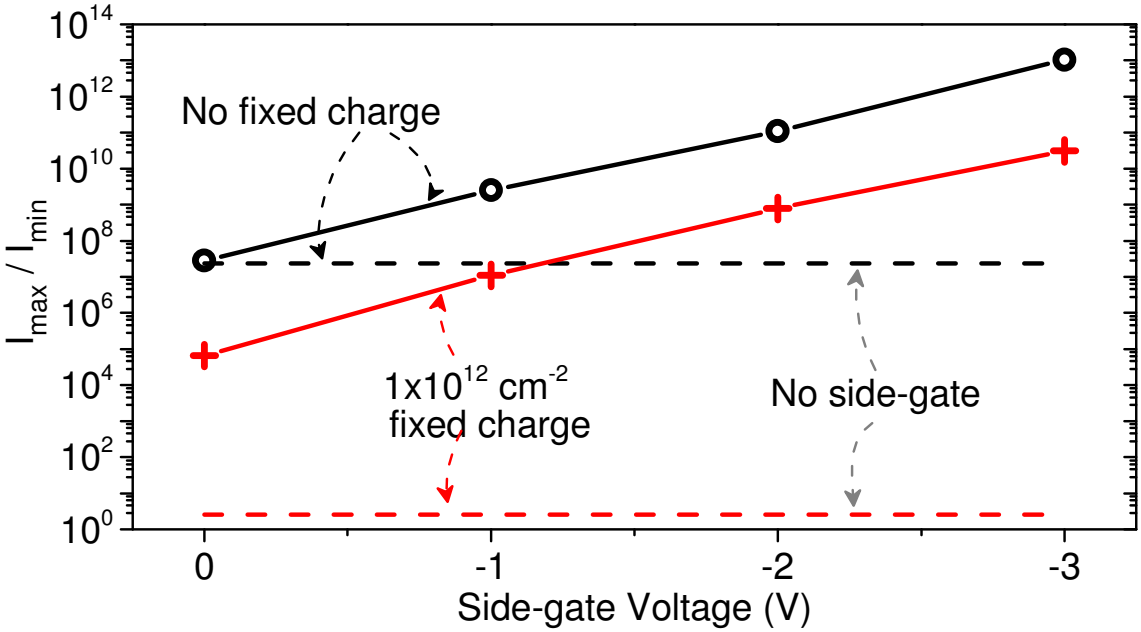


Figure 2.17. Maximum and minimum current ratio (taken at V_g = 2 V and V_g = -2 V respectively) for conventional and (p+ side-gate) accumulated body nMOSFETs with and without an imposed positive fixed charge. The ratio increases with increasing negative side-gate bias compensating the positive fixed charges. V_{sub} = 0 V, W = 10 nm, L = 15 nm.

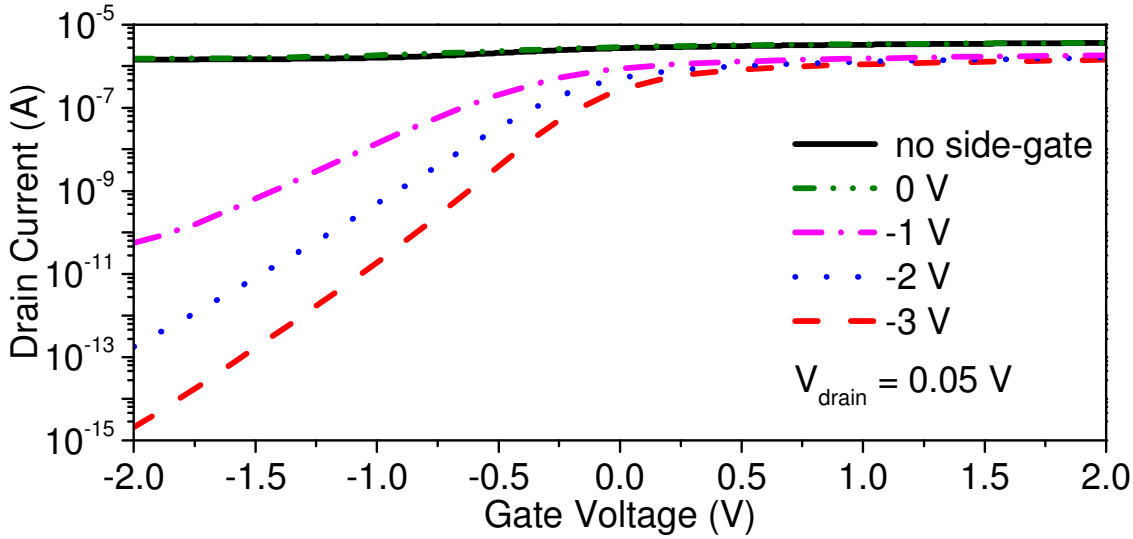


Figure 2.18. Transfer characteristics for an nMOSFET with 1x10^{12} cm^{-2} interface positive fixed charges. The side-gate is n+ doped, which does not provide improvement for V_{side} = 0 V. W = 10 nm, L = 15 nm, V_{sub} = 0 V.

2.10 AC Analysis

Side-gate's spacer-like geometry ensures strong coupling to the channel while reducing parasitic capacitance to the gate. This added capacitance, however, is important for gate delays. C-V characteristics of the gate of a narrow device (Figure 2.19) show a constant capacitance increase with the introduction of the side gate. When translated into intrinsic gate delay (CV/I), conventional FET results in 12.9 ps, which increases to 32.2 ps for an accumulated body FET with the side-gate biased at -3 V. The main reason of the slowdown is lower output current with the side-gate bias, as explained in subsection 2.5. On the other hand, accumulated body FETs can be fabricated to have shorter gate lengths for the same leakage performance which may compensate for this increase in parasitic capacitance.

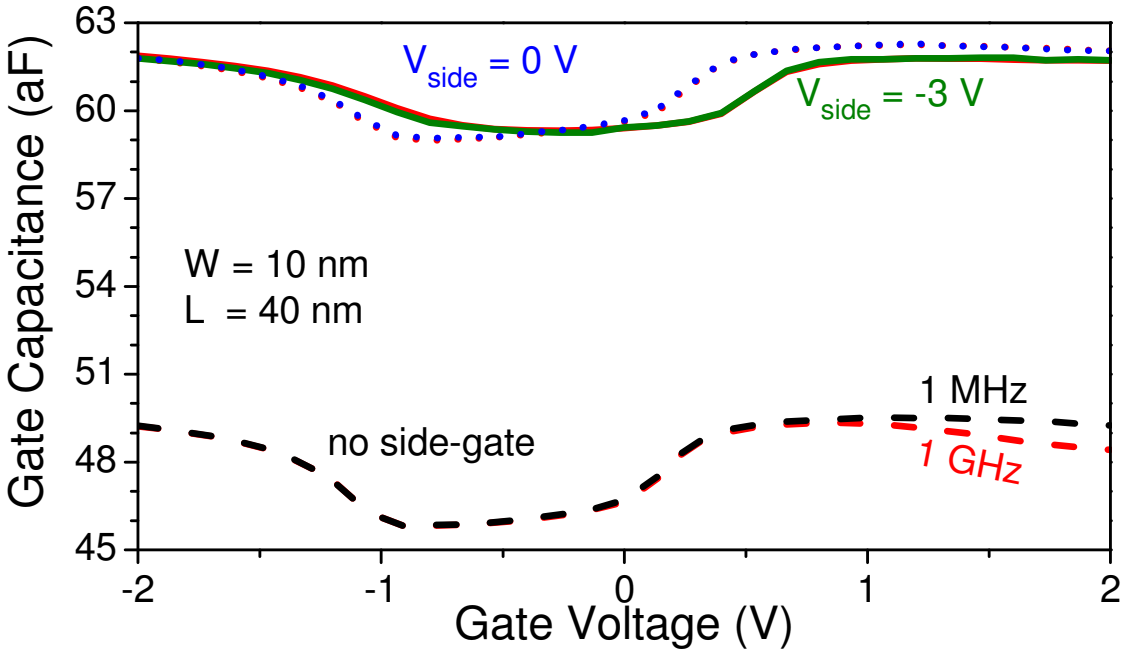


Figure 2.19. Gate C-V characteristics showing increase in gate capacitance with the side-gate and the threshold voltage shift with side-gate bias (p+ side-gate). f = 1 GHz (red), 1 MHz for the rest.

2.11 Three-dimensional Monte Carlo Simulations

The 3D nature of side-gated devices requires any solution with Monte Carlo method to be three-dimensional as well.

Sentaurus Device Monte Carlo (version G-2012.06 and later) provides 3D Monte Carlo simulation capability, using the single-particle approach [28].

In this particular approach, single charge-carrying particle is considered at a time from the contact it enters to the contact it exits from; in contrast to the ensemble approach where a set of particles is simulated at the same time [29].

2.11.1 Simulation Method

To get the most accurate picture available for extremely scaled transistors, we used three-dimensional, single-particle Monte Carlo simulations. As shown in Figure 2.20, the channel width and effective channel length were chosen to be 15 nm, with a low-doped ($1x10^{16}$) p-type body. A 20 nm polysilicon gate separated from the channel by a 2 nm SiO_2 was assumed. Side-gate structure of the experiment was mimicked by placing two polysilicon plates on the either side of the channel separated from the body by a 4 nm SiO_2. Control groups with no side-gates were also simulated. Synopsys Sentaurus Monte Carlo tool [30] used for the simulations takes into account the full band structure for Si, as well as four scattering mechanisms, namely phonon scattering, impurity scattering, impact ionization, and surface roughness scattering. For the latter, a phenomenological approach is assumed where for each electron hitting the dielectric surface, a specular or diffusive scattering process is assumed randomly. To match

literature values, however, a bias towards more specular scattering is used [31], where 85% of electron-dielectric collisions resulted in specular scattering.

We used drift-diffusion simulations to create initial guesses for Monte Carlo simulations, as well as to compare results wherever appropriate.

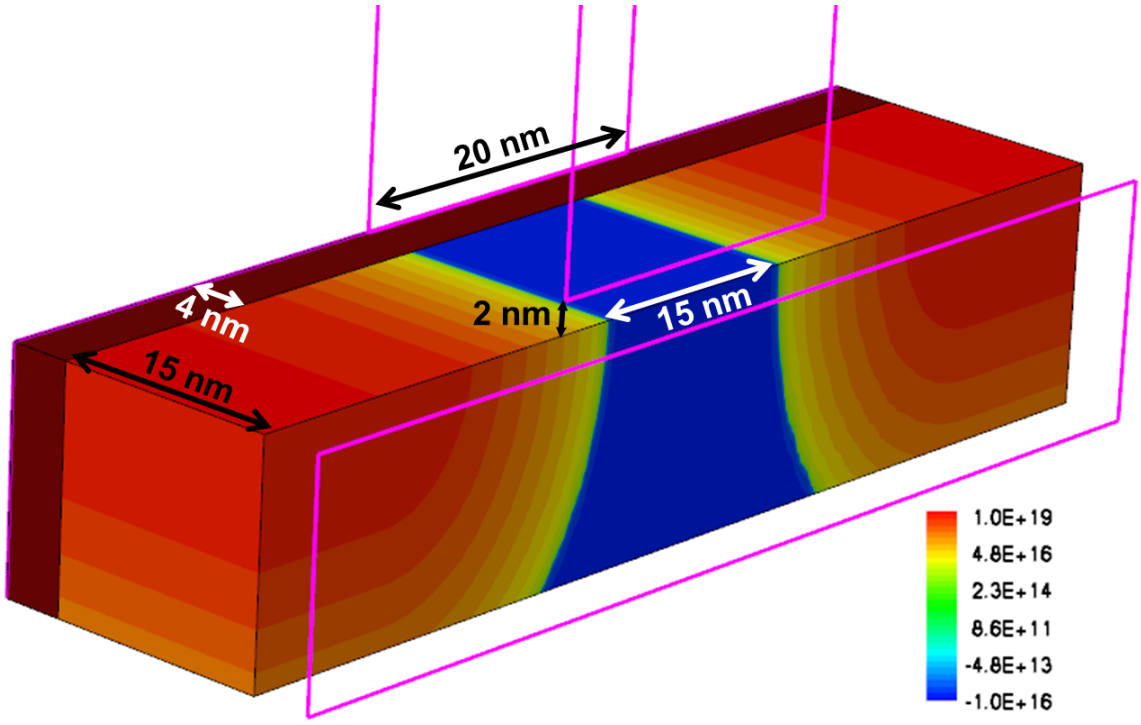


Figure 2.20. nMOSFET geometry used for Monte Carlo simulations. Pink outlines are for contacts. Gate oxide is not shown. Legend shows the doping concentration (red: n-type, blue: p-type)

2.11.2 Simulation of Electrical Characterization

Transfer characteristics of the device were extracted by running an individual MC simulation for each bias condition (each data point in the curve). The results show that at

higher gate voltages, surface roughness scattering dominates the conduction, leading to a zero, then a negative transconductance value (Figure 2.21). This effect is not readily visible on experimental devices at room temperature, implying that surface scattering in the model is stronger than it actually is.

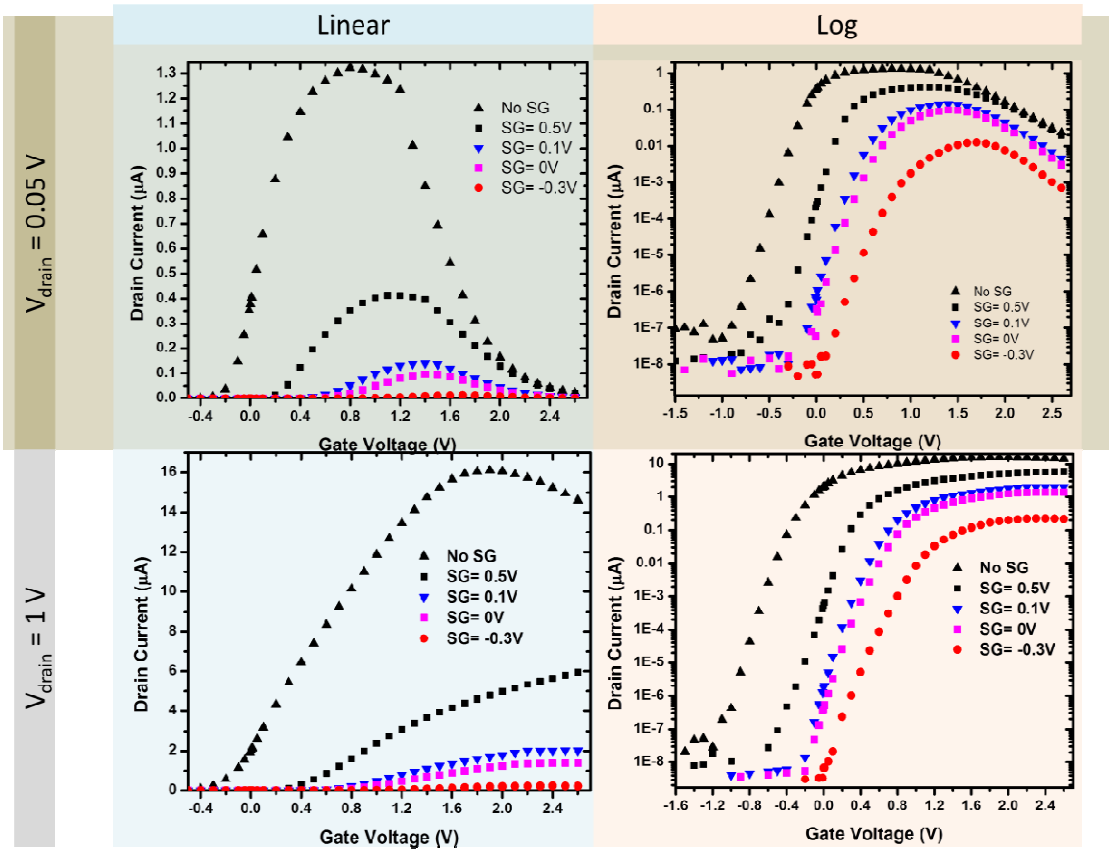


Figure 2.21. Transfer characteristics generated using Monte Carlo simulations for the device in Figure 2.20. Surface scattering dominates and leads to a negative transconductance effect in higher gate voltages.

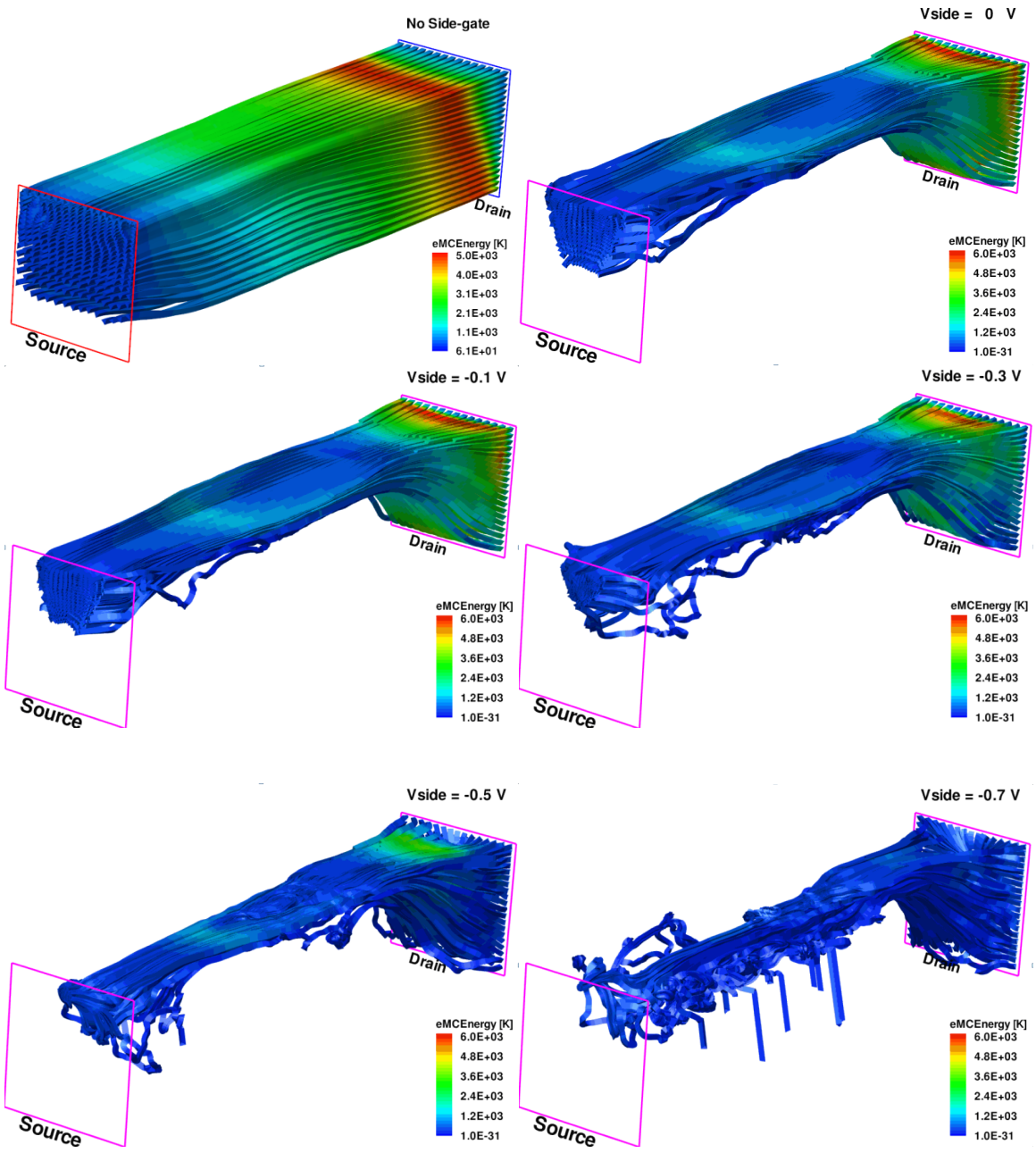


Figure 2.22. Electron velocity streamlines for an nMOSFET with no side gates (top left) and as more side-gate bias is applied for side-gated devices. It is seen that electrons are more and more confined to the top surface as more side-gate bias is applied. Color indicates electron energy.

Monte Carlo simulations also enabled us to see the electron density and energy distribution throughout the device.

When electron velocities are traced with their direction information, it is seen that at higher gate voltages, carrier energy and velocity are disrupted near the interface of Si and the gate dielectric, especially for side-gated transistors (Figure 2.22). This implies that increased surface scattering occurs when side-gate structure is introduced to the MOSFET. These results, however, should be taken with a grain of salt, mainly because the amount of negative transconductance extracted is not close to any experimental value even at reduced temperature, let alone at room temperature [32, 33]. This implies that more complicated surface scattering models need to be considered for a case like side-gated transistor.

3 Investigation of Line Edge Roughness and Accumulated Body MOSFETs

Line edge roughness (LER) has been a limiting factor in gate scaling of silicon MOSFETs [34]. Recently, however, with the introduction of lithographically defined thin body devices such as FinFET and Tri-gate FETs, LER started to affect the active region of MOSFETs as well [35, 36]. Grazing incidence ion beams [37] and high temperature hydrogen annealing [38] have been proposed to reduce LER, which was shown to result in significant silicon diffusion with LER reduction from ~ 2.8 nm to 0.8 nm. In this chapter, instead of focusing on reduction of LER itself, an electrostatic method to reduce the effects of LER is studied, through the use of a guard-ring gate surrounding the body of the FET.

It was previously shown that gating the body of a Si MOSFET with a side-gate biased such as to accumulate the Si body (Figure 3.1) reduces off-state leakage currents by countering the effect of positive fixed charges and passivating defects at the at the Si body / dielectric interface and enables significant threshold voltage tuning [2].

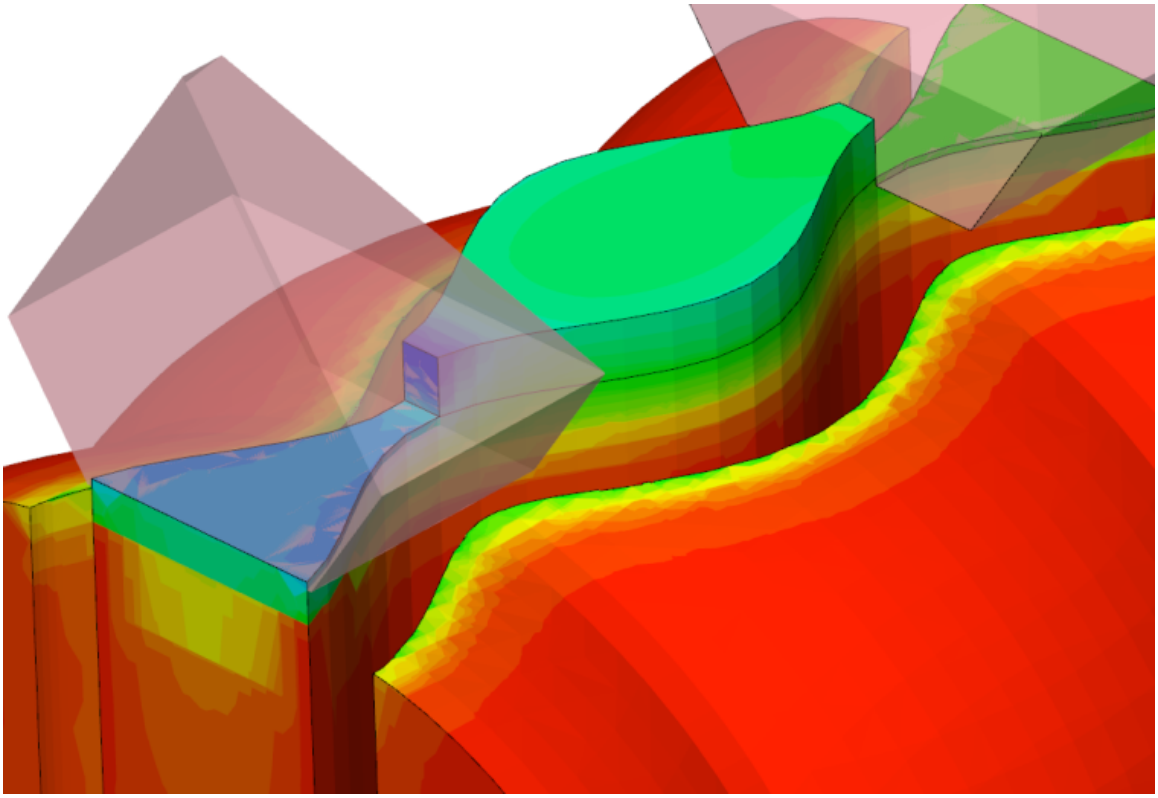


Figure 3.1 3D electron density graph of a pFET with applied side-gate bias. Red indicates a density of 1.1×10^{21} cm^{-3}. The LER considered here is a 'wide center' case as defined in Table 3.1.

In a case where the body edge is severely non-uniform due to LER, the side-gate follows the edges of the body. The normal electric field converges on convexities while diverging on concavities on the side surfaces, resulting in stronger accumulation of majority carriers in convex portions, electrostatically smoothing the channel pathway for the minority charge carriers (Figure 3.2).

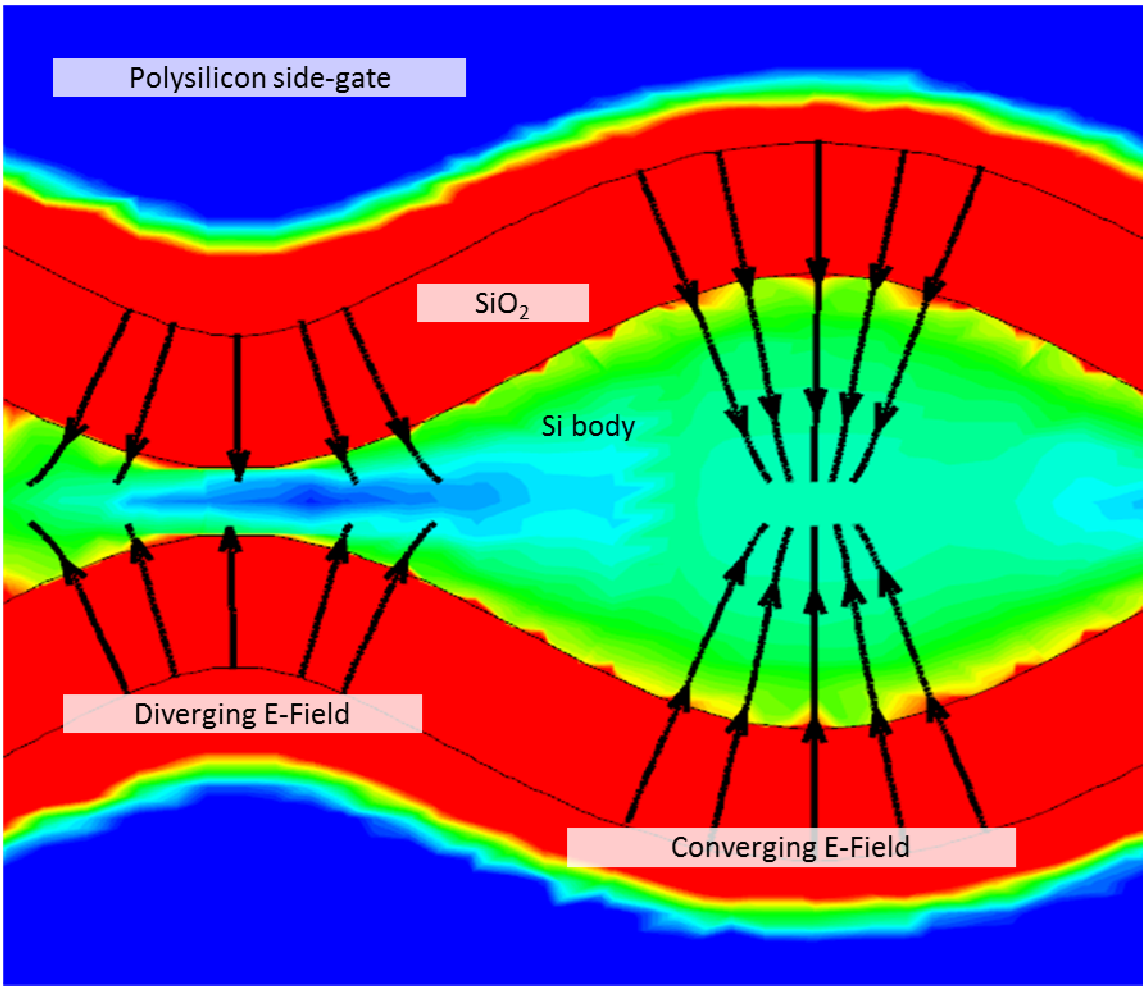


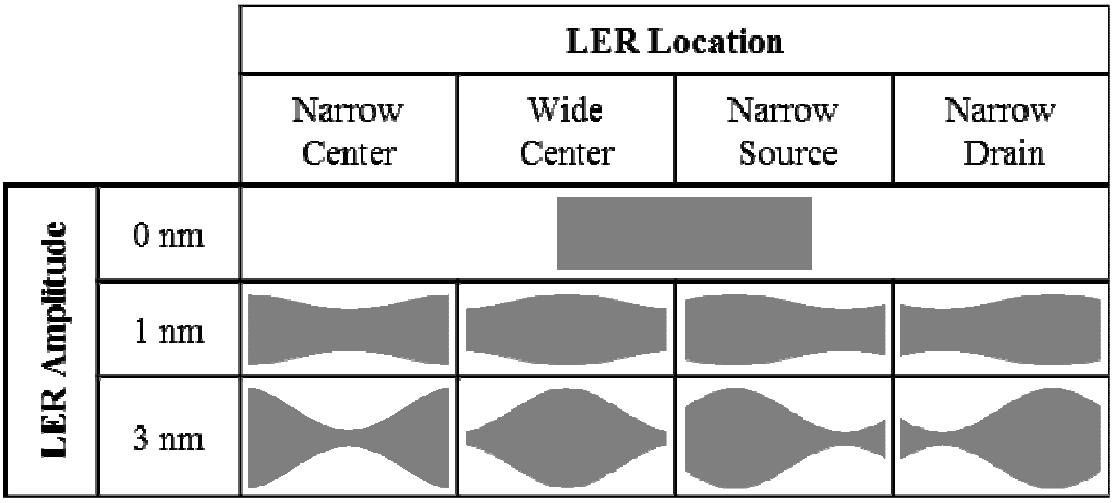
Figure 3.2. Cross-section of a simulated silicon body surrounded by a polysilicon side-gate. Arrows denote vector components of the electric field and color scale going from blue to red denotes electric field intensity from low to high. Diverging and converging electric fields (arrows) follow LER and electric field intensity is larger on wider regions of the body.

3.1 Simulation

Three-dimensional tri-gate n- and p-FET structures with LER were simulated to study the effect of the side-gate on the device characteristics, using Synopsys Sentaurus TCAD tools [39]. The simulation tools were used to create various sinusoidal LER cases

with varying amplitudes imposed on a nominal width (shown in Table 3.1). An idealized fabrication process was simulated, after which the electrical characteristics of the resulting devices were analyzed.

Table 3.1. LER amplitude and location combinations tested. n-type and p-type FETs with side-gates as well as control devices without side-gates were simulated for these 9 LER cases.



53 nm tall fins with LER were formed on a low-doped bulk silicon substrate. The top 3 nm portion of the fin is strongly coupled to the tungsten metal gate (top-gate). 5 nm HfO_2 was used as the top-gate dielectric. The bottom 50 nm were surrounded by the side-gate through a 2 nm thermally grown silicon dioxide side-gate dielectric (Figure 3.3). Control devices were also simulated in which the remaining 50 nm are surrounded by silicon dioxide (STI, shallow trench isolation). Source and drain regions were formed by faceted epitaxial growth. The gate length and nominal width for all simulated cases are 16 nm and 8 nm respectively.

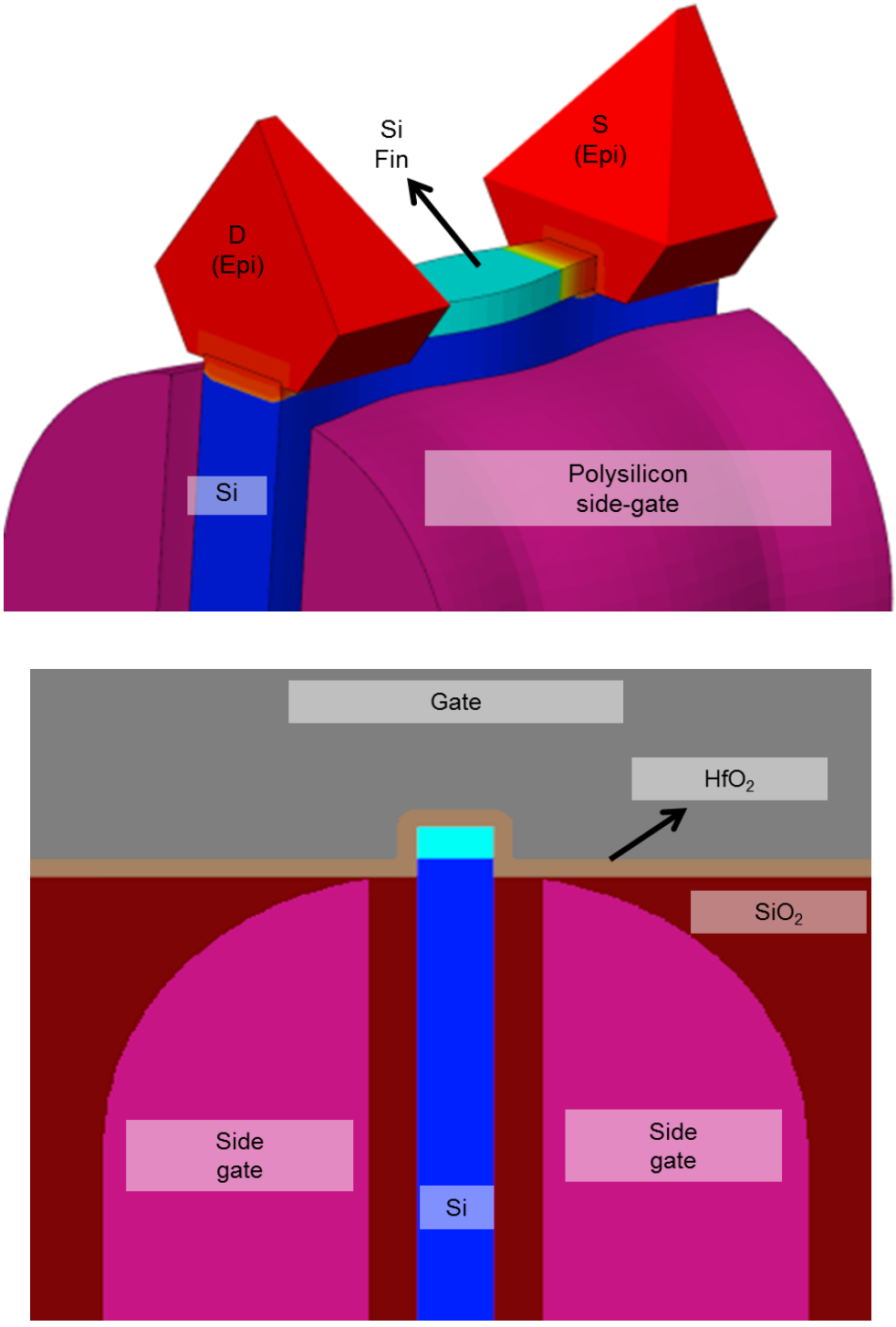


Figure 3.3. Si body with imposed sinusoidal LER of 1 nm amplitude. Gate and dielectrics are not shown (top). Vertical cross-section image at the FET channel center for a side-gated device. Top 3 nm (cyan) is covered by the gate (bottom).

3.2 Results

Transfer characteristics of the side-gated devices (in accumulation) show lower off-state current as well as improved short channel effects such as drain induced barrier lowering (DIBL), as previously reported for side-gated planar FETs [2] (Figure 3.4, Figure 3.5, and Figure 3.6).

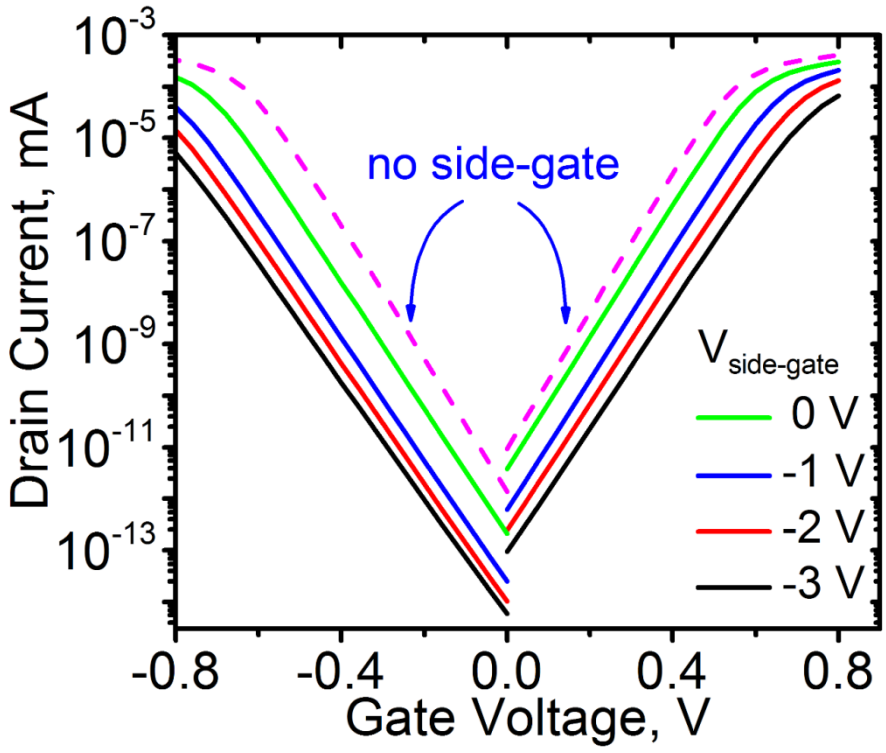


Figure 3.4. Transfer characteristics in log scale for an nFET and a pFET with wide-center LER (see Table 3.1) of 3 nm amplitude. Dashed lines are for control devices with no side-gate. Drain bias is 50 mV.

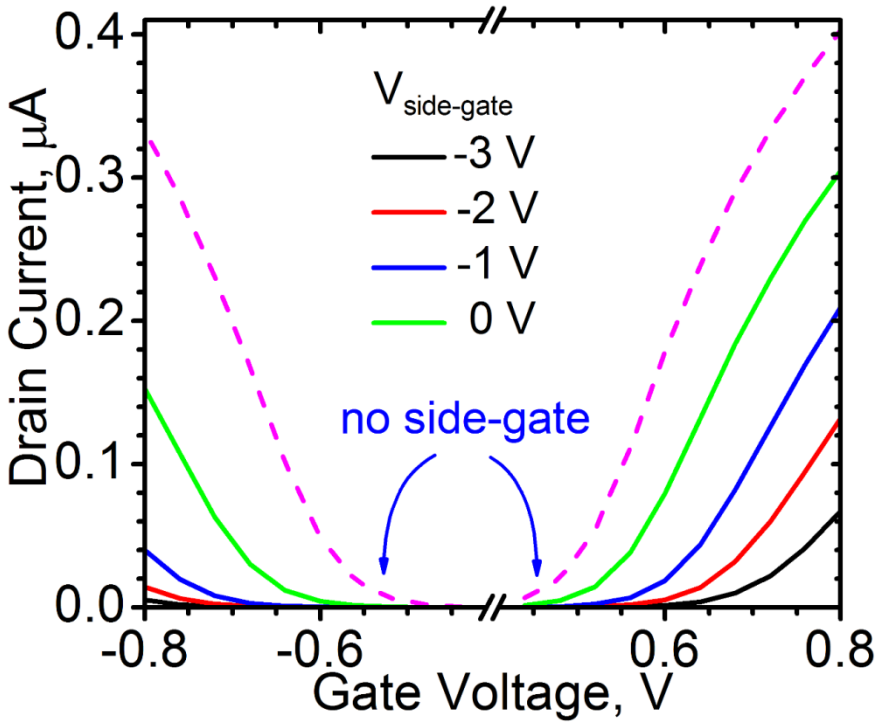


Figure 3.5. Transfer characteristics in linear scale (middle) for an nFET and a pFET with wide-center LER of 3 nm amplitude. Dashed lines are for control devices with no side-gate. Drain bias is 50 mV.

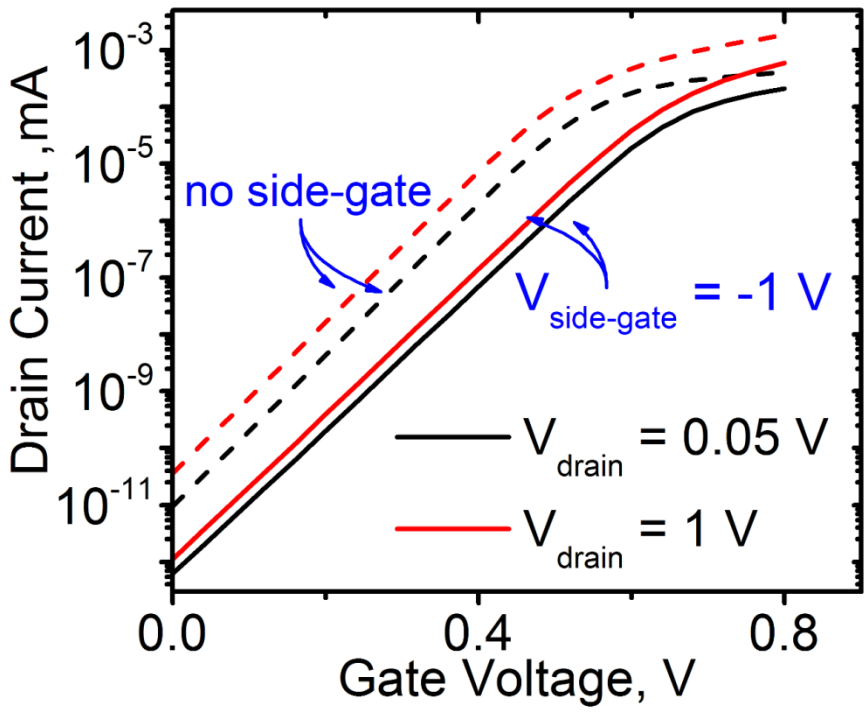


Figure 3.6. High and low drain bias transfer curves for the nFET device with no side-gate and side-gate bias of -1 V, showing reduced DIBL.

In applications where drain and source can be used interchangeably, asymmetric channel geometries due to LER can display different electrical characteristics and the use of a side-gate to accumulate the body may reduce this variation. Figure 3.7 illustrates this point by comparing a 'narrow source' and a 'narrow channel' pMOSFET, with and without a side-gate. A visible difference between the two transfer characteristics is observed in the no side-gate devices. With a side-gate bias of -1 V the two transfer characteristics converge, showing the effect of the side-gate in reducing the effect of the LER induced asymmetry, especially in the subthreshold region.

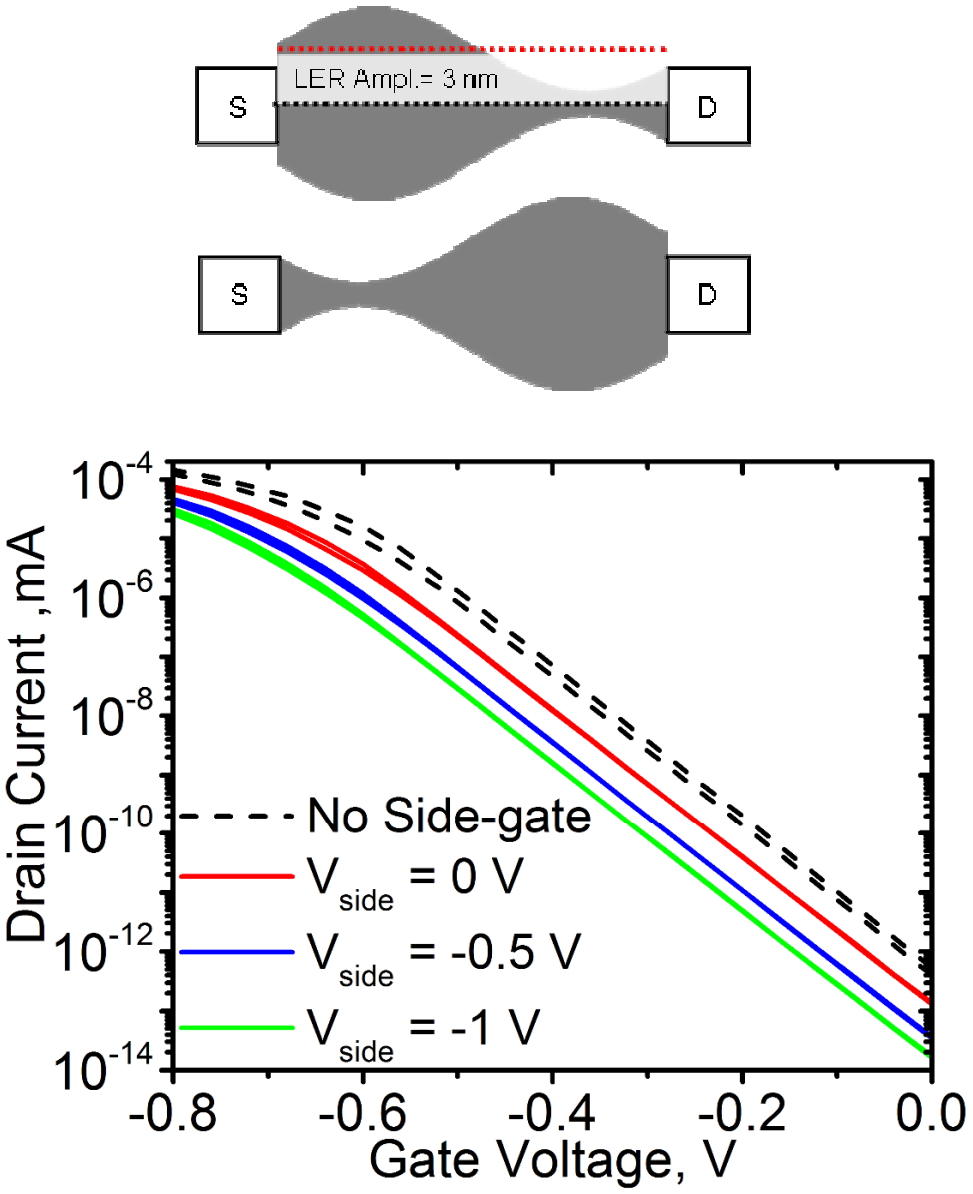


Figure 3.7. Transfer characteristics for a 'narrow source' and 'narrow drain' pFET cases with no side-gate, and with side gate bias of 0, -0.5 and -1 V. With the side-gate bias, the 'narrow source' and 'narrow drain' characteristics overlap showing effective reduction of the LER induced variability.

In addition to the enhancement of individual devices, accumulation of the device body is expected to improve device-to-device variations among a variety of LER

conditions. While the improvements are visible on devices with enlarged source or drain end (Figure 3.7), not all cases show an improvement. In essence, LER variations impact the device-to-device variations the most if the line width variations are at the source end since the source-barrier controls the injections of the charges into the channel. The variations in the rest of the channel are within an acceptable range as long as the average width remains approximately the same and therefore the impact of the side-gate is less noticeable.

In summary, body accumulation using a side-gate can be used as an electrostatic approach to reduce LER effects on devices where source and drain are desired to be used interchangeably. Also, low off-state current provides this technique some applications in low-power electronics. On the other hand, in this approach, an area penalty is inevitable due to the additional side-gate contact. The side-gate approach may be a viable way to reduce LER induced variability especially at the source-end. This approach is expected to be even more effective in planar devices due to increased coupling of side-gate to the MOSFET channel, versus fin- or tri-gate devices in which the geometry limits the proximity of the side-gate.

4 Fabrication of Accumulated Body MOSFETs

4.1 Overview of Fabrication Steps

The fabrication process of accumulated body n-channel MOSFETs followed a similar to that of conventional bulk transistors with SiO_2 dielectric and polysilicon gate. The overall process consists of six levels of photolithography: Active area (Si fin), side-gate contact pad, side-gate polysilicon via, gate, vias, and metal. Two of these levels (side-gate contact pad and polysilicon via) are additions to the conventional MOSFET fabrication flow. Main steps of the fabrication are summarized in Figure 4.1

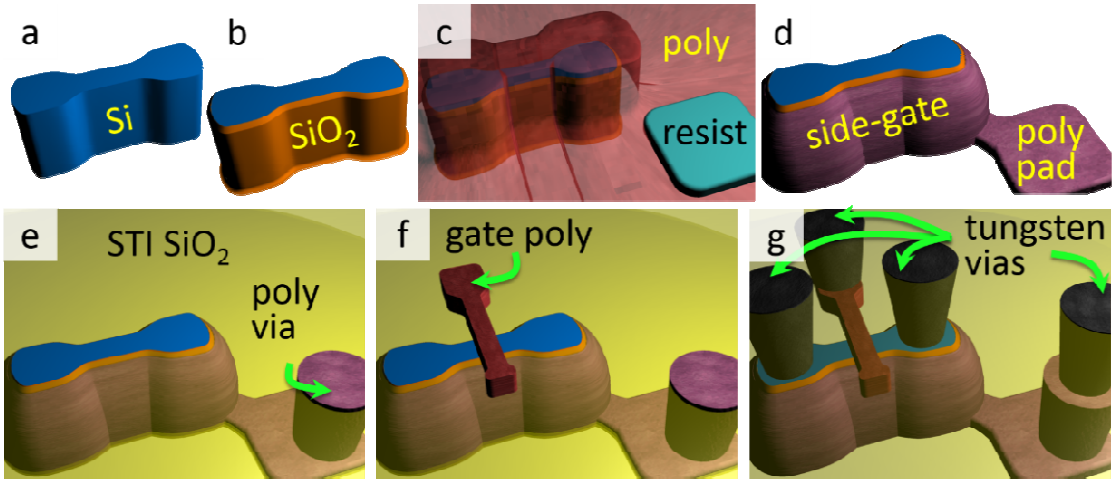


Figure 4.1. Drawings showing major fabrication steps for accumulated body MOSFETs. (a) Si fin definition (final body doping ~$1\times10^{17}cm^{-3}$, p-type). (b) 9-nm side-gate dielectric growth. (c) 50 nm in-situ doped p+ polysilicon film deposition and photoresist to protect polysilicon pad. (d) spacer-like side-gate structure after the polysilicon reactive ion etching (RIE). (e) STI SiO_2 deposition, STI planarization, and forming of polysilicon via for electrical access to side-gate from the top of STI. (f) FET gate formation (3.9 nm oxidation for gate dielectric, SiO_2 and Si_3N_4 spacer formation, source/drain formation via ion implantation and nickel silicidation are not shown) (g) Tungsten via formation (middle of line via liner, and subsequent copper contact metal formation steps are not shown).

The details of the mask design can be found in Appendix 7.3.1.

In the fabrication steps to form the side-gate, electrical contact between the side-gate contact pad and the side-gate was obtained through exploiting the fact that RIE slows down for tighter pitches (Figure 4.2), providing some flexibility in overlay accuracy.

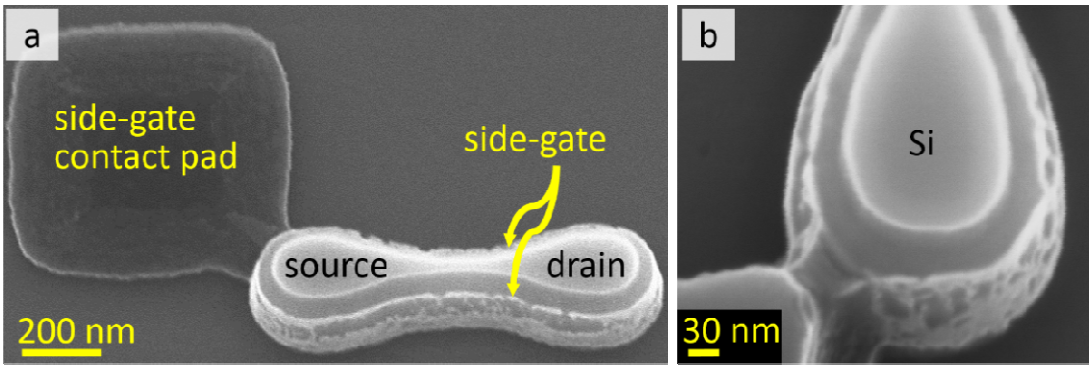


Figure 4.2. SEM micrograph of Si fin and the surrounding side-gate with the polysilicon contact pad connected to it. Design W x L = 120 nm x 200 nm.

The introduction of polysilicon via serves in bringing the side-gate contact to a comparable height with the active region. As a result, the RIE process that forms the tungsten vias to all contacts does not require much modification or risk etching into active area while making contact to the side-gate contact pad.

Choosing in-situ doped polysilicon as the material for this via and the side-gate, as well as the fact that the side-gate is encapsulated within the STI ensure that front-end-of-line processes can be safely used for subsequent fabrication steps. By the same token, FETs with the added side-gate formation steps are still compatible with high-κ dielectric

and metal-gate processes, as well as stressors and SiGe source/drain, although these techniques were not employed in the fabrication.

The final design had nMOSFETs with a wide range of dimensions. Estimated channel widths (W_{est}) and estimated physical gate lengths (L_{est}) were extracted through the extrapolation of channel resistance to determine an offset value which was subtracted from design dimensions. Extracted values vary from $W_{est} \times L_{est}$ = 13 nm × 37 nm to $W_{est} \times L_{est}$ > 500 nm × 500 nm with many dimensions in between.

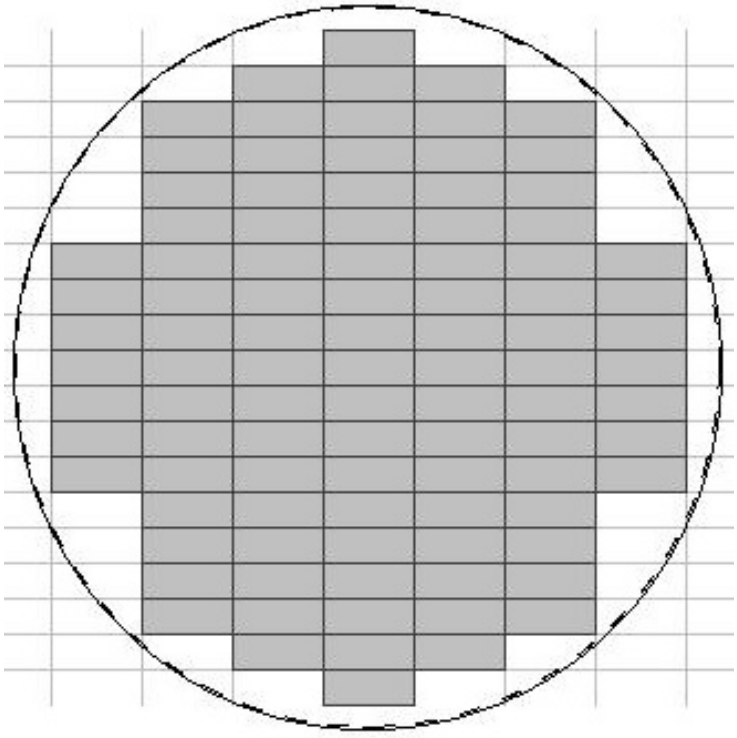


Figure 4.3. Wafer map showing the placement of dies on an 8" wafer. Gray dies are complete dies with a total count of 97. The rest are still printed although they are not full dies.

The fabrication uses an 8” process with 193-nm lithography available at IBM Research Microelectronics Research Laboratory (MRL) at Yorktown Heights, NY. Entire

process except for electrical characterization was conducted at the mentioned facility. The 8” wafers, given the die dimensions of 30 mm x 10 mm, can fit 97 complete dies. The rest of the wafer however was still printed with partial dies. ~2 mm margin was left on wafer edges.

4.2 Active Region Definition

Active region is a mesa structure that contains the source, drain and channel of the MOSFET. Modern MOSFETs use a shallow trench isolation (STI) process where a relatively deep etch into silicon separates active levels of close-by transistors [4, 5, 9].

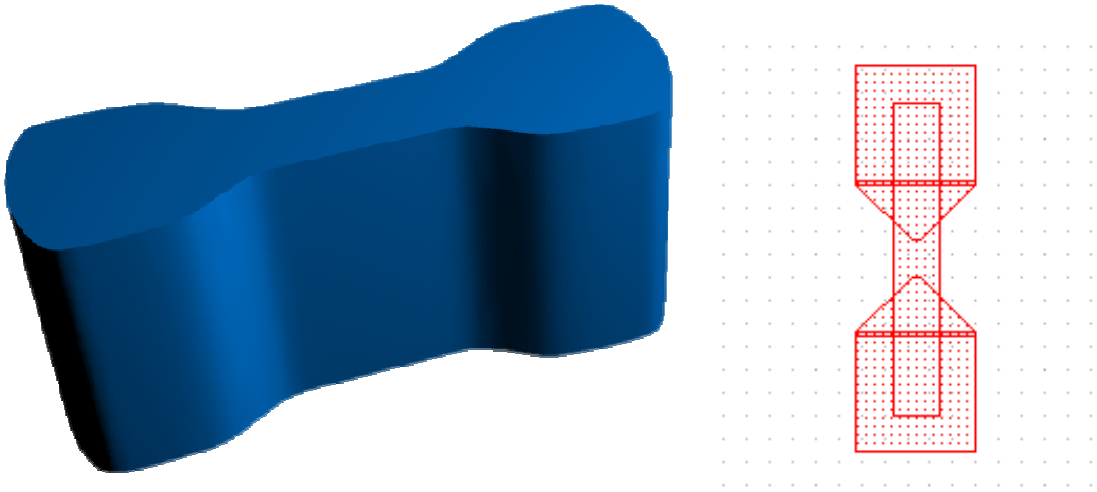


Figure 4.4. Three-dimensional drawing of active layer after mesa definition (left) and layout appearance of the active (RX) level (right).

After obtaining wafers with resistivity values of ~1.5 Ω.cm, an initial three-level ion implantation was conducted to set the final p-type doping level of approximately $1\times10^{17}cm^{-3}$.

4.2.1 Photolithography and Reactive Ion Etching

To serve as the hard mask and to provide polish stop, pad SiO_2 followed by a Si_3N_4 layer was deposited on the wafer. On top of the nitride layer, a tri-layer stack was formed of a NFC-like polymer, a low temperature SiO_2, and the photoresist. A 193-nm ASML scanner was used to pattern the active (RX) level. After patterning, reactive ion etching was used to form mesa structures.

4.2.2 Mesa Thinning through Oxidation

In order to obtain ultra-narrow structures, a thinning process through oxidation of Si mesas was employed. It was seen that vertical mesa sidewalls oxidize faster than the floor and corners of Si, causing concavities in the sidewall. Furthermore, the pad oxide enlarges, separating the nitride pad from Si mesa. Figure 4.5 shows a sample of such sidewall oxidation issue.

Although there are certain ways in the literature to mitigate some effects of this issue [40], extreme oxidation was abandoned for the last generation of wafers. This is despite the fact that this effect can be used to obtain nanowire structures by pinching the concavities of the mesa sidewalls (see Figure 4.6).

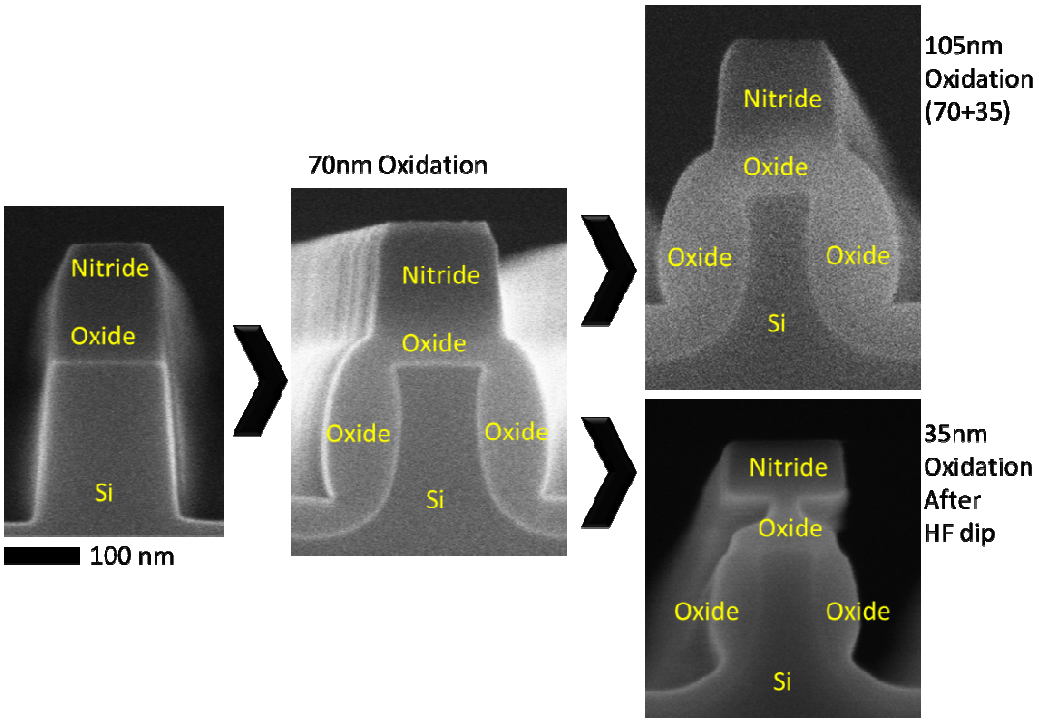


Figure 4.5. Oxidation of a mesa structure. Oxidation amounts are based on known floor oxidation rates for the furnace as measured in blank monitor wafers (W_{design} = 200 nm).

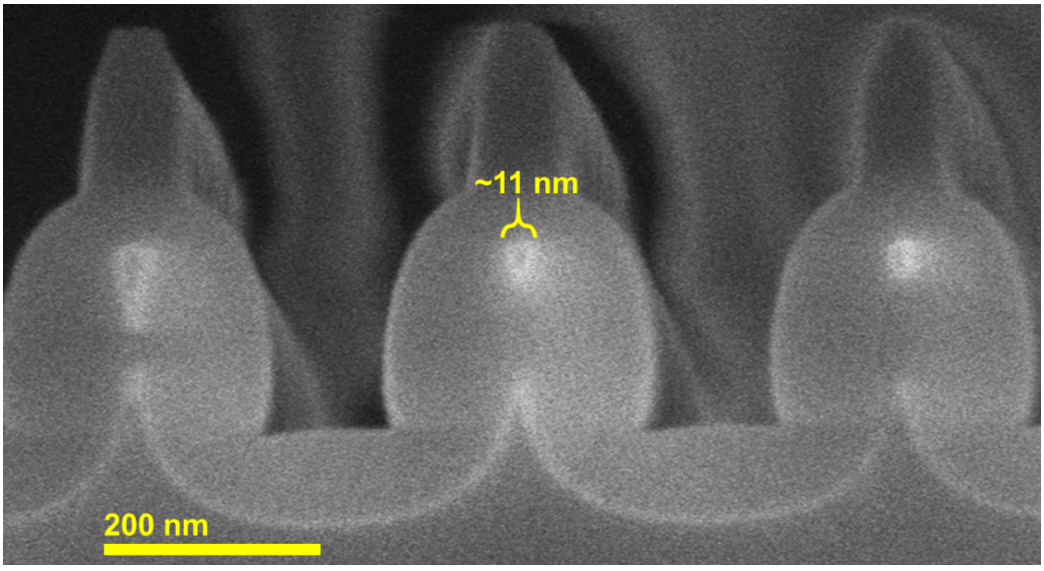


Figure 4.6. Nanowire structures with an approximate diameter of 11 nm can be formed by extreme oxidation of narrow mesa structures. (W_{design} = 60 nm, Oxidation for 105 nm floor rate, lot name: 5GRXTHIN2K48)

4.3 Side-Gate Formation

Side-gate is the most unique part of the process flow. This is because the rest of the processes (except for polysilicon plug formation) are standard processes in CMOS microfabrication.

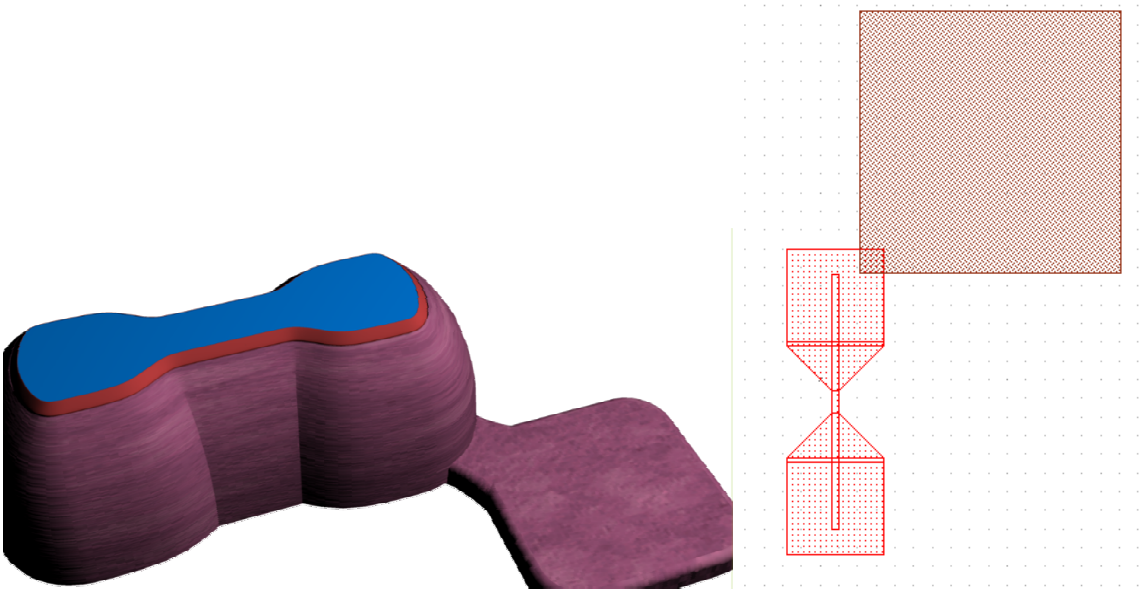


Figure 4.7. Drawing of a Si mesa surrounded by the side-gate structure (left). Layout drawing showing active (RX) and side-gate contact pad (SG) levels.

4.3.1 Side-Gate Dielectric

Side-gate dielectric is designed to be thicker than the gate dielectric to avoid an over-powerful side-gate to channel coupling. 9 nm of SiO_2 was grown using an RTP oxidation process (Figure 4.8). In order to avoid native oxidation after this step, coordinating it with the Coordinating this step to be right before the subsequent side-gate polysilicon deposition is essential in avoiding native oxidation.

Another split of wafers (lot 5GATEINT3K51, wafers 4 and 5) is designed to have a $SiO_2/Si_3N_4/SiO_2$ (ONO) stack (4 nm inner SiO_2, 10 nm Si_3N_4, 3 nm outer SiO_2) for a side-trapping flash memory device. Due to process-related issues, electrical contact to devices is not established reliably, thus no electrical data from them is available.

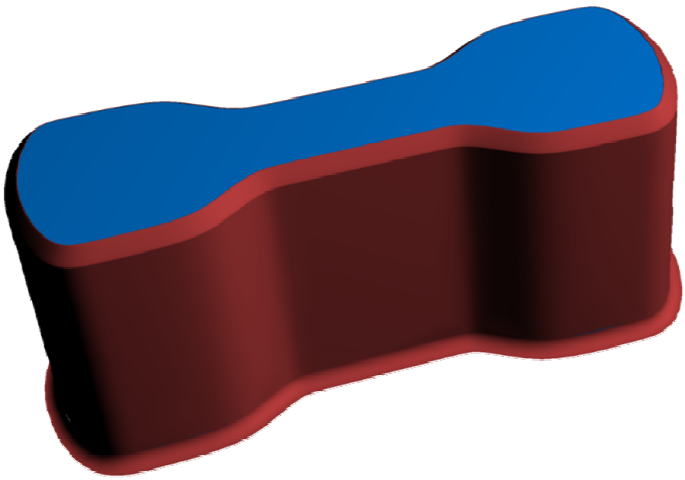


Figure 4.8. Drawing of Si mesa with side-gate oxide. Oxidation on top of the mesa is not shown, although it is present.

4.3.2 In-situ Doped Polysilicon Deposition

Side-gate polysilicon was chosen to be highly doped to reduce any side-gate depletion effects.

In order to uniformly dope a deposited film of polysilicon with high topography (Figure 2.1), an in-situ doping approach needs to be taken [18].

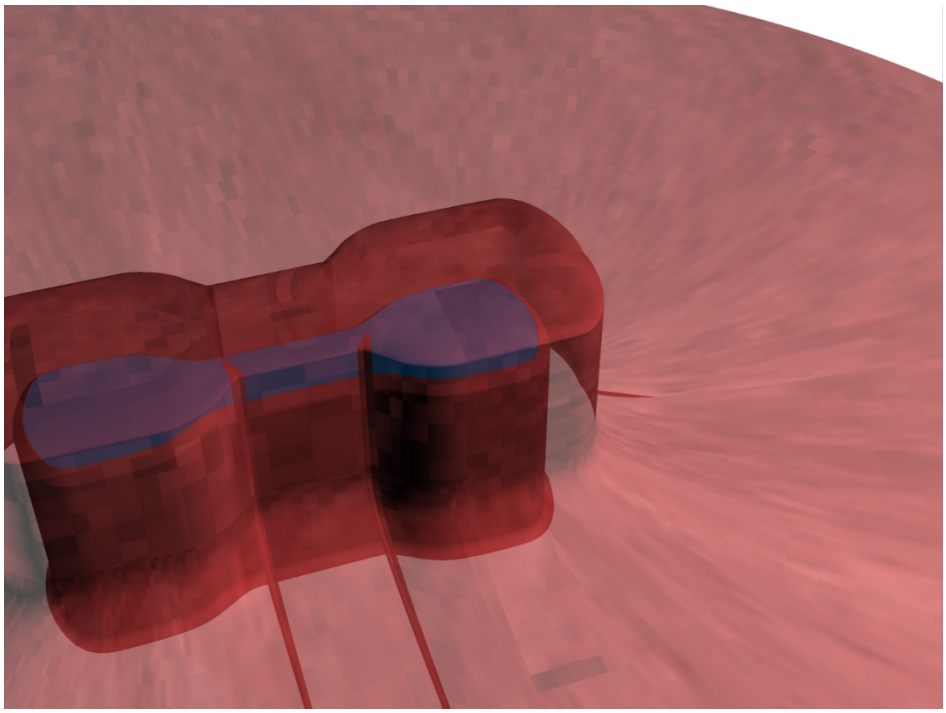


Figure 4.9. Drawing of deposited polysilicon film on Si mesa.

An in-situ Boron doped polysilicon film was deposited with a thickness of 50 nm at 630 °C. A 5-second anneal at 1050 °C was conducted in an RTP chamber for dopant activation. The resulting film has a sheet resistance of ~2 Ω.cm which corresponds to a high doping level ($1x10^{19}$-$1x10^{20}$ cm^{-3}).

4.3.3 Photolithography for Side-Gate Contact Pad

Side-gate is a thin (~50 nm) vertical structure on the sidewalls of Si mesa, so making successful electrical contact to it is a challenge. To overcome this, a side-gate contact pad is designed to be placed on one corner of the side-gate. In this scheme, after polysilicon is deposited for the side-gate, side-gate contact pad (SG) level is defined photolithographically (Figure 4.10).

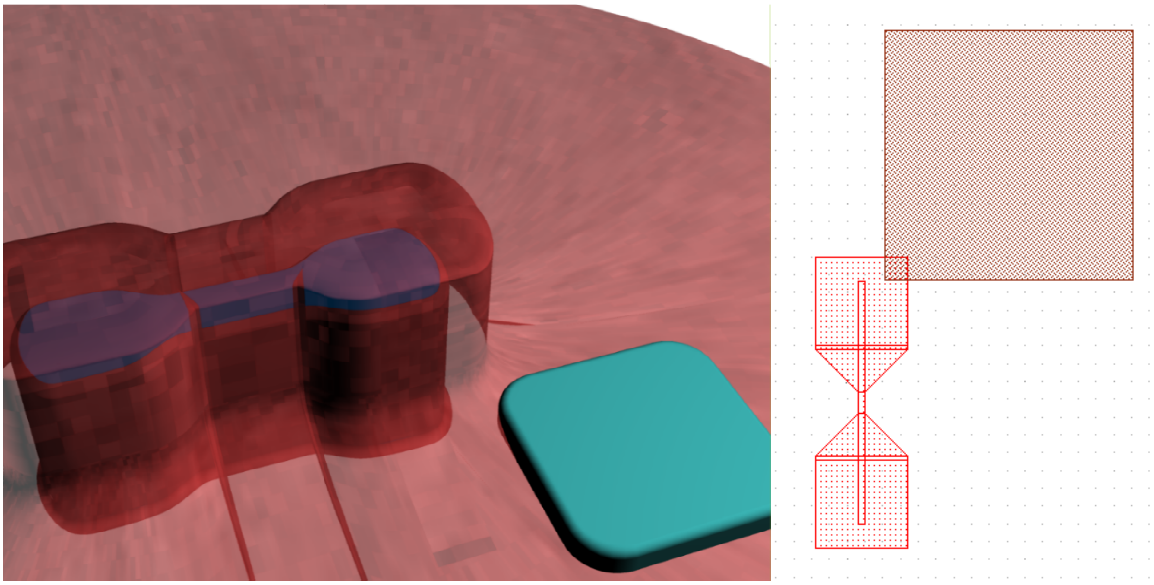


Figure 4.10. Drawing showing the photoresist for side-gate contact pad (left). The layout showing the SG level in the corner of active (RX) level (right).

4.3.4 Spacer Reactive Ion Etching for Side-Gate Formation

Side-gate formation can either be done through polishing down the top portion of the deposited polysilicon, along with the top of Si mesa [18], or through a spacer etch. In the latter, the tapering shape helps in reducing gate to side-gate capacitance.

Spacer RIE process was developed to have three steps: The first step is SiO_2 breakthrough, which is aimed to etch away any native SiO_2 buildup on polysilicon. The second step is longer and involves a slow silicon etch. When side-gate oxide is exposed on top of Si mesa and on the floor of the wafer, the third step, which is a 5-second overetch step is taken to clear out the floor altogether (Figure 4.11). The way to measure the clearing of the oxide is to watch for the inflection points of a measured $SiBr_4$ vs. time

graph from the RIE chamber. First inflection point (top knee) occurs when the oxide on top of the Si mesa is exposed. The final point (bottom knee) occurs when the floor clears.

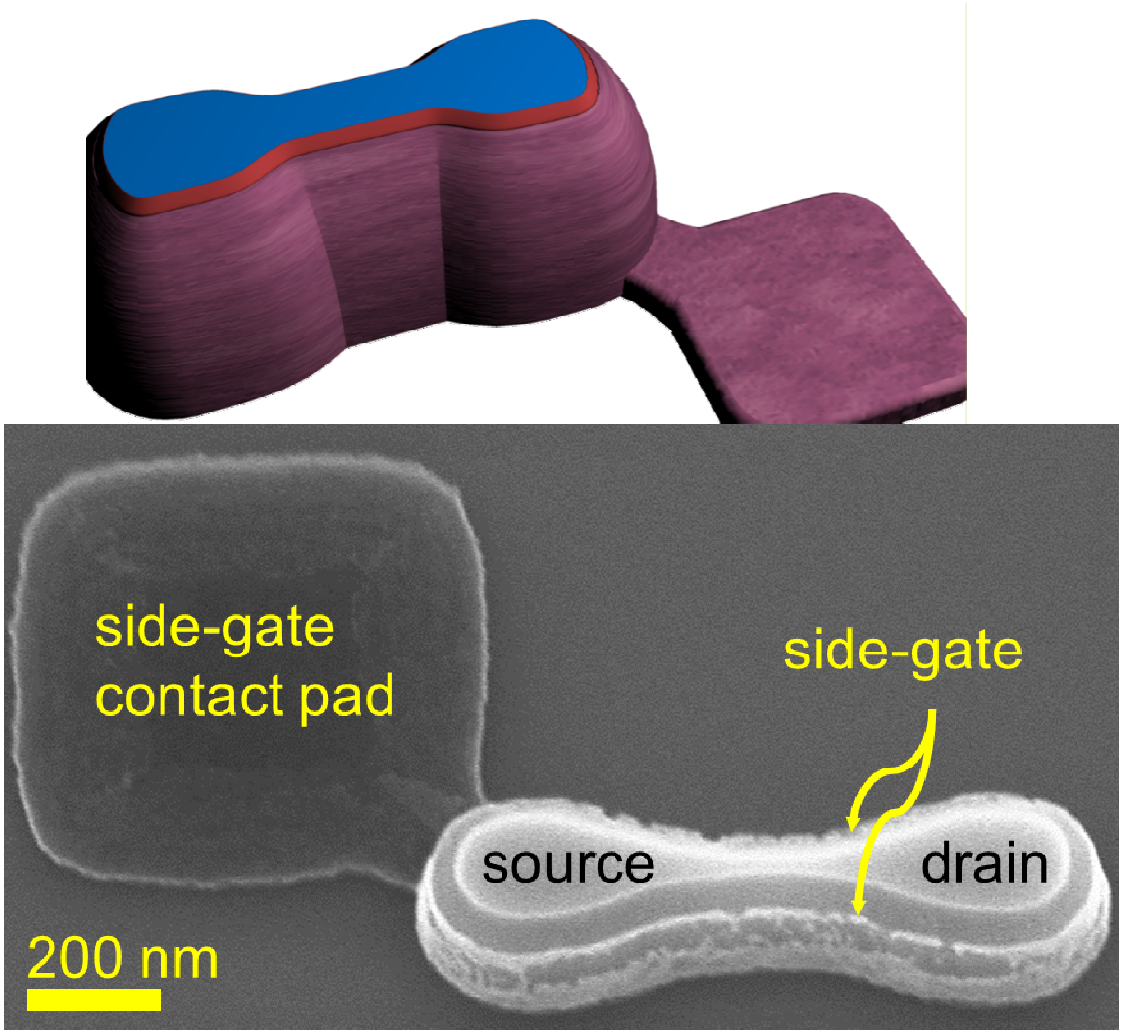


Figure 4.11. Drawing of a side-gated Si mesa with polysilicon contact pad attached in one corner (top). SEM micrograph of a Si mesa with the side-gate structure (lot: 5GATERX2I40, wafer 7) (bottom).

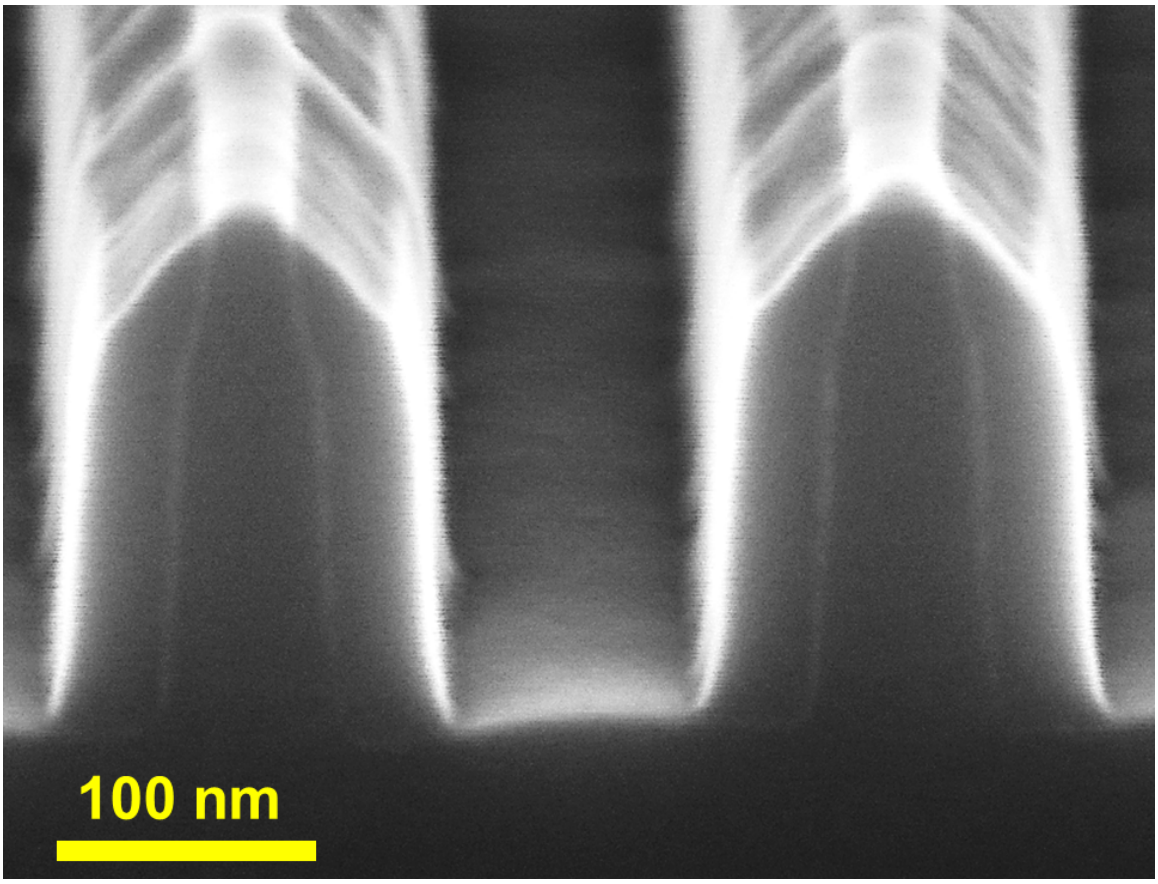


Figure 4.12. Cross-section SEM micrograph of side-gate on Si lines. The top has the Si_3N_4 cap, unlike the latest generation whose cap is removed before this step. (lot: 5GATEPSPCJ23, wafer 4).

4.4 Polysilicon Plug Formation

Polysilicon plug is essentially a preliminary via process that is front end of line compliant by using polysilicon as the fill material. Although regular via process is designed to handle some level of topography, namely the height difference of Si mesa and gate poly, the side-gate contact pad presents another challenge by having a height

difference of ~300 nm between gate silicide and side-gate contact pad (100 nm gate poly + ~250 nm Si mesa height - ~50 nm contact pad (side-gate poly) thickness).

Therefore, a preliminary via that is called ‘polysilicon plug’ is devised to bring the level of contact pad close to the level of source and drain contacts.

4.4.1 Shallow Trench Isolation Deposition and Planarization

The first step in having the polysilicon plug is to deposit high density plasma (HDP) oxide of 800 nm, densified by annealing at 900 °C for 60 minutes in N_2 ambient in a furnace.

The deposited STI oxide is then planarized to remove ~440 nm, leaving ~360 nm SiO_2 as measured from the bottom of Si mesa. This planarization step is a way to ensure that the following photolithography step will work on reduced topography.

4.4.2 Photolithogrophic Definition and Reactive Ion Etch

Poly plug (IH) level of the mask layout is a multi-purpose level that covers the poly plug, as well as the irrigation holes for DNA transistors. In the context of side-gated transistors, the level was exposed to have a relatively large via hole above the side-gate contact pad.

A timed RIE process is used for removing the STI SiO_2 and to connect the top of STI to the side-gate contact pad.

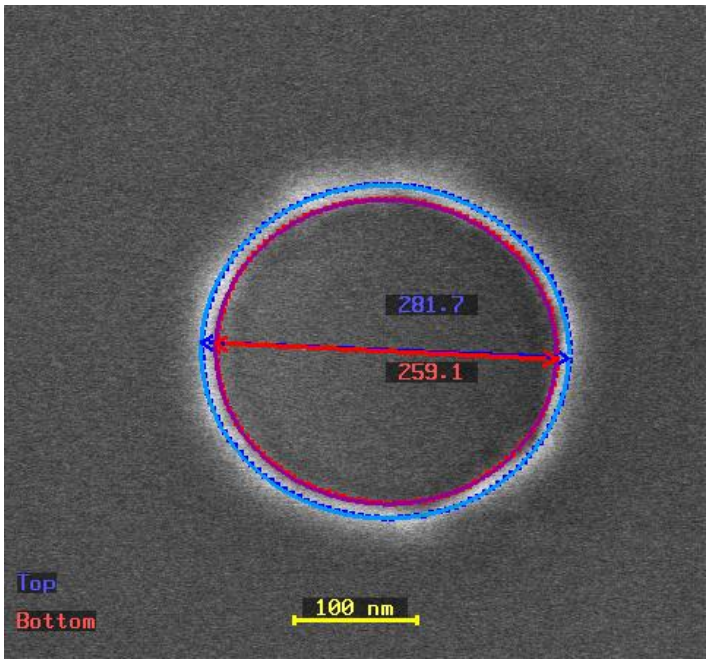


Figure 4.13. Measurement image from the VeraSEM 3D system after polysilicon plug (IH) level photolithography. The design dimension of the via is 300 nm.

4.4.3 In-situ Doped Polysilicon Deposition and Planarization

To fill the via hole, 250 nm of in-situ doped polysilicon of the same doping concentration as the side-gate and the side-gate contact pad was deposited. Afterwards, a chemical mechanical polishing (CMP) process is used to remove top portion of the polysilicon. A second CMP step is then taken to recess the STI further down, along with the polysilicon vias (Figure 4.14).

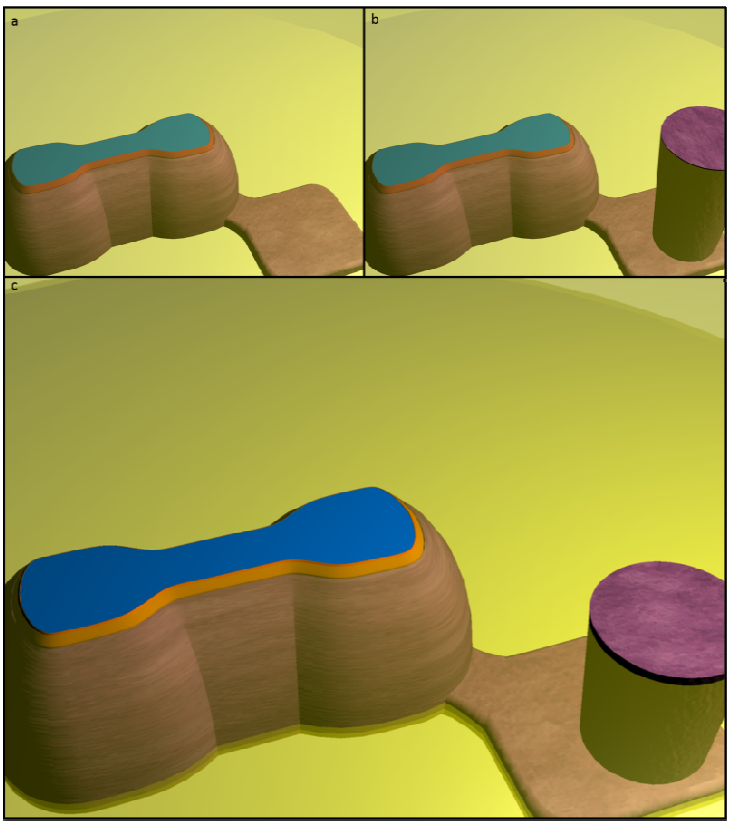


Figure 4.14. Drawing of fabrication steps of a side-gated Si mesa with STI SiO_2 and polysilicon plug (via) for side-gate contact. STI deposition and planarization (a), Poly plug definition and planarization (b), final planarization of poly plug with STI, and oxide recess with diluted HF (c).

4.5 Gate Stack and Ion Implantation

The process for accumulated body transistors is compatible with high-κ, metal gate processes, but for the sake of simplicity, polysilicon gate and a SiO_2 gate dielectric were used as the gate stack.

4.5.1 Shallow Trench Isolation Recess

Depending on what is above Si mesa, STI recess takes on two splits: If there is a nitride cap, and consequently polysilicon fingers under it, a silicon-etching CMP is conducted to remove some part of Si mesa along with the STI and poly plug. If no nitride is present, a 100:1 diluted HF process is used to remove the STI to expose Si mesa.

4.5.2 Gate Stack

For gate dielectric, 3.9 nm of SiO_2 was grown on Si. This growth is preceded by a modified Huang (RCA) clean with a short DHF step to remove native oxidation. After the oxide growth, 100 nm of polysilicon is deposited. These three steps are coordinated to be immediately one after the other, to minimize native oxidation and contamination issues.

The polysilicon gate is doped using ion implantation with phosphorus. An in-situ doping is not conducted for the gate because the topography of the wafer at this stage is flat enough for ion implantation. Afterwards, a tri-layer approach was taken to handle the photolithography of the gate (PC) level (see section 4.2.1 for details of the tri-layer method).

In order to obtain short gate lengths, some resist trimming (with O_2 plasma) is conducted within the RIE chamber before starting the etching of the gate poly in the same chamber. RIE stops on gate oxide through automatic detection.

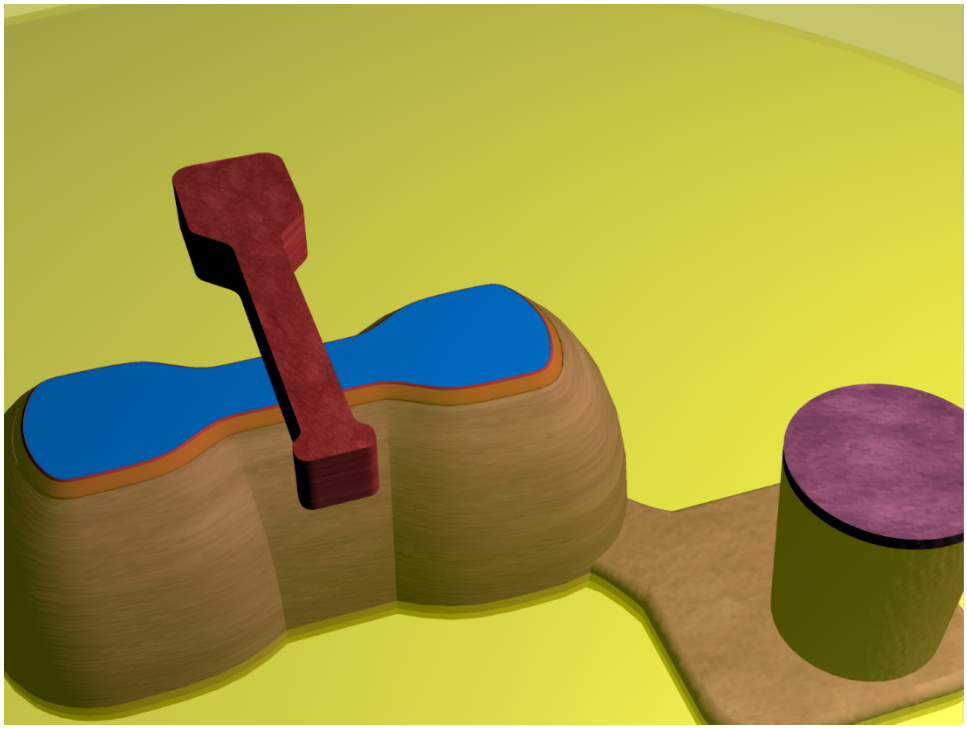


Figure 4.15. Drawing of an accumulated body transistor after gate formation.

4.5.3 Spacers

A 3.5-nm SiO_2 layer, followed by a 17 nm of Si_3N_4 was deposited and then a RIE step to etch the nitride and the oxide is performed to form spacer structures around the polysilicon gate.

4.5.4 Ion Implantation for Source and Drain Formation

Before arsenic dopants were introduced, an ion implantation step with Ge was conducted to amorphize the top of source and drain, so that phosphorus does not 'tunnel'

into the single crystalline mesa. Afterwards, arsenic ion implantation with an energy of 25 keV and a dose of $3x10^{15}$ cm^{-2} was conducted for source and drain formation. A 5-second anneal at 990 °C was used to activate the dopants.

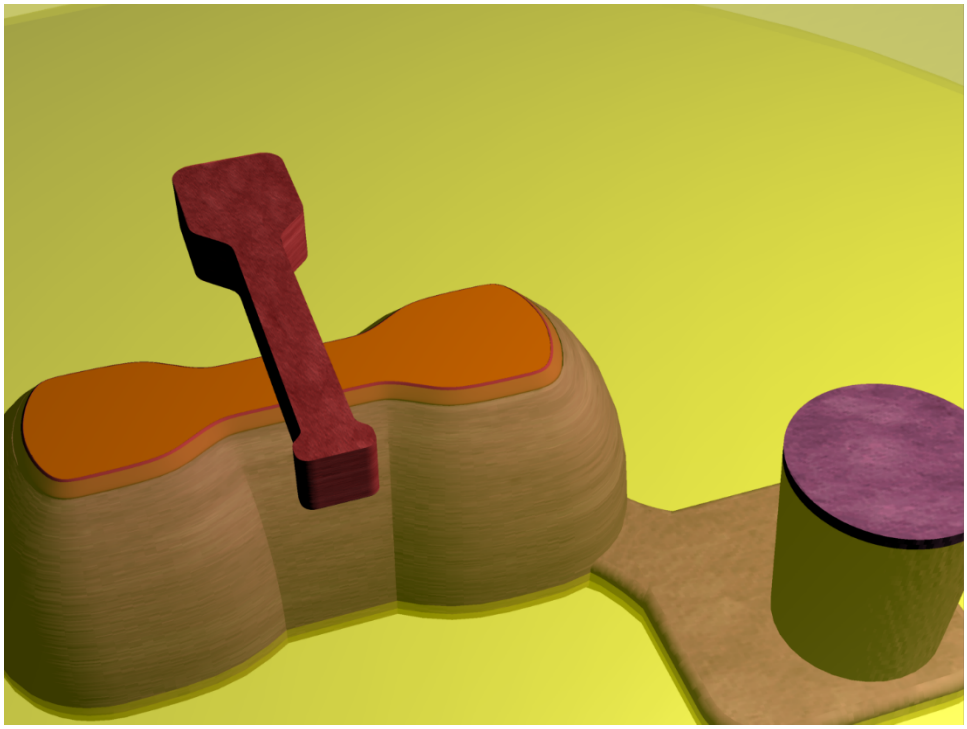


Figure 4.16. Ion implantation step to form source and drain regions also increases the doping of the gate. On the other hand, it counter-dopes polysilicon plug.

4.6 Back-End-Of-Line Integration

4.6.1 Self-aligned Silicide

Nickel and TiN were deposited and then annealed at 400 °C for 5 seconds in an RTP chamber to form self-aligned silicide (salicide) layers on source, drain, gate and side-gate contacts.

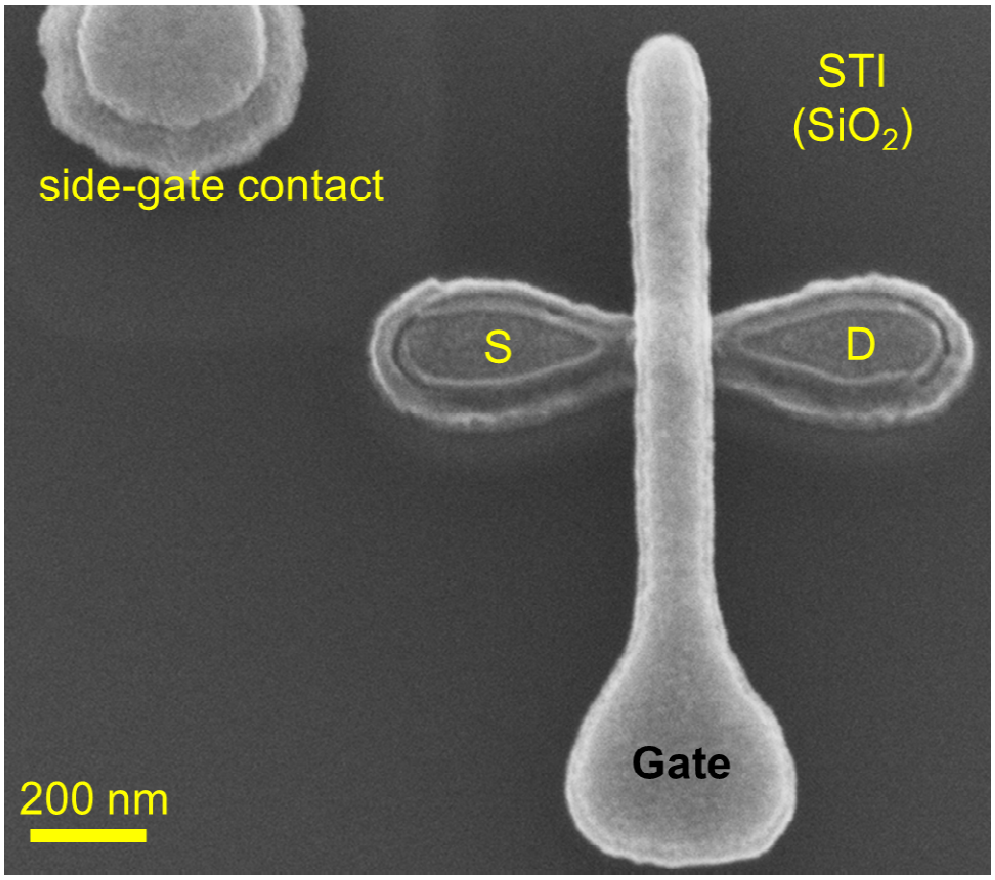


Figure 4.17. SEM micrograph showing silicided terminals of an accumulated body FET.

4.6.2 Vias

After silicidation, a 40-nm low-stress nitride was deposited to serve as an etch stop for via level RIE. A 500-nm low temperature SiO_2 layer was then deposited as the inter-level dielectric (ILD). To reduce topography for the upcoming via level (CA) photolithography, the wafers went through a CMP process which removes ~200 nm of ILD.

Via (CA) level photolithography leaves via holes exposed, where the subsequent RIE step removes 300 nm ILD and the 40-nm silicon nitride layers, stopping on silicide.

A middle-of-line (MOL) liner metal stack was then deposited as a Ti/TiN stack. The remaining was filled with tungsten (W) and then polished to clear excess tungsten. A clean step with diluted HF (100:1) and ammonium hydroxide is then conducted, followed by a touch-up tungsten RIE process to make sure there are no shorts between vias.

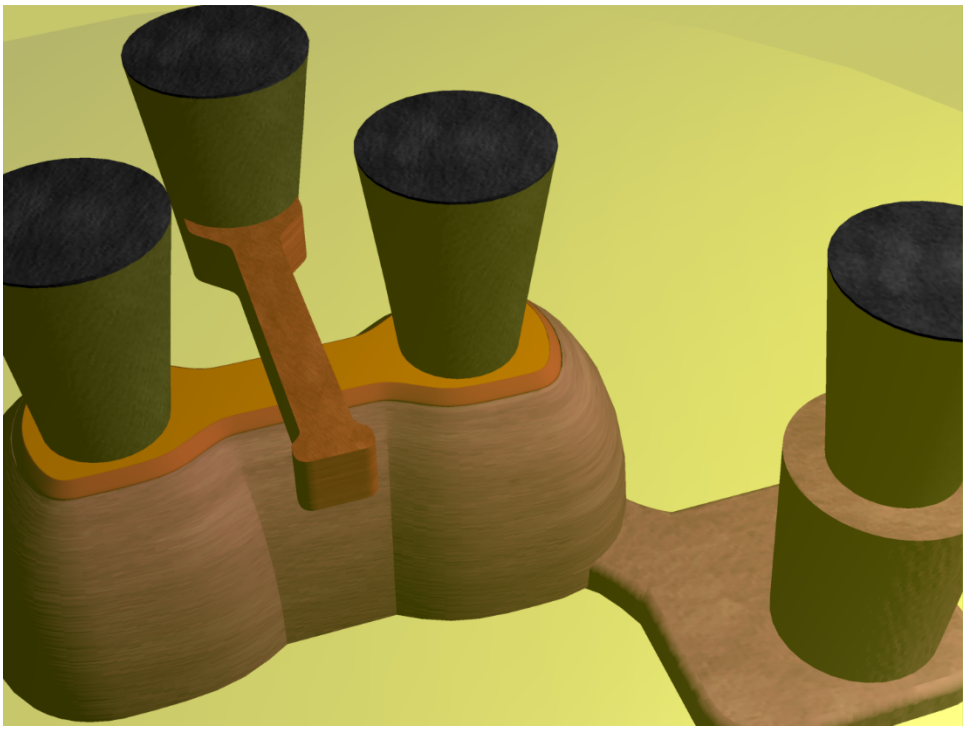


Figure 4.18. Drawing showing vias placed on gate, source, drain and side-gate terminals.

4.6.3 Copper Interconnects

The only interconnect level in the mask (M1) was exposed to define trenches on a 165-nm low temperature SiO_2. After etching SiO_2 down to vias, a seed liner layer was deposited in the trenches. Afterwards, the wafer was copper-plated and then polished to

clear the areas outside the trenches. Upon annealing, the seed metal encapsulates Cu to avoid contamination.

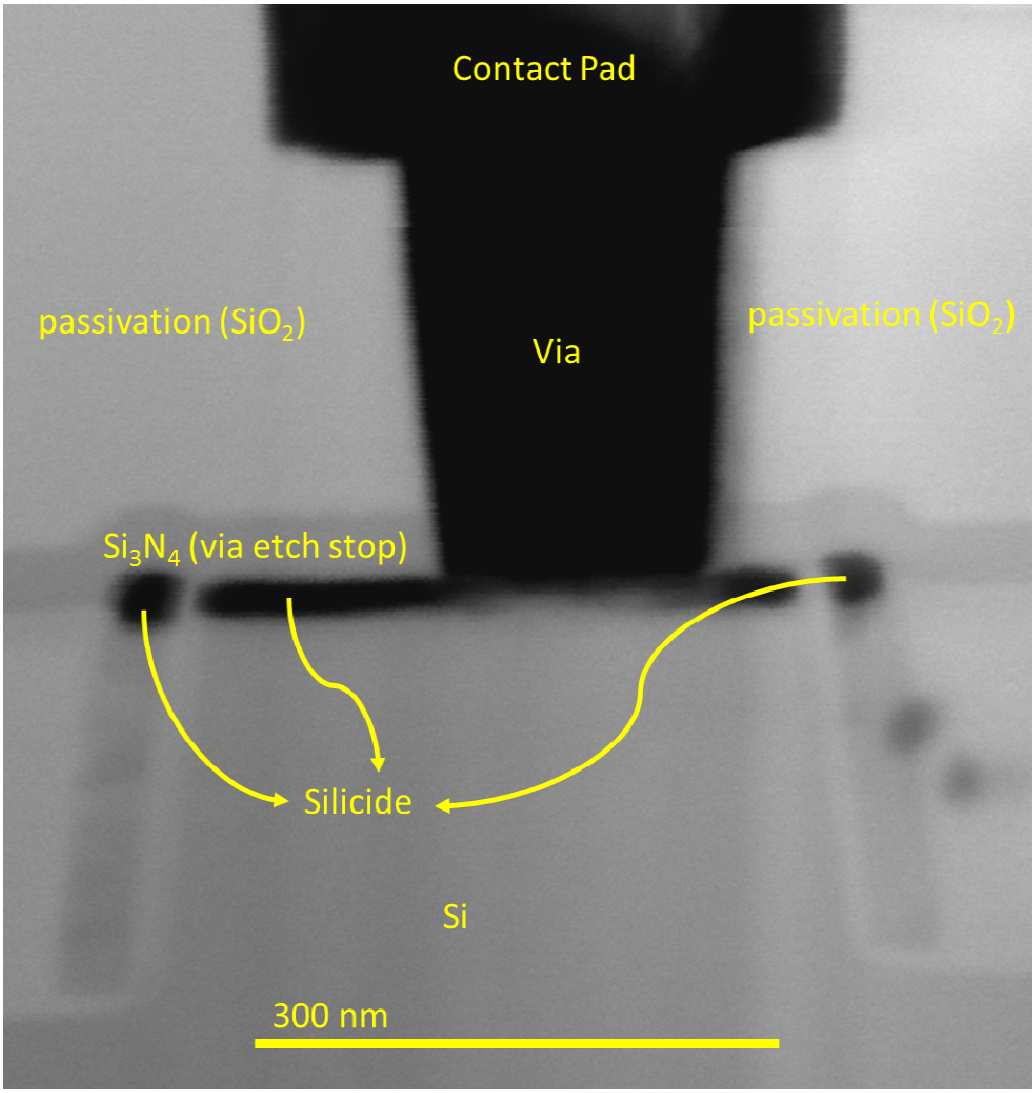


Figure 4.19. Scanning Tunneling Electron Microscope (STEM) image of an accumulated body MOSFET's cross section across its contact pad, showing via and the copper interconnect.

5 Electrical Characterization of Accumulated Body MOSFETs

Electrical characterization of wafers was conducted at the University of Connecticut Nanoelectronics Laboratory, using a microprobe station with an HP 4156C parameter analyzer.

5.1 Narrow and Short FETs

Transfer characteristics for narrow accumulated body nFETs ($W_{est} \times L_{est}$ = 17 nm × 37 nm) display strong V_T response to the V_{side} in a relatively small V_{side} window, due to accumulation of the body by the side-gate. The same effect helps improve subthreshold slope (SS) and drain induced barrier lowering (DIBL), when comparing the three cases where side-gate contact is floating, where it is grounded and where it is biased at -1 V (Figure 5.1).

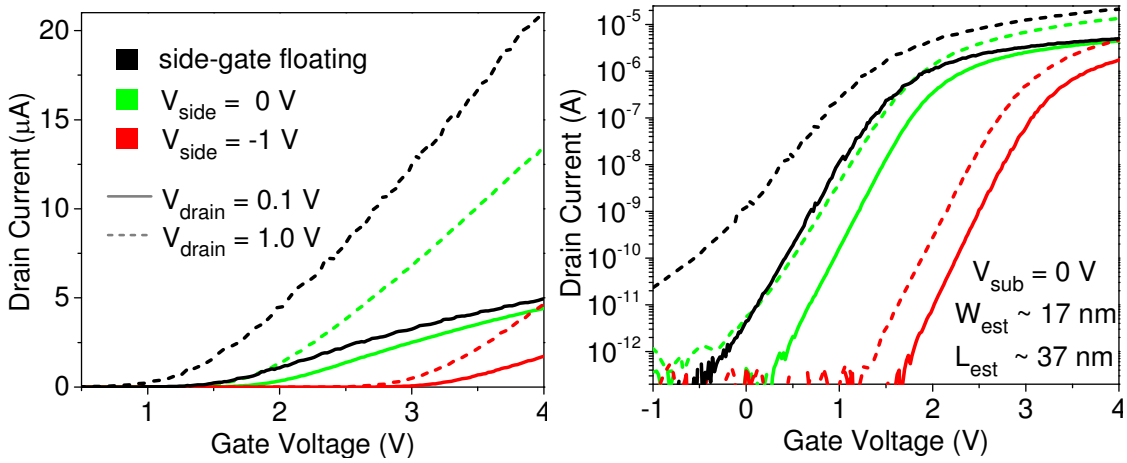


Figure 5.1. Transfer characteristics (linear scale on left, log scale on right) of a short and narrow accumulated body FET, comparing low and high drain bias conditions when the side-gate is a floating contact, and when it is biased. Strong threshold voltage response and improvement in short channel effects are observed.

The V_T response to side-gate spans a wide range for narrow devices (Figure 5.2a). Although it is certain that the body is accumulated for sub-zero side-gate bias (V_{side}) values, for small positive side-gate biases (e.g. V_{side} = 0.5 V), the device maintains a very low off current, implying that the body is not going into depletion at that stage. This is due to the work function difference of the p+ side-gate and the p-type body with a low doping level (~$1\times10^{17}cm^{-3}$). This also implies that some work function engineering could potentially be done on the side-gate to have more precise V_T control even when the side-gate is not biased [41].

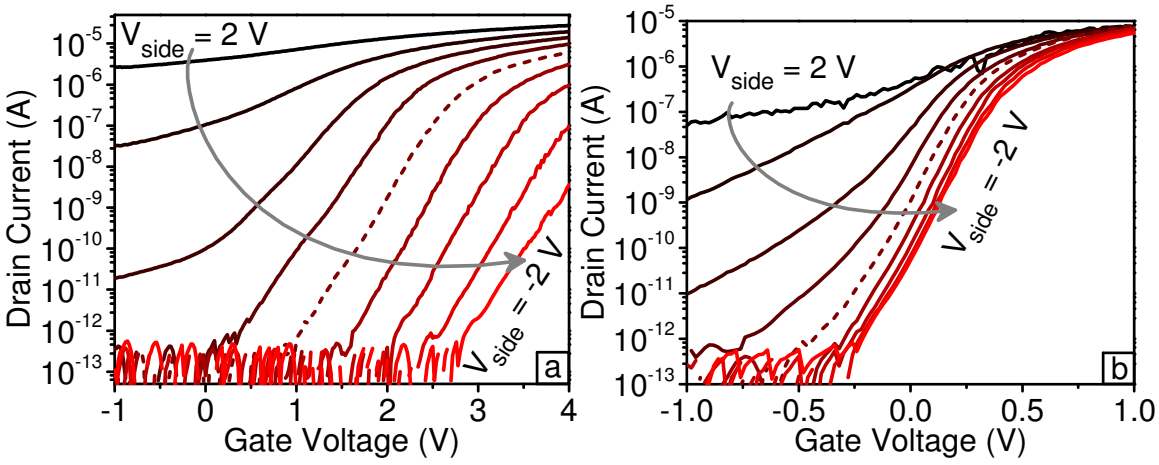


Figure 5.2. Transfer characteristics for a side-gate voltage sweep from 2 V to -2 V with 0.5 V decrements, (a) for a narrow device (W_{est} = 17 nm) (b) for a wider device (W_{est} = 53 nm). L_{est} = 37 nm, V_{drain} = 1 V, V_{sub} = 0 V for both. Dashed lines indicate V_{side} = 0 V.

5.2 Effect of Channel Width and Length

For wider devices (e.g. $W_{est} \times L_{est}$ = 53 nm × 37 nm), the side-gate's electrostatic control of the body degrades, resulting in decreased V_T sensitivity to side-gate bias (V_{side}) (Figure 5.2b). On the other hand, wider devices still show considerable V_T shift per volt applied on the side-gate ($\Delta V_T/\Delta V_{side} \approx 0.1$ V), as well as improvements in mitigation of short channel effects, mainly due to reduction of leakage paths along the sidewall of the body (Figure 5.3). SS and DIBL for these devices improve as a function of accumulation by the side-gate (i.e. negative side-gate bias), with minimal effect on transconductance (g_m). In this case V_T was extracted through the extrapolation of linear on current, and DIBL was calculated as $(V_{T-lin} - V_{T-sat})/0.9$ where $V_{T\text{-}lin}$ is V_T at V_{drain} = 0.1 V and $V_{T\text{-}sat}$ is V_T at V_{drain} = 1 V.

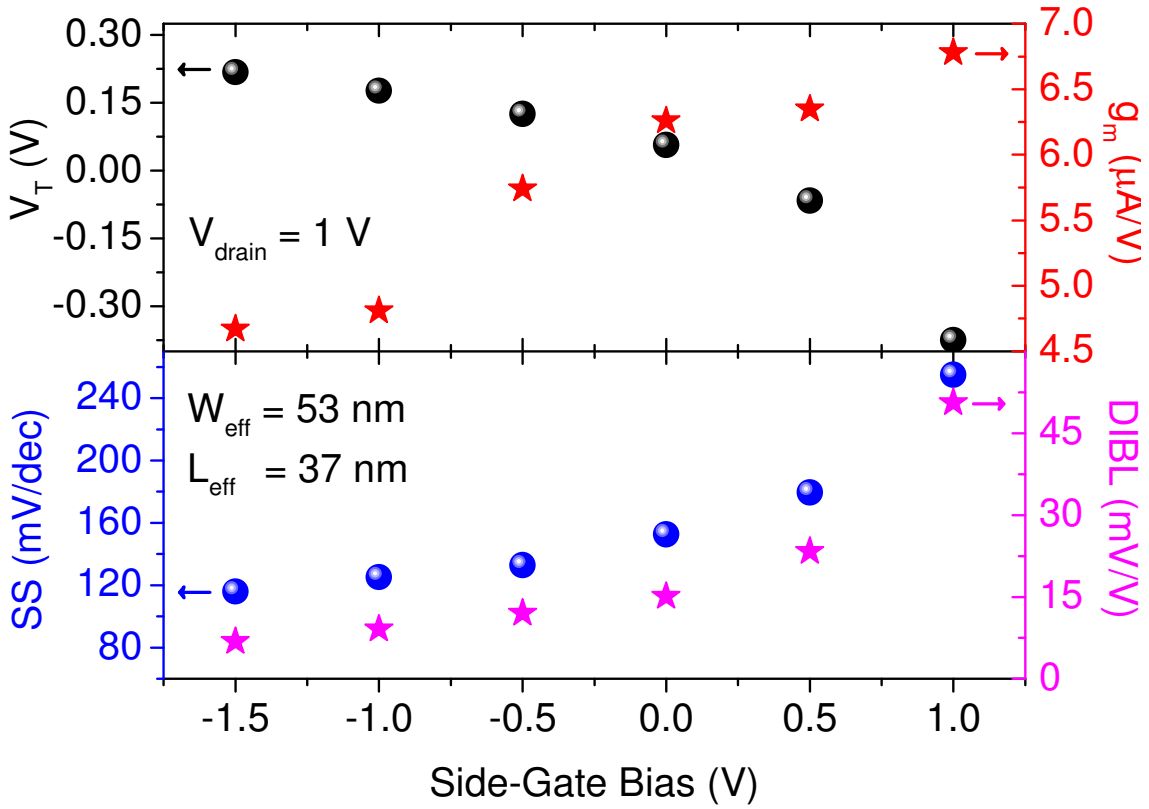


Figure 5.3. Threshold Voltage (V_T), transconductance (g_m), subthreshold slope (SS), and drain induced barrier lowering (DIBL) as a function of side-gate bias for a wider device with a short channel. V_{sub} = 0 V.

To quantify the role of channel width on the effectiveness of the side-gate's operation, for a given gate length (L_{est} = 37 nm), V_T values for a range of channel widths were extracted at V_{side} = 0 and at V_{side} = -2 V. $\Delta V_T/\Delta V_{side}$ values were obtained by dividing the V_T difference by 2. This method does not count in the fact that V_T shift achieved when V_{side} goes from 0 V to -1 V is more than when it goes from -1 V to -2 V [2], but it serves well to visualize the average shift. Results show the strong relationship

between the channel width and the V_T tunability that is achievable through accumulation by the side-gate ($\Delta V_T/\Delta V_{side} \approx 1.2$ V) (Figure 5.4a). When a similar analysis is done for the gate length at a given width (W_{est} = 55 nm), the correlation is weaker, which can be understood not as a change in the effectiveness of the side-gate but as a change in the FET gate's electrostatic control of the channel (Figure 5.4b).

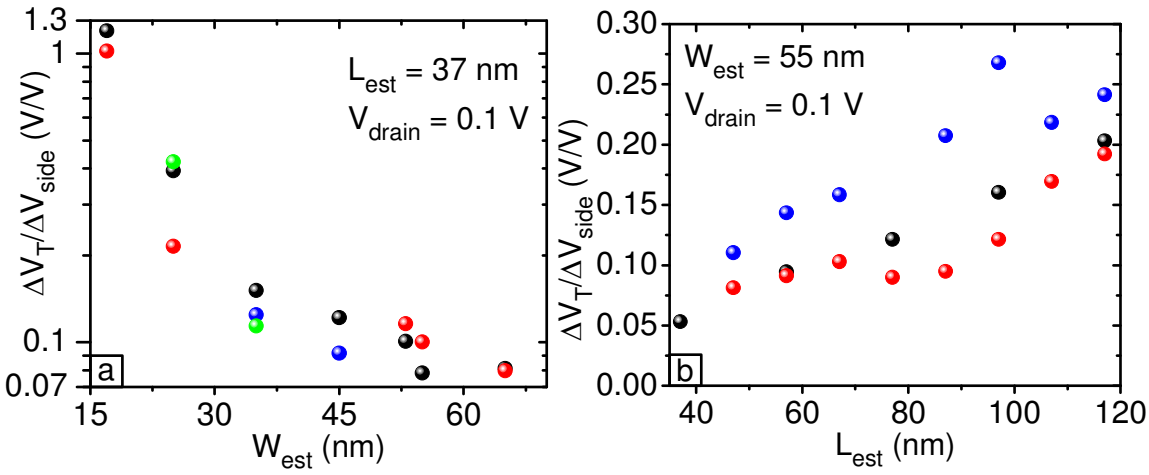


Figure 5.4. V_T change per -1 V applied to the side-gate as a function of (a) effective channel width, (b) as a function of effective gate length. Different colors denote different dies on the same wafer.

5.3 Output Current Degradation and Its Comparison to Leakage Performance

The V_T shift and increased vertical fields [41] with biasing the side-gate leads to some degradation in the on-current (Figure 5.5). This degradation, however, when compared to the decrease in the off-current, is smaller, resulting in an overall gain in the I_{max}/I_{min} ratio (Figure 5.6).

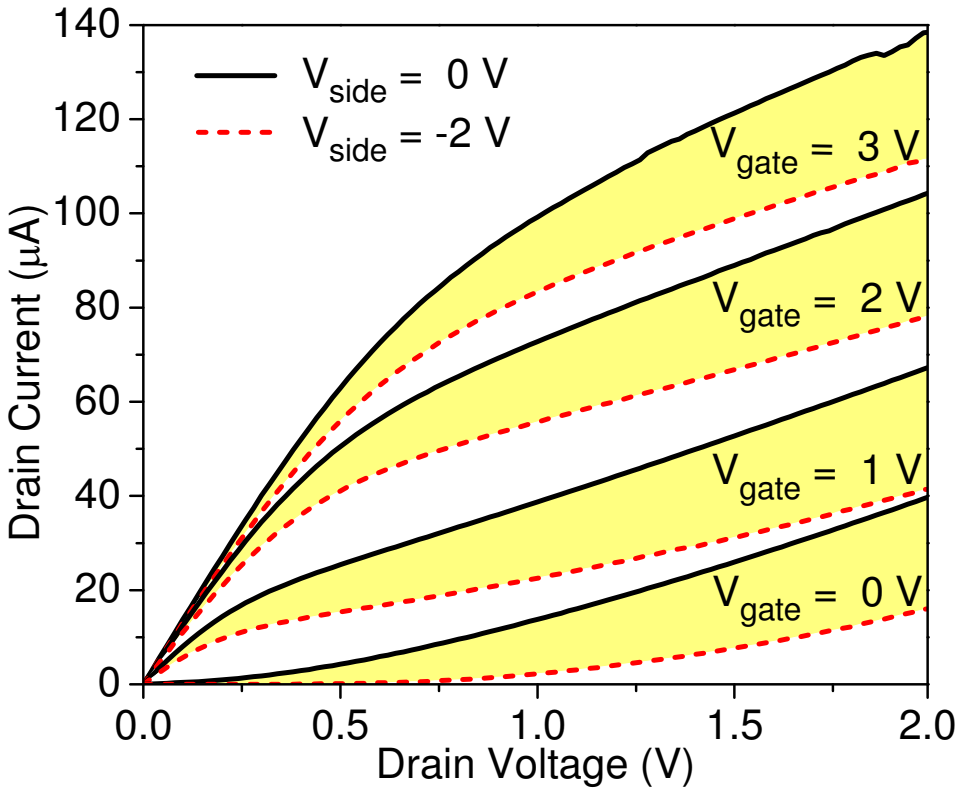


Figure 5.5. Output characteristics of an accumulated body nFET for different side-gate biases, showing the degradation in on-current with increased side-gate bias. V_{sub} = 0 V, W_{est} = 53 nm, L_{est} = 37 nm.

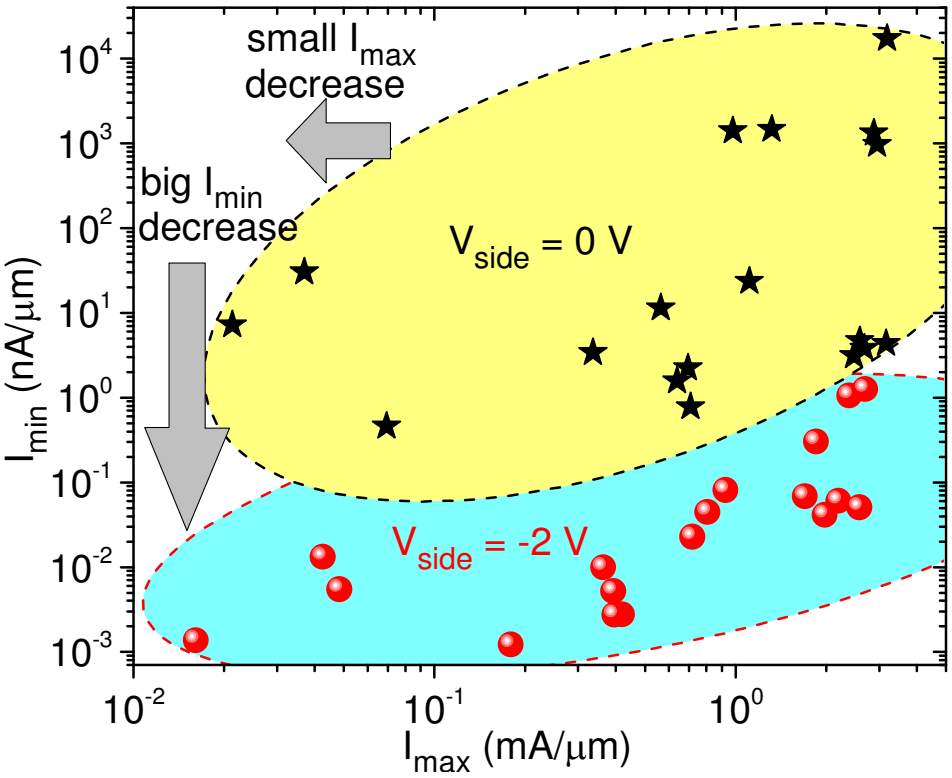


Figure 5.6. Normalized minimum drain current (I_{min}) vs. normalized maximum drain current (I_{max}) for accumulated body nFETs of various dimensions. When V_{side} is ramped from 0 V (values in the yellow ellipse) to -2 V (values in the cyan ellipse), minimum current goes down a few orders of magnitude whereas the maximum current level suffers only a small decrease. V_{gate} = -2 for I_{min}, V_{gate} = 2 V for I_{max}, V_{drain} = 1 V, V_{sub} = 0 V.

5.4 Side-gate vs. Substrate Biasing

The side-gate's control on the FET body affects the sensitivity to substrate biasing as well. When the body is depleted by the side-gate, V_T sensitivity to substrate bias (V_{sub}) is minimal. However, as side-gate is used to accumulate the body ($V_{side} < 0$), substrate coupling to the body increases dramatically, enhancing the V_T sensitivity to V_{sub}; hence, increasing the V_T tuning range (Figure 5.7). When $V_{sub} < V_{side}$, and both being negative, side-gate/body capacitor helps substrate bias widen the body depletion depth. When the

two voltages are comparable or $V_{side} < V_{sub}$, the mobile majority carriers (holes) brought by the side-gate bias are more responsive to changes in substrate bias, thus increasing the V_T sensitivity to V_{sub}.

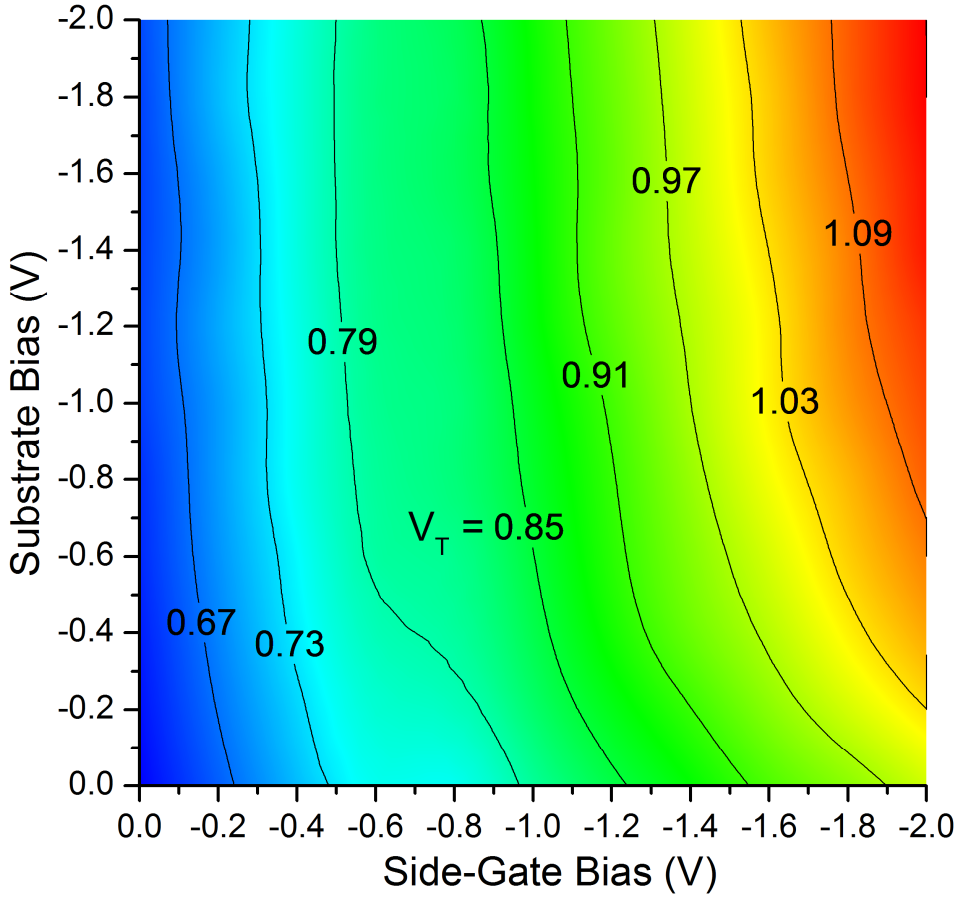


Figure 5.7. Threshold voltage as a function of side-gate and substrate biases for a short, narrow device (W_{est} = 17 nm, L_{est} = 37 nm). Accumulation by side-gate (as V_{side} → -2 V), a change in V_{sub} leads to greater V_T change. V_{drain} = 0.1 V

6 Conclusions

Accumulated body approach via an independently controlled side-gate has been experimentally demonstrated to significantly suppress leakage currents at < 70 nm gate length bulk Si MOSFETs with very high side-interface fixed charge densities [2]. What has been missing was the understanding of the governing physics of accumulated body behavior through modeling and its experimental implementation using a conventional CMOS flow.

The 3D computational analysis reported here captures the general accumulated body device behavior and provides insight to possible design approaches to extend the use of planar MOSFETs down to the 10-nm regime using a modified STI scheme. The earlier experimental work utilizing n+ side-gate required $V_{side} < -1$ V to effectively suppress leakage currents [2, 17]. The use of p+ side-gate is demonstrated to give a significant reduction in leakage currents even if it is not biased, due to the work function difference between the body and the side-gate, hence V_T adjustments can be achieved through work function of the side-gates during device fabrication. This was verified through the integration of MOSFETs with p+ type side-gates, showing low leakage currents even at positive side-gate biases.

The experimental integration of the devices also employed novel techniques, such as the technique of creating a lateral contact pad for the vertical side-gate structure without the need of complicated procedures, and with good variation tolerance.

The simulation results show significant increase in the source barrier height even in the center of the device. The improvement in SS is due to suppression of leakage currents to < 1 fA while the improvement in DIBL is due to suppressed drain coupling to the channel with reduced depletion depth by accumulation of the body. The improvement is even more pronounced when compared to wide and short planar FETs for which the increased off currents degrade subthreshold characteristics sharply. With accumulated body FETs, threshold voltage control over 1 V range is predicted down to < 15 nm gate length. In experimental devices, V_T control is even stronger, partly because of the fact that relative ratio of side-gate to gate dielectric is higher in them. More than 1 V of V_T shift is observed per volt of side-gate bias for narrow and short devices.

Output conductance is reduced with increased side-gate bias due to suppressed short channel effects as well as increased surface roughness scattering with increased vertical field for the same carrier concentration. V_T shift also affects the suppression in output current. When normalized maximum and minimum drain currents of experimental devices are compared, however, it is seen that the loss in output current is much less than the gain acquired through the suppression of leakage current.

The device response to substrate bias depends on the relative side-gate bias since the depletion depth is controlled by the side-gate if $V_{side} < V_{sub}$. For large negative side-gate biases, the side interfaces and the body experiences significant accumulation by majority carriers. It is also possible to achieve a fully-depleted body if $V_{side} > V_{sub}$ while keeping the source to substrate diode reverse biased ($V_{sub} < V_s$). Hence, depletion capacitances and substrate sensitivity can be significantly controlled with the side-gate.

When compared to FinFETs, which show negligible response to substrate biasing, this feature of accumulated body FETs is appealing for certain applications requiring dynamic V_T control, although side-gate parasitic capacitance is a factor worth considering for high speed applications. Using the accumulated body approach is also predicted to enable higher temperature operation by maintaining $I_{max}/I_{min} > 10^3$ at T = 600 K.

Suppression of leakage currents is responsible for the overall improvement in I_{max}/I_{min} with a value of $> 10^6$ for devices with very low side-interface fixed charge densities. This improvement is $>10^{10}$ for FETs with interface positive fixed charge densities in the order of 10^{12} cm^{-2}, verifying the experimental results using Si_3N_4 as the side-insulation and STI material [2]. The flexibility in STI dielectric, then, enables integration of accumulated body FETs to systems with different material needs [18, 42].

7 Appendices

7.1 Running Synopsys Sentaurus

After a discussion on different components forming the Sentaurus suite, a tutorial on how to run the tools will be given. The tutorial was written as a part of a class; thus some colloquial language can be expected and hopefully forgiven by the readers.

7.1.1 Components of Sentaurus

Although Sentaurus might not be the easiest suite to learn, it provides a comprehensive simulation environment starting from process simulations to device simulations. Here are some important components of Sentaurus *(Linux terminal commands associated with those tools are given in parenthesis)*:

Sentaurus Process (sprocess):

Sentaurus Process is a semiconductor process simulator. This tool is capable of running simulations in 1-D, 2-D or 3-D. Processes like ion implantation, annealing, etching and deposition are simulated using the parameters utilized in an actual processing tool (e.g. implantation dose and energy is inputted for simulating ion implantation). This tool can make use of an assisting user interface called Ligament Flow.

Figure 7.1. Logo for Sentaurus Process.

Ligament Flow Editor (ligedit):

Ligament Flow is an assisting tool to Sentaurus Process and provides the conversion of Graphical User Interface commands into the Sentaurus Process' scripting language.

Sentaurus Structure Editor (sde):

Sentaurus Structure editor is a piece of software with many capabilities like creating/modifying structures to be simulated, *emulating* some processes and adding contacts to a structure produced by Sentaurus Process.

Although this software has a compelling Graphical User Interface (GUI), its Scheme-based scripting is used when in conjunction with Sentaurus Process.

Figure 7.2. Logo for Sentaurus Structure Editor.

Sentaurus Device (sdevice):

Sentaurus Device is the simulator of *electrical characterization* of devices generated through Sentaurus Process and/or Sentaurus Structure Editor.

This tool can use a variety of physical principles and can measure all the electrical characteristics of a device. This tool also has a scripting language to input commands.

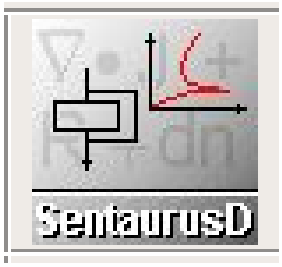


Figure 7.3. Logo for Sentaurus Device.

Inspect (inspect):

Inspect is a Graphing tool that can organize the data generated by Sentaurus Device and other simulation tools in the Sentaurus Suite.

This tool can either be used through its GUI, or can be programmed through a Tcl based scripting language to automatically generate the desired data. **".plt" files are usually associated with this tool.**

Figure 7.4. Logo for Inspect plotting tool.

Tecplot (tecplot_sv):

Tecplot is a visualization and graphing tool that is capable of manipulating 1, 2 and 3 dimensional data and structures generated by the simulation tools.

This tool can get **slices** of 3D data for visualization. **Usually, ".tdr" files are associated with this tool.**

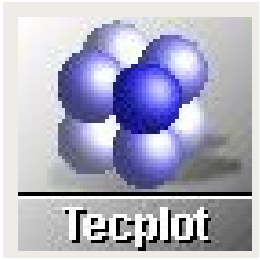


Figure 7.5. Logo for Tecplot plotting tool.

Sentaurus Workbench (swb):

Sentaurus Workbench is the organization tool that organizes the interfacing of all the tools mentioned above. This tool is also useful when creating splits in the simulation, that is generating different cases (or experiments in Sentaurus terminology), without modifying the underlying simulation.

Sentaurus Visual (svisual):

Sentaurus Visual is very similar to Tecplot and is being phased in to newer versions of Sentaurus to replace Tecplot. It has many features of Tecplot with small differences.

Figure 7.6. Logo for Sentaurus Visual.

7.1.2 Setting up Sentaurus

Creating the user folder:

Before using Sentaurus for the first time, you should create a folder for projects (STDB). In creating such a folder, care needs to be exercised, however to NEVER include spaces in the folder name. Sentaurus will generate errors. This is also the case for project names inside Sentaurus.

Running Sentaurus:

To run Sentaurus, start a Terminal window. Then, type in **swb** on the command line and press Enter.

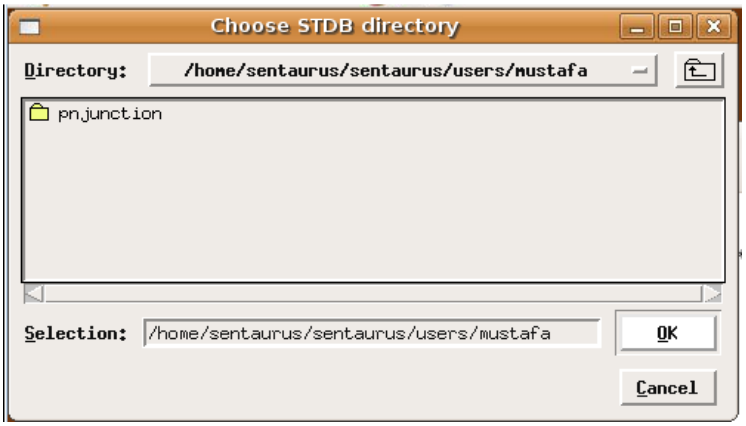


Figure 7.7. The screenshot of STDB (user folder) selection window.

On the “Choose STDB directory” window, go to the user folder that you have created and press OK. Please note that if the environment variable named STDB is already defined, then the selection window will not appear.

Important: Do NOT click any folder (project) name inside your user folder (STDB) before clicking OK. This would tell Sentaurus that the user folder is the *project* and you will not be able to see your other projects.

Sentaurus Workbench screen will appear. Please note the path of your user folder at the top of the Projects list.

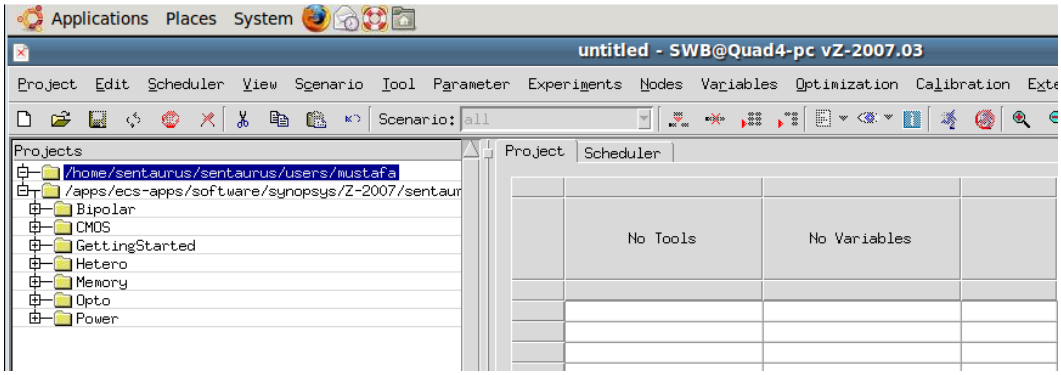


Figure 7.8. Screenshot showing a Sentaurus Workbench window upon loading.

Importing a Project

In order to import a project, you need to have a GZP file containing the compressed project folder.

1. In the Sentaurus Workbench (SWB) window, click on the **Project** menu from the top menu bar and select **Import…**

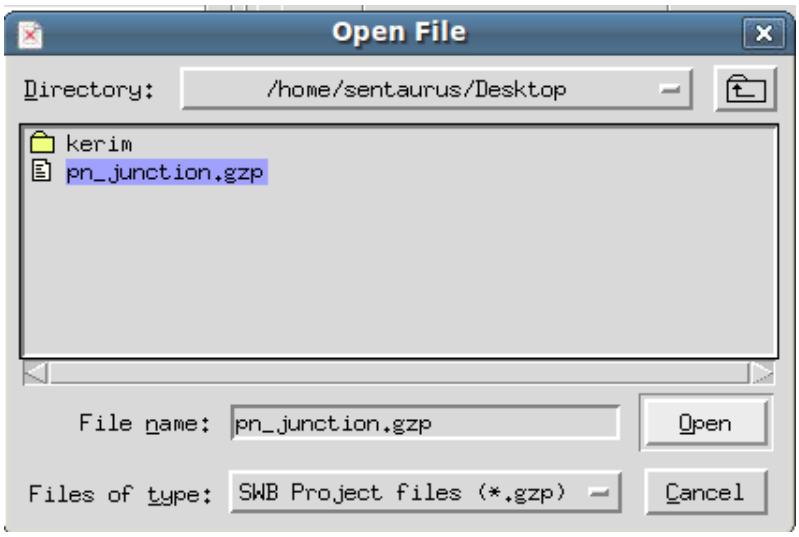


Figure 7.9. Screenshot for the dialog to import a project file.

2. From the **Open File** dialog, select the File that you have downloaded and Press **Open**. Remember, your desktop is at **/home/<user>/Desktop** path.
3. In the **Unpacking** Dialog, select **Save As…**

Note: If you select **Unpack**, it will still open the project, but will save it in a temporary location. Therefore, in that case, you should still go to **Project > Save As…** to save your project.

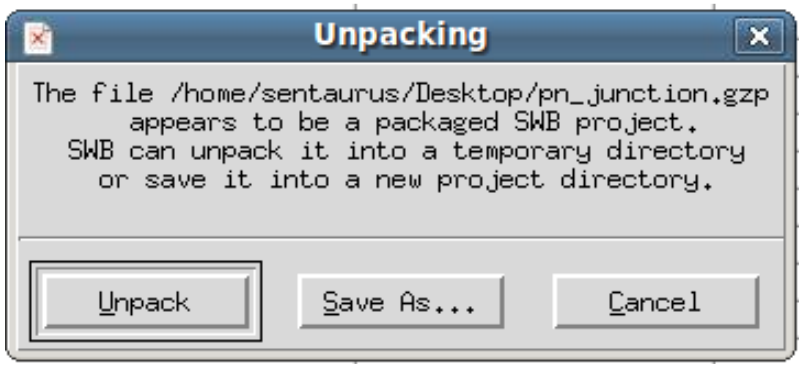


Figure 7.10. Screenshot of the dialog providing options on unpacking a file. It is recommended to select 'Save As...'

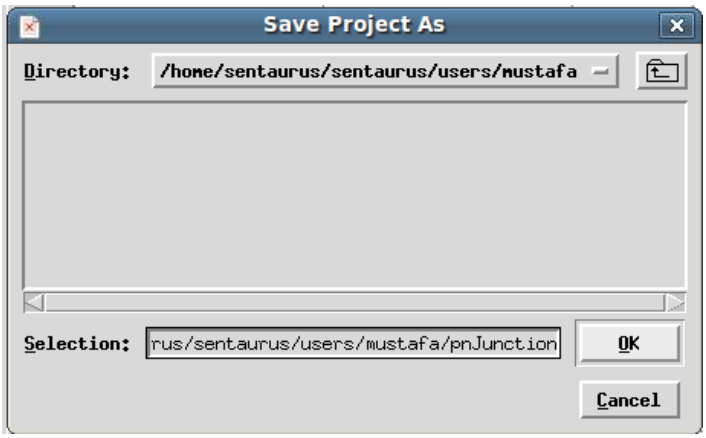


Figure 7.11. Screenshot of 'Save Project As' dialog box which appears after selecting 'Save As...' option upon unpacking a project file.

In the ‘Save As…’ dialog, type in a name for your project. Make sure that you use the FULL path name of your user folder in the selection section or any ‘File Input / Output’ operation in Sentaurus. If you start typing in a name, it will delete the full path, and you will not be able to write to the root folder (/), generating errors.

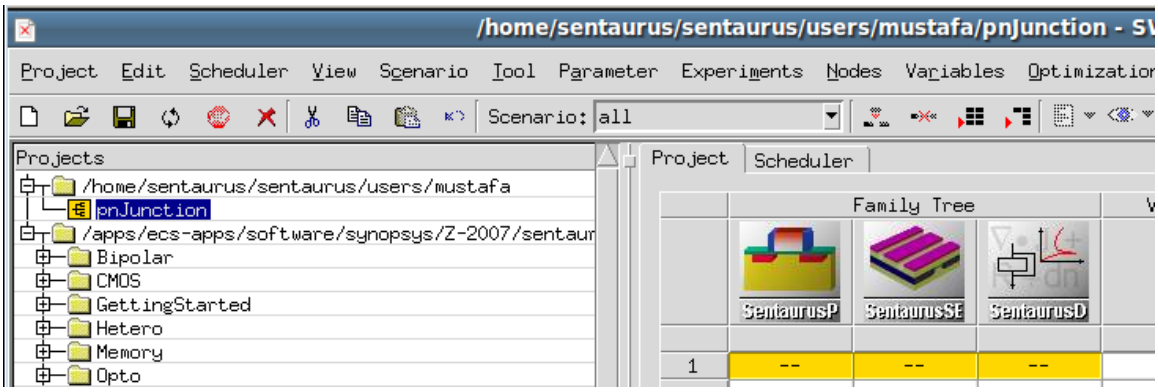


Figure 7.12. Screenshot of the Sentaurus Workbench and Project Explorer, showing the imported project.

When the saving is complete, you should be able to see a similar window to the one in Figure 7.12 with:

- The Title Bar displaying the full path to your project.
- **Projects** column on the left showing the project *under* your user folder.

Project opens up in the excel-like area on the right.

7.1.3 Running a Sentaurus Project

Nodes:

Each “cell” in the excel-like display of Sentaurus is called a **node** and represents a case that is run for a simulation. For the familiar ones to Object-Oriented programming, nodes are more like instances of classes that are defined by the simulation.

Unlocking a Project:

More than often, you will see that a project is locked when you are trying to run it. This might be due to a few things like a simulation that is still running or an output window popped up by the simulation (like a TecPlot plot) is still open.

To unlock a project, simply go to the **Project Menu** and Press **Unlock (Ctrl+K).** The same menu is available if you right-click on the project name on the Projects column and select Project (Figure 7.13).

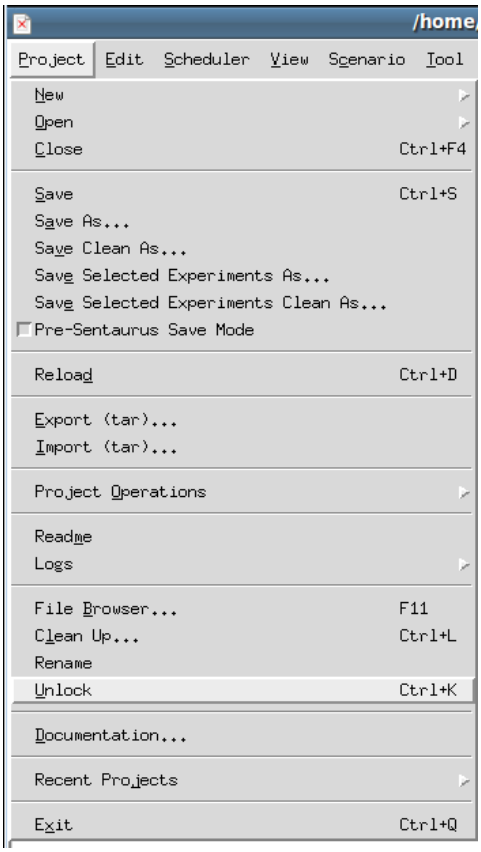


Figure 7.13. 'Project' menu on Sentaurus Workbench with 'Unlock' option highlighted.

Running a Node:

In order to run a simulation node (see the Node definition above), you should:

1. Select the node by clicking on it. (You can select multiple nodes either by pressing the mouse button and dragging the pointer across or by clicking on different nodes while Ctrl button is pressed.)

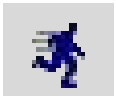


Figure 7.14. 'Running Person' symbol that is used to run selected simulation nodes.

2. Click on the ‘running person’ symbol (Figure 7.14) on the toolbar at the top to run. If it is not active, please unlock your project as described above.

Alternatively, you can select **Run…** from the **Nodes** Menu in the Menu Bar or from the right-click menu of a node.

7.1.4 Editing a Sentaurus Project:

As discussed in the Components of Sentaurus section above, different tools combine to create a full simulation of a device, from the fabrication to the electrical characterization. Before editing the simulation, please keep the following in mind:

- Each simulation tool (e.g. Sentaurus Process, Sentaurus Device etc.) has a different script / GUI to do the edit.
- Editing the simulation (input) does not automatically change the results; individual nodes need to be run again for the new results.
- Once a simulation is edited, all the nodes under that tool (in the excel-like table) as well as any node on its right becomes obsolete and need to be run again to reflect the change.

Once the points above are noted, to edit a simulation tool's input:

1. Right-click on the icon of the tool for which the input needs to be edited.
2. Go to Edit Input…
3. Select the appropriate method. (For SProcess, Ligament Flow is the main editor whereas the Command File is the method of editing for the rest.)

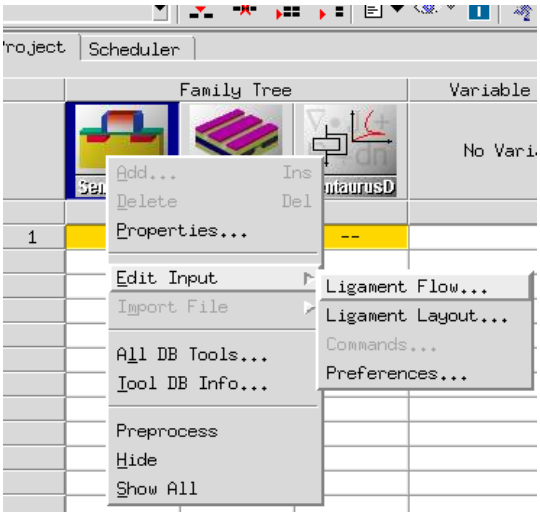


Figure 7.15. Right-click menu of a Sentaurus Process column, showing the 'Edit Input' submenu. Ligament flow provides a graphical interface. In most cases, however, 'Commands' is selected to edit the script.

Ligament Flow:

When SProcess is being edited, Ligament Flow can be used. To edit the process conditions set by the Ligament flow, you should click on the related process on the **Flow** Column on the left, and **double click** the related value that needs to be changed on the **Arguments** column on the right.

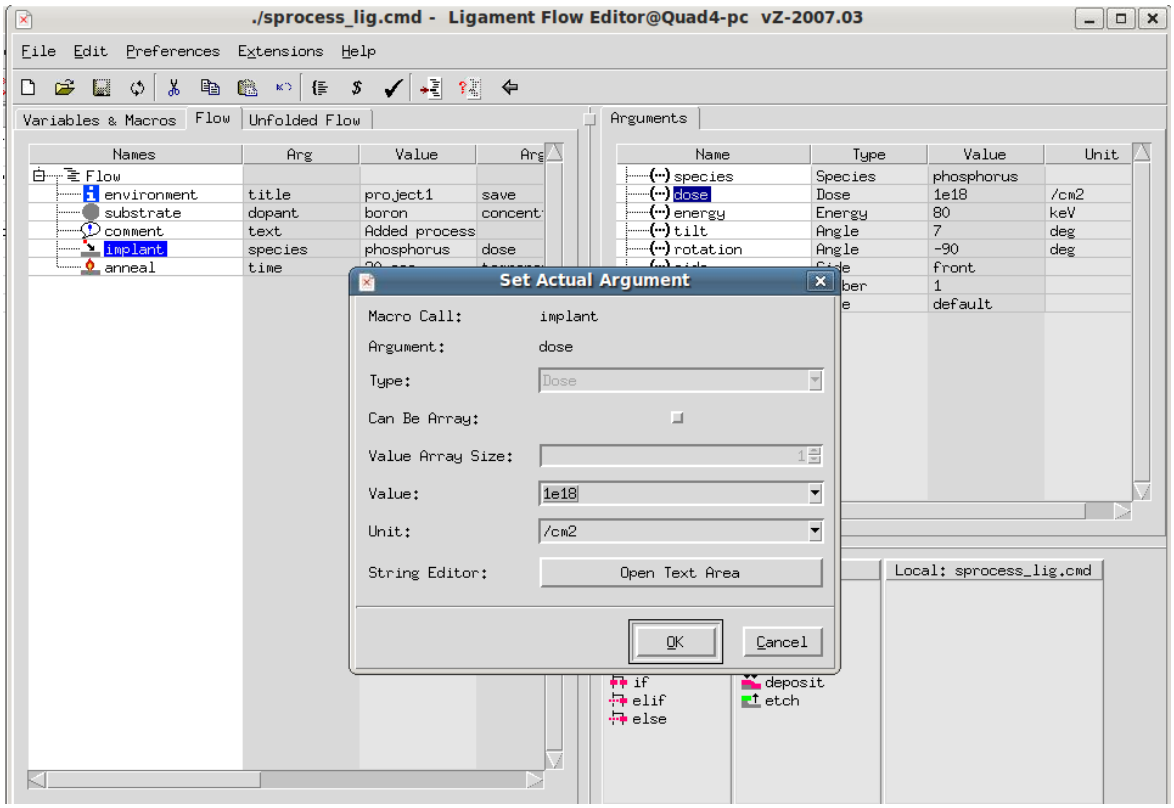


Figure 7.16. Ligament Flow window with the argument setting dialog for ion implantation dose.

Usually, changing the Value should be enough. In some cases Unit might also be important (e.g. in implant energy).

7.1.5 Visualizing the Results

Since each node is run separately, the results generated will also be different. Common sense tells us that the nodes associated with processing would have results more related to wafer processing (like impurity levels), whereas the results related to electrical characterization would be under the nodes related to Sentaurus Device.

To display a node's results:

1. Right-click on the node.
2. Select Visualize…

3. Select an Output file type (like tdr or plt or dat).
4. Select a tool (like Sentaurus Visual or Inspect)

Common output file types:

TDR: This file type is almost always generated automatically after **Sentaurus Process**, **Sentaurus Device** and **Sentaurus Structure Editor** simulations. This file is usually saved at the end of the simulation and is 1-D, 2-D or 3-D depending on the simulation (In the sample, it is a 2-D simulation). Because of its complex nature, **TecPlot or Sentaurus Visual** is perfectly suited to view this file type.

PLT: These are usually generated while running electrical characterization sweeps in **Sentaurus Device** by the user. Information like current, voltage etc. are kept in this file. **Inspect** is suited to open this file, although TecPlot or Sentaurus Visual is capable too.

DAT: This file is generated by the user and resembles the TDR files in nature. It is usually generated in a few different places within the simulation as opposed to TDR which is generated at the end. **Sentaurus Device** and **Sentaurus Process** widely use this file. Like the TDR files, **TecPlot or Sentaurus Visual** is perfect for viewing these files.

7.2 Details of Sentaurus TCAD Simulations

This appendix explains some details on numerical analysis discussed in Chapter 2.

7.2.1 Programming Code for Process Simulations and Structure Editing

As discussed in section 2.2, the process simulation starts in 2D and then is extruded to 3D. The simulation is based on a sample found in Synopsys SolvNet (3D Bulk NMOSFET).

```
#header
## ********** 2D portion of nMOS 3D simulation *********
#endheader

#include "LIB/models.par"


line x location=0 spacing=0.005 tag=bottom
line x location=0.5 spacing=0.05
line x location=10 spacing= 0.5 tag=top

line y location=0.0 spacing=0.05 tag=left
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
## --- Increased 0.1 to 0.3 -----------------
line y location=@<W+0.3>@ spacing=0.05 tag=right
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

#set TopRef 0.0

region Silicon xlo=bottom xhi=top ylo=left yhi=right
init
select Silicon z=1e+15 name=Boron store
solution name=Boron add

## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
## --- Screen Oxide -------------------
deposit material = { Oxide } time=1.0 rate=0.0015 type = {isotropic}


## --- Anti-punchthrough & Vt adjustment implants ----
implant  Boron  dose=2.00e13  energy=200  tilt=0 rotation=0
implant  Boron  dose=1.00e13  energy=80   tilt=0 rotation=0
implant  Boron  dose=2.00e12  energy=25   tilt=0 rotation=0

## p-well: RTA of channel implants
diffuse  time=10.0<s>   temp=1050
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
## ------------------------------------
## ---- Pad Oxide -----
## ------------------------------------

gas_flow name=gasflow2 pressure=1 flowO2=1.0
diffuse temp=1050 time=1.5 gas_flow=gasflow2

## ------------------------------------
## ---- Nitride Deposition -----
## ------------------------------------

#postheader
mgoals on min.normal.size=0.001 normal.growth.ratio=1.5 accuracy=2e-6
#endpostheader
deposit material = {Nitride} type=isotropic rate=1.0 time=0.1000
diffuse temp=800 time=30


## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
## ---------- LTO Deposition ----------------
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

deposit material = {Oxide} type = isotropic rate = {1.0} time=0.1
diffuse temp=1050 time=10

#split <trench>

## ------------------------------------
## ---- STI Lithography -----
## ------------------------------------
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
## --- Increased 0.1 to 0.3 -----------------
mask name=mask2 segments = {-1.0 @W@ @<W+0.3>@ } negative
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
deposit mask=mask2 material = {Photoresist} rate = {0.5} time=1
type=anisotropic


## ------------------------------------
## ---- STI Etching -----
## ------------------------------------

## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
etch material = {Oxide} type=anisotropic rate = {0.1} time=1.1
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

etch material = {Nitride} type=anisotropic rate = {0.1} time=1.05

etch material = {Oxide}   type=anisotropic rate = {0.01} time=1.1

strip Photoresist

etch time=40 type=directional material= {Silicon} rate=0.01 direction=
{tan(85.0*atan(1.0)/45.0) 1.0 0.0}
```

```
## ------------------------------------
## ---- Liner Oxide -----
## ------------------------------------

gas_flow name=gasflow20 pressure=1 flowO2=15 flowH2O=5
temp_ramp name=liner temp=500 time=10 ramprate=45<K/min>
temp_ramp name=liner temp=950 time=5 gas_flow=gasflow20
temp_ramp name=liner temp=950 time=18 ramprate=-25<K/min>
diffuse temp_ramp=liner

struct tdr=n@node@_liner

## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
## ---------- Side-gate poly deposition -----
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

deposit  material = {Polysilicon} rate=1 type=isotropic  time=0.18
species=boron concentration=10^20

struct tdr =n@node@_sgpolydep

## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
## ---------- Side-gate poly etch -----
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

etch material = {Polysilicon} type=anisotropic rate = {0.01}
time=@SGEtchTime@ isotropic.overetch=0.01

## ------------------------------------
## ---- TEOS Deposition -----
## ------------------------------------

deposit material = {Oxide} type = isotropic rate = {1.0} time=0.1

## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
struct tdr =n@node@_TEOS
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

## ------------------------------------
## ---- Fake STI CMP -----
## ------------------------------------
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
##etch  type = cmp material = all rate = {1.0} coord=-0.06
etch  type = cmp material = all coord=-0.06
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
## etch  type = cmp material = {Oxide} rate = {1.0} coord=-0.03

deposit material = {Oxide} type = fill coord=-0.1

etch material = {Oxide} type=anisotropic rate = {0.05} time=1.0



## ------------------------------------
```

```
## ---- Nitride Removal + Overetch -----
## -------------------------------------

etch material = {Nitride} type=isotropic rate = {0.15} time=1.5
etch material = {Oxide} type=isotropic rate = {0.014} time=1.1

## Making it a finfet for different SGEtchTime conditions

if {@SGEtchTime@>"40"} {
    etch material = {Oxide} type= isotropic rate= {0.01} time =
{@<SGEtchTime-40>@}
}

#split <Lpoly>

## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
## ---------- Moved the well doping to up -----
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

## gate oxidation
diffuse  time=8.0   temp=800 dryO2


## poly gate deposition
deposit  material = {Polysilicon} rate=1 type=isotropic  time=0.18

#split <save>
line z location=0 spacing=0.1 tag=back
line z location=@<Lpoly/2.0 + 0.3>@ spacing= 0.1 tag=front

set oxsi [ interface y=0.0 silicon /oxide]
puts "DOE: TopRef $oxsi"

mgoals accuracy=0.0002

struct tdr=poly_n@node@ bnd !gas !interfaces !FullD

struct dfise=n@node@

exit 0
```

The following file (sdep_dvs.cmd) is a Structure Editor (sde) script based on the Scheme language. This set of commands extrudes 2D model into 3D selectively. After that, it emulates the nitride spacer and meshes the structure for the subsequent 3D simulation:

```
(sde:clear)
```

```
(define WL  @<Lpoly/2.0+0.3>@)
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; Changing 0.1 to 0.3
(define WW  @<W+0.3>@)
(define Toffspa 0.004)
(define Tspa    0.08)
(define Hspa    0.15)

;--------------------------------------
; Loading SP 2D boundary
(sdeio:read-tdr-bnd "poly_n@previous@_bnd.tdr")
(sdegeo:bool-unite (find-material-id "Silicon"))
(sdegeo:bool-unite (find-material-id "Oxide"))
;(sdegeo:bool-unite (find-material-id "PolySilicon"))

;-----------------------------------------------;

;Transfer the 2D model and identify the faces, regions
(define siface (car (find-face-id (position 0.01 5.0  0.0))))
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; Changing 0.05 to 0.25
(define oxface (car (find-face-id (position @<W+0.25>@ 0.1  0.0))))
(define poface (car (find-face-id (position 0.1 -0.1 0.0))))

; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------- SG Interface ----------------

(define sgface (car (find-face-id (position @<W+0.1>@ 0.25 0.0))))

; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

(define sibody (car (find-body-id (position 0.01 5.0  0.0))))
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; Changing 0.05 to 0.25
(define oxbody (car (find-body-id (position @<W+0.25>@ 0.1  0.0))))
(define pobody (car (find-body-id (position 0.1 -0.1 0.0))))

; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------- SG Body ----------------

(define sgbody (car (find-body-id (position @<W+0.1>@ 0.25 0.0))))

; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

;-----------------------------------------------;
; Extrusion to 3D:
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; Adding sgbody to the list
(sdegeo:extrude (list sibody oxbody sgbody) WL)
(sdegeo:extrude (list pobody) @<Lpoly/2.0>@)

;Rotate to proper coordinate system
(define lmodel (part:entities (filter:type "solid?")))
(sdegeo:rotate lmodel 0 0 0 1 0 0 -90)
```

```
(sdegeo:rotate lmodel 0 0 0 0 0 1  90)
(entity:move lmodel @<Lpoly/2.0+0.3>@ 0 0)


;-----------------------------------------------;
; Reassigning the proper region names
(sde:addmaterial sibody "Silicon" "RSubstrate")
(sde:addmaterial oxbody "Oxide" "RTrench")
(sde:addmaterial pobody "PolySilicon" "RGate")
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------- SG Region ----------------

(sde:addmaterial sgbody "PolySilicon" "RSideGate")

; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

;-----------------------------------------------;
;Poly oxide spacer
(sdepe:depo "material" "Oxide" "thickness" Toffspa "type" "iso")

(sdepe:fill "Gas" 2.0)
(part:save "n@node@_halo.sat")
(sdepe:strip-material "Gas")


;-----------------------------------------------;
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; changing 0.1 to 0.3 in W+
; Nitride Specer
(sdegeo:set-default-boolean "BAB")
(sdegeo:create-cuboid (position (- WL 0.001) 0.0 -1) (position (- WL (+
Toffspa (+ Tspa (+ @<Lpoly/2.0>@ )))) @<W+0.3>@ Hspa) "Si3N4"
"R.Spacer")
(sdegeo:fillet-edges (car (find-edge-id (position (- WL (+ Toffspa (+
Tspa (+ @<Lpoly/2.0>@ )))) @<W-0.001>@ Hspa ))) 0.08)

(sdepe:fill "Gas" 2.0)
(part:save "n@node@_spacer.sat")

(sde:clear)
(sdesp:begin)
(sdesp:define-step "halo" "n@node@_halo.sat")
(sdesp:define-step "spacer" "n@node@_spacer.sat")
(sdesp:finalize "n@node@_sp_sde.tcl")

;-------------------------------------
; Meshing Strategy:
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; changing 0.1 to 0.3
(sdedr:define-refinement-window "All_RW" "Cuboid"
 (position 0.0 0.0 -10.0)  (position WL @<W+0.3>@ 1.0))
(sdedr:define-refinement-size "All_RD"
   (/ WL 4)          (/ WW 4)          1.0
   (/ WL 8)          (/ WW 8)          0.5 )
(sdedr:define-refinement-placement "All_PL" "All_RD" "All_RW" )
```

```
(sdedr:define-refinement-function "All_RD" "MaxLenInt" "Polysilicon"
"Oxide" 0.001 2.0)

# Si refinements
(sdedr:define-refinement-window "GSDII_RW" "Cuboid"
 (position 0.325 @<W>@ @<-TopRef-0.02>@)  (position 0.275 0.0 @<-
TopRef>@))
(sdedr:define-refinement-size "GSDII_RD"
   (/ WL 64)        (/ WW 32)        0.015625
   (/ WL 128)       (/ WW 64)        0.0078125 )
(sdedr:define-refinement-placement "GSDII_PL" "GSDII_RD" "GSDII_RW" )

(sdedr:define-refinement-window "GSDI_RW" "Cuboid"
 (position WL @W@ -0.1 )  (position 0.0 0.0 0.0))
(sdedr:define-refinement-size "GSDI_RD"
  (/ WL 16)         (/ WW 16)        0.015625
  (/ WL 32)         (/ WW 32)        0.0078125 )
(sdedr:define-refinement-placement "GSDI_PL" "GSDI_RD" "GSDI_RW" )
(sdedr:define-refinement-function "GSDI_RD" "MaxLenInt" "Silicon"
"Oxide" 0.001953125 1.5)

(sdedr:define-refinement-window "GSD_RW" "Cuboid"
 (position WL @W@ -0.25 )  (position 0.0 0.0 0.0))
(sdedr:define-refinement-size "GSD_RD"
  (/ WL 16)         (/ WW 16)        0.015625
  (/ WL 32)         (/ WW 32)        0.0078125 )
(sdedr:define-refinement-placement "GSD_PL" "GSD_RD" "GSD_RW" )

; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; changing 0.1 to 0.3
(sdedr:define-refinement-window "GOx_RW" "Cuboid"
 (position WL @<W+0.3>@ -0.40)  (position 0.0 0.0 -0.25))
(sdedr:define-refinement-size "GOx_RD"
  (/ WL 8)          (/ WW 8)         0.03125
  (/ WL 16)         (/ WW 16)         0.015625 )
(sdedr:define-refinement-placement "GOx_PL" "GOx_RD" "GOx_RW" )
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; changing 0.1 to 0.3
(sdedr:define-refinement-window "Si_RW" "Cuboid"
 (position 0.0 0.0 -0.4)  (position WL @<W+0.3>@ -1.0))
(sdedr:define-refinement-size "Si_RD"
  (/ WL 8)          (/ WW 8)         0.0725
  (/ WL 16)         (/ WW 16)         0.03125 )
(sdedr:define-refinement-placement "Si_PL" "Si_RD" "Si_RW" )

# Poly refinement
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; changing 0.1 to 0.3
(sdedr:define-refinement-window "Po_RW" "Cuboid"
 (position (- WL @<Lpoly/2.0>@) 0.0 0.0)  (position WL @<W+0.3>@ 0.2))
(sdedr:define-refinement-size "Po_RD"
 (/ WL 8)         (/ WW 16)        0.03125
  (/ WL 16)         (/ WW 32)        0.015625 )
(sdedr:define-refinement-placement "Po_PL" "Po_RD" "Po_RW" )
```

```
(sdedelaunizer:set-parameters "maxPoints" 150000)

;---------------------------------
; Saving:

(part:save "n@node@_dvs.sat")

(sdeio:save-dfise-bnd (get-body-list) "n@node@_msh.bnd")
(sdedr:write-cmd-file "n@node@_msh.cmd")
```

The following file (SProcess3D_fps.cmd) is the 3D portion of the process simulation after the extrusion is done in Sentaurus Structure Editor:

```
#header

##   ************* 3D Portion *************

source n@node|sdep@_sp_sde.tcl

set WL  @<Lpoly/2.0+0.3>@
## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
## Changing 0.1 to 0.3
set WW  @<W+0.3>@
set hgate @<Lpoly/2.0>@
set topSi @TopRef@

#endheader

#include "LIB/models.par"

mgoals min.normal.size=0.01 max.lateral.size=1000 \
max.box.angle=165 normal.growth.ratio = 2 accuracy=1e-6 sliver.split


##DFISE          -Z    Y     X
refinebox min= "-2.0          0.0              0.0" \
          max= "10.0          $WW              $WL" \
          xrefine= 1.5        yrefine= $WW/2.0 zrefine= $WL/4.0


refinebox min= "0.4           0.0              0.0" \
          max= "1.0           $WW              $WL" \
          xrefine= 0.09375    yrefine= $WW/2.0 zrefine= $WL/4.0


refinebox min= " 0.2          0.0              0.0" \
          max= " 0.4          ($WW-0.1)        $WL" \
          xrefine= 0.046875   yrefine= $WW/4.0 zrefine= $WL/8.0
```

```
refinebox min= " $topSi         0.0               0.0" \
          max= " 0.2            ($WW-0.1)         $WL" \
          xrefine= 0.0234375    yrefine= $WW/16.0 zrefine= $WL/16.0


refinebox min= "$topSi          0.0                0.0" \
          max= "$topSi+0.016     ($WW-0.1)          ($WL-$hgate-0.01)" \
          xrefine= 0.002929688 yrefine= $WW/16.0 zrefine= $WL/32.0

refinebox min= "$topSi          0.0                ($WL-$hgate-0.01)" \
          max= "$topSi+0.032     ($WW-0.1)          ($WL-$hgate+0.02)" \
          xrefine= 0.002929688 yrefine= $WW/32.0 zrefine= $WL/64.0



init tdr=n@previous@_msh.tdr


recreate_step halo

load dfise=n@node|Sprocess2D@ replace

#split <ext>

## nldd implantation
implant  Arsenic  dose=2e14    energy=10 tilt=0  rotation=0
ifactor=1.0 vfactor=0 info=1

#split <halo>

## Halo implantation: Quad HALO implants:

## %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
## --------- Adding Y reflection for full ---
struct tdr=n@node@_quart !interfaces
exec tdx -mtt -X  n@node@_quart_fps n@node@_half
exec tdx -mtt -y  n@node@_half n@node@_full

init tdr=n@node@_full

implant  Boron    dose=@HaloDose@ energy=20 tilt=30 rotation=0
ifactor=0.8 vfactor=0 info=1
implant  Boron    dose=@HaloDose@ energy=20 tilt=30 rotation=90
ifactor=0.8 vfactor=0 info=1
implant  Boron    dose=@HaloDose@ energy=20 tilt=30 rotation=180
ifactor=0.8 vfactor=0 info=1
implant  Boron    dose=@HaloDose@ energy=20 tilt=30 rotation=270
ifactor=0.8 vfactor=0 info=1


struct tdr=n@node@_halo !interfaces

init tdr=n@node@_quart_fps
```

```
load tdr=n@node@_halo replace


#split <rtpext>

## RTA of LDD/HALO implants
diffuse  time=1.0<s>  temp=1050 info=1 init=1e-8

#split <nplus>

## nitride spacer
recreate_step spacer

## N+ implantation
implant  Arsenic  dose=5e15    energy=40 tilt=0  rotation=0 ifactor=1.5
vfactor=0 info=1

#split <rtp>

## N+ implantation & final RTA
diffuse time=2.0<s>  temp=1050 info=1

struct tdr=n@node@dmp


struct smesh=n@node@

exit 0
```

When 3D process simulation is done, a final step of Sentaurus Structure Editor (sde_dvs.cmd) is executed where contacts are placed, uniform doping is assigned to the gate and the side-gate, bottom of the device is cut to save computation time, and the parameters for final meshing are set. At this point, conventional devices (no-side gate) can be created simply by replacing the side-gate with the isolation material (oxide). The following code is for a side-gated device:

```
(part:load "n@node|sdep@_dvs.sat")

(define WL  @<Lpoly/2.0+0.3>@)
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; Changing 0.1 to 0.3
(define WW  @<W+0.3>@)
(define Toffspa 0.004)
(define Tspa    0.08)
; %%%%%%%%%%%%%%%%%%%%%%DopPol change
;(define DopPol  "BoronActiveConcentration")
(define SGDopPol  "BoronActiveConcentration")
```

```
(define GDopPol  "ArsenicActiveConcentration")

(sdepe:strip-material "Gas")

;Merge oxides in one single region
(sdegeo:bool-unite (find-material-id "Oxide"))

;Rename the regions
(sde:addmaterial (find-material-id "Silicon")  "Silicon"
"Substrate")
(sde:addmaterial (find-material-id "Oxide")    "Oxide"        "Trench")
(sde:addmaterial (find-material-id "Nitride")  "Nitride"      "Spacer")
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; Changing 0.1 to 0.3
; Create Metal contacts
(sdegeo:set-default-boolean "ABA")
(sdegeo:create-cuboid (position 0.0 0.0 @<-TopRef-0.005>@) (position (-
(- WL (+ Toffspa (+ Tspa (+ @<Lpoly/2.0>@ )))) 0.01) @W@ 0.01) "Metal"
"R.SourceContact")
(sdegeo:create-cuboid (position WL 0.0 0.15) (position (- WL
@<Lpoly/2.0>@) @<W+0.3>@ 0.22) "Metal" "R.GateContact")
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------Metal contact for SG ------------
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdegeo:create-cuboid (position WL @<W+0.3>@ -0.19) (position 0
@<W+0.1>@ -0.39) "Metal" "R.SideGateContact")


; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------0.1 to 0.3 ------------
; Cut the device
(sdegeo:create-cuboid (position 0.0 0.0 -20) (position WL @<W+0.3>@ -
1.0) "Silicon" "Dummy")
(sdegeo:delete-region (find-body-id (position 0.1 0.1 -5.0)))


; Set Contacts
(sdegeo:define-contact-set "gate"   4.0  (color:rgb 1.0 0.0 0.0 ) "##"
)
(sdegeo:define-contact-set "source" 4.0  (color:rgb 1.0 0.0 0.0 ) "=="
)
(sdegeo:define-contact-set "bulk"   4.0  (color:rgb 1.0 0.0 0.0 )
"<><>" )
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------Metal contact for SG ------------
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdegeo:define-contact-set "sidegate"   4.0  (color:rgb 1.0 0.0 0.0 )
"[][]" )

(sdegeo:set-current-contact-set "gate")
(sdegeo:set-contact-boundary-faces (find-body-id (position (- WL
@<Lpoly/4.0>@) @W@ 0.2)))
(sdegeo:delete-region (find-body-id (position (- WL @<Lpoly/4.0>@) @W@
0.2)))
```

```
(sdegeo:set-current-contact-set "source")
(sdegeo:set-contact-boundary-faces (find-body-id (position 0.001 0.001
0.0)))
(sdegeo:delete-region (find-body-id (position 0.001 0.001 0.0)))
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------Set contact for SG ------------
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdegeo:set-current-contact-set "sidegate")
(sdegeo:set-contact-boundary-faces (find-body-id (position (- WL 0.1)
@<W+0.2>@ -0.29)))
(sdegeo:delete-region (find-body-id (position (- WL 0.1) @<W+0.2>@ -
0.29)))



(sdegeo:set-current-contact-set "bulk")
(sdegeo:set-contact-faces (find-face-id (position 0.01 0.01 -1.0))
"bulk")
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------Cutting the y=0 side of the device------
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; Cut the device
(sdegeo:create-cuboid (position -1.0 0.001 1.0) (position 1.0 -1.0 -
1.5) "Silicon" "Dummy2")
(sdegeo:delete-region (find-body-id (position -0.5 -0.5 -0.5)))


; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------Change 0.101 to 0.301 ------------
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
;-------------------------------------
; Doping profiles:
(sdedr:define-refinement-window "DataWin" "Cuboid"  (position -0.001 -
0.001 0.201)  (position (+ WL 0.001)  @<W+0.301>@ -1.001) )
(sdedr:define-submesh-placement "Process" "Doping" "DataWin" 0
"NoReplace" 0 0 0 "" "Z" 0)
(sdedr:define-submesh "Doping" "n@previous@_fps.tdr" 'r)

;-----------------------------------------------------------------------
; Poly Doping
;%%%%%%%%%%%%%%%%%%%%%%separation of G and SG
(sdedr:define-constant-profile "GPoly" GDopPol 1e+20)
(sdedr:define-constant-profile "SGPoly" SGDopPol 1e+20)
;(sdedr:define-constant-profile-material "PolyPlacement" "Poly"
"PolySilicon" 0 "Replace")
(sdedr:define-constant-profile-region "GPolyPlacement" "GPoly"
"RGateRGate" 0 "Replace")
(sdedr:define-constant-profile-region "SGPolyPlacement" "SGPoly"
"RSideGateRSideGate" 0 "Replace")

;-------------------------------------
; Meshing Strategy:
# Si refinements
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdedr:define-refinement-window "GateI_RW" "Cuboid"
```

```
 (position 0.0 0.0 0.0)  (position WL @<W+0.3>@ -0.15))
(sdedr:define-refinement-size "GateI_RD"
   (/ WL 20)   @<W/8.0>@       0.02
   (/ WL 40)   @<W/16.0>@      0.01 )
(sdedr:define-refinement-placement "GateI_PL" "GateI_RD" "GateI_RW" )
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdedr:define-refinement-window "GOx_RW" "Cuboid"
 (position 0.0 0.0 -0.4) (position WL @<W+0.3>@ -0.15))
(sdedr:define-refinement-size "GOx_RD"
  (/ WL 10)        @<W/8.0>@        0.05
  (/ WL 40)        @<W/16.0>@       0.02 )
(sdedr:define-refinement-placement "GOx_PL" "GOx_RD" "GOx_RW" )
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdedr:define-refinement-window "Si_RW" "Cuboid"
 (position 0.0 0.0 -1.0)  (position WL @<W+0.3>@ -0.4))
(sdedr:define-refinement-size "Si_RD"
  (/ WL 10)        @<W/8.0>@         0.1
  (/ WL 40)        @<W/16.0>@        0.05 )
(sdedr:define-refinement-placement "Si_PL" "Si_RD" "Si_RW" )
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdedr:define-refinement-window "CBE_RW" "Cuboid"
 (position 0.0 0.0 -0.02) (position WL @<W+0.3>@ -0.025))
(sdedr:define-refinement-size "CBE_RD"
  (/ WL 100)        @<W/100.0>@        0.05
  (/ WL 100)        @<W/100.0>@       0.02 )
(sdedr:define-refinement-placement "CBE_PL" "CBE_RD" "CBE_RW" )
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

; Offset-Global
(sdenoffset:create-global
  "usebox" "aam"
  "maxangle" 150
  "maxconnect" 1000000
  "background" ""
  "options" "-p junction2 -p surface2 -p del-snps2 -p noffset3d -p
refine -p del-snps -p interpolate -x"
  "triangulate" 0
  "recoverholes" 0
  "hlocal" 0
  "factor" 1.5
  "subdivide" 0
  "terminateline" 3
  "maxedgelength" 0.1
  "maxlevel" 5)



(sdenoffset:create-noffset-interface "region" "Substrate" "Trench"
  "hlocal" 0.0005
  "factor" 1.3
  "window" (- 0.3 Tspa) 0.0 0.0 WL WW -0.15)

(sdenoffset:create-noffset-interface "region" "Trench" "Substrate"
  "hlocal" 0.0005
  "factor" 1.5
```

```
  "window" (- 0.3 Tspa) 0.0 0.0 WL WW -0.15)


(sdenoffset:create-isoline "pnj" "region" "Substrate"
                    "value" 0 "length" 0.0 "species"
"DopingConcentration"
                    "isobgcmode" "dopingmaxg" "bgesize" 0.0125)

;(sdenoffset:create-noffset-interface "region" "Substrate" "pnj"
;  "hlocal" 0.001
;  "factor" 2.0)

; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdenoffset:create-boundary "region" "Substrate" "Trench"
 "reggrid-regmod" "snap"
 "reggrid-uniform"    (/ WL 20)   @<W/8.0>@    0.02
 "reggrid-window"  0.0 0.0 -0.15 WL @<W+0.3>@ 0.0
 "reggrid-minedgeratio" 0.4
)


;---------------------------------
; Saving:
(sdeio:save-dfise-bnd (get-body-list) "n@node@_msh_quart.bnd")
(sdedr:write-cmd-file "n@node@_msh_quart.cmd")

(system:command "noffset3d -F tdr n@node@_msh_quart")
(system:command "tdx -mtt -X -ren source=drain  n@node@_msh_quart_pof
n@node@_msh_half")
(system:command "tdx -mtt -y -ren sidegate=sidegate2 n@node@_msh_half
n@node@_msh")
```

As discussed above, conventional (no side-gate) devices can be created at this stage (sde1_dvs.cmd) to provide utmost comparability, by deleting the side-gate and replacing it with SiO_2. Other functionality of the file is similar to file above:

```
;NO SIDE GATE ALTERNATIVE
(part:load "n@node|sdep@_dvs.sat")

(define WL  @<Lpoly/2.0+0.3>@)
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; Changing 0.1 to 0.3
(define WW  @<W+0.3>@)
(define Toffspa 0.004)
(define Tspa    0.08)
; %%%%%%%%%%%%%%%%%%%%%%DopPol change
;(define DopPol  "BoronActiveConcentration")
;(define SGDopPol  "BoronActiveConcentration")
```

```
(define GDopPol  "ArsenicActiveConcentration")

(sdepe:strip-material "Gas")

;%%%%%!!!!!!!!!!!!!!!!!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
;Deleting SideGates !!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
;%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sde:add-material (find-body-id (position 0 @<W+0.1>@ -0.39))  "Oxide"
"RSideGateRSideGate")

;Merge oxides in one single region
(sdegeo:bool-unite (find-material-id "Oxide"))

;Rename the regions
(sde:addmaterial (find-material-id "Silicon")  "Silicon"
"Substrate")
(sde:addmaterial (find-material-id "Oxide")    "Oxide"        "Trench")
(sde:addmaterial (find-material-id "Nitride")  "Nitride"      "Spacer")
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; Changing 0.1 to 0.3
; Create Metal contacts
(sdegeo:set-default-boolean "ABA")
(sdegeo:create-cuboid (position 0.0 0.0 @<-TopRef-0.005>@) (position (-
(- WL (+ Toffspa (+ Tspa (+ @<Lpoly/2.0>@ )))) 0.01) @W@ 0.01) "Metal"
"R.SourceContact")
(sdegeo:create-cuboid (position WL 0.0 0.15) (position (- WL
@<Lpoly/2.0>@) @<W+0.3>@ 0.22) "Metal" "R.GateContact")
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------Metal contact for SG ------------
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
;(sdegeo:create-cuboid (position WL @<W+0.3>@ -0.19) (position 0
@<W+0.1>@ -0.39) "Metal" "R.SideGateContact")


; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------0.1 to 0.3 ------------
; Cut the device
(sdegeo:create-cuboid (position 0.0 0.0 -20) (position WL @<W+0.3>@ -
1.0) "Silicon" "Dummy")
(sdegeo:delete-region (find-body-id (position 0.1 0.1 -5.0)))


; Set Contacts
(sdegeo:define-contact-set "gate"   4.0  (color:rgb 1.0 0.0 0.0 ) "##"
)
(sdegeo:define-contact-set "source" 4.0  (color:rgb 1.0 0.0 0.0 ) "=="
)
(sdegeo:define-contact-set "bulk"   4.0  (color:rgb 1.0 0.0 0.0 )
"<><>" )
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------Metal contact for SG ------------
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
;(sdegeo:define-contact-set "sidegate"   4.0  (color:rgb 1.0 0.0 0.0 )
"[][]" )
```

```
(sdegeo:set-current-contact-set "gate")
(sdegeo:set-contact-boundary-faces (find-body-id (position (- WL
@<Lpoly/4.0>@) @W@ 0.2)))
(sdegeo:delete-region (find-body-id (position (- WL @<Lpoly/4.0>@) @W@
0.2)))

(sdegeo:set-current-contact-set "source")
(sdegeo:set-contact-boundary-faces (find-body-id (position 0.001 0.001
0.0)))
(sdegeo:delete-region (find-body-id (position 0.001 0.001 0.0)))
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------Set contact for SG ------------
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
;(sdegeo:set-current-contact-set "sidegate")
;(sdegeo:set-contact-boundary-faces (find-body-id (position (- WL 0.1)
@<W+0.2>@ -0.29)))
;(sdegeo:delete-region (find-body-id (position (- WL 0.1) @<W+0.2>@ -
0.29)))



(sdegeo:set-current-contact-set "bulk")
(sdegeo:set-contact-faces (find-face-id (position 0.01 0.01 -1.0))
"bulk")
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------Cutting the y=0 side of the device------
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; Cut the device
(sdegeo:create-cuboid (position -1.0 0.001 1.0) (position 1.0 -1.0 -
1.5) "Silicon" "Dummy2")
(sdegeo:delete-region (find-body-id (position -0.5 -0.5 -0.5)))


; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; ---------Change 0.101 to 0.301 ------------
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
;-------------------------------------
; Doping profiles:
(sdedr:define-refinement-window "DataWin" "Cuboid"  (position -0.001 -
0.001 0.201)  (position (+ WL 0.001)  @<W+0.301>@ -1.001) )
(sdedr:define-submesh-placement "Process" "Doping" "DataWin" 0
"NoReplace" 0 0 0 "" "Z" 0)
(sdedr:define-submesh "Doping" "n@node|sde|-1@_fps.tdr" 'r)

;-----------------------------------------------------------------------
; Poly Doping
;%%%%%%%%%%%%%%%%%%%%separation of G and SG
(sdedr:define-constant-profile "GPoly" GDopPol 1e+20)
;(sdedr:define-constant-profile "SGPoly" SGDopPol 1e+20)
;(sdedr:define-constant-profile-material "PolyPlacement" "Poly"
"PolySilicon" 0 "Replace")
(sdedr:define-constant-profile-region "GPolyPlacement" "GPoly"
"RGateRGate" 0 "Replace")
;(sdedr:define-constant-profile-region "SGPolyPlacement" "SGPoly"
"RSideGateRSideGate" 0 "Replace")
```

```
;-------------------------------------
; Meshing Strategy:
# Si refinements
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdedr:define-refinement-window "GateI_RW" "Cuboid"
 (position 0.0 0.0 0.0)  (position WL @<W+0.3>@ -0.15))
(sdedr:define-refinement-size "GateI_RD"
   (/ WL 20)   @<W/8.0>@       0.02
   (/ WL 40)   @<W/10.0>@      0.01 )
(sdedr:define-refinement-placement "GateI_PL" "GateI_RD" "GateI_RW" )
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdedr:define-refinement-window "GOx_RW" "Cuboid"
 (position 0.0 0.0 -0.4) (position WL @<W+0.3>@ -0.15))
(sdedr:define-refinement-size "GOx_RD"
  (/ WL 10)        @<W/8.0>@        0.05
  (/ WL 40)        @<W/10.0>@       0.01 )
(sdedr:define-refinement-placement "GOx_PL" "GOx_RD" "GOx_RW" )
; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdedr:define-refinement-window "Si_RW" "Cuboid"
 (position 0.0 0.0 -1.0)  (position WL @<W+0.3>@ -0.4))
(sdedr:define-refinement-size "Si_RD"
  (/ WL 10)        @<W/8.0>@         0.1
  (/ WL 40)        @<W/10.0>@        0.05 )
(sdedr:define-refinement-placement "Si_PL" "Si_RD" "Si_RW" )

; Offset-Global
(sdenoffset:create-global
  "usebox" "aam"
  "maxangle" 150
  "maxconnect" 1000000
  "background" ""
  "options" "-p junction2 -p surface2 -p del-snps2 -p noffset3d -p
refine -p del-snps -p interpolate -x"
  "triangulate" 0
  "recoverholes" 0
  "hlocal" 0
  "factor" 1.5
  "subdivide" 0
  "terminateline" 3
  "maxedgelength" 0.1
  "maxlevel" 5)



(sdenoffset:create-noffset-interface "region" "Substrate" "Trench"
  "hlocal" 0.0002
  "factor" 1.3
  "window" (- 0.3 Tspa) 0.0 0.0 WL WW -0.15)

(sdenoffset:create-noffset-interface "region" "Trench" "Substrate"
  "hlocal" 0.0002
  "factor" 1.5
  "window" (- 0.3 Tspa) 0.0 0.0 WL WW -0.15)
```

```
(sdenoffset:create-isoline "pnj" "region" "Substrate"
                    "value" 0 "length" 0.0 "species"
"DopingConcentration"
                    "isobgcmode" "dopingmaxg" "bgesize" 0.0125)

(sdenoffset:create-noffset-interface "region" "Substrate" "pnj"
  "hlocal" 0.001
  "factor" 2.0)

; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
(sdenoffset:create-boundary "region" "Substrate" "Trench"
 "reggrid-regmod" "snap"
 "reggrid-uniform"     (/ WL 20)    @<W/8.0>@    0.02
 "reggrid-window"  0.0 0.0 -0.15 WL @<W+0.3>@ 0.0
 "reggrid-minedgeratio" 0.4
)


;---------------------------------
; Saving:
(sdeio:save-dfise-bnd (get-body-list) "n@node@_msh_quart.bnd")
(sdedr:write-cmd-file "n@node@_msh_quart.cmd")

(system:command "noffset3d -F tdr n@node@_msh_quart")
(system:command "tdx -mtt -X -ren source=drain  n@node@_msh_quart_pof
n@node@_msh_half")
;(system:command "tdx -mtt -y -ren sidegate=sidegate2 n@node@_msh_half
n@node@_msh")
(system:command "tdx -mtt -y n@node@_msh_half n@node@_msh")
```

7.2.2 Programming Code for Electrical Characterization Simulations

For side-gated and conventional devices, electrical characterization simulation in Sentaurus Device involves selection of the Physics, the solver and the initial and final state of electrical contacts. Multiple transfer or output curves can be obtained with a single file as shown below, however separating them into multiple files is possible and provides the flexibility needed for parallelization in computing. The following file, for a drain bias (V_d) or 1.0 V, ramps the side-gate voltage to the parametrized value of @Vsg@ which is defined in Sentaurus Workbench, and saves its state for 4 intermediate

stages. Afterwards, gate voltage is ramped to 2.0 V for each side-gate voltage case to obtain transfer characteristics:

```
#define Vd_sat <1.0>


* Define electrodes and their initial conditions.
Electrode{
  { Name="source"   Voltage=0.0 }
  { Name="drain"    Voltage=@Vd_sat@ }
  { Name="gate"     voltage=-2.0 }
  { Name="bulk"         voltage=0.0 }
  { Name="sidegate" voltage=0.0}
  { Name="sidegate2"    voltage=0.0}
}


* Get the input from the previous tool in Sentaurus workbench
File{
  Grid     = "n@previous@_msh.tdr"
  Plot     = "@tdrdat@"
  Current  = "@plot@"
  Output   = "@log@"
}


* Modified Local Density Approximation for electrons only in Silicon.
Physics (material="Silicon"){
  eMLDA
}


* Philips Unified Mobility
* Mobility saturation at high fields as a function of electric field
parallel to interfaces
* Mobility degradation as a function of Electric field normal to
surfaces.
* BandGapNarrowing through OldSlotboom method.
* SRH recombination as a function of doping.
Physics{
  Mobility(
    PhuMob
    HighFieldSaturation( EparallelToInterface )
    Enormal
    )
  EffectiveIntrinsicDensity( OldSlotboom )
  Recombination(SRH(DopingDep))
}


* Plot these (Not all of them will be calculated.)
Plot{
```

```
  eDensity hDensity
  TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
  eMobility hMobility
  eVelocity hVelocity
  eQuasiFermi hQuasiFermi
  eTemperature Temperature * hTemperature
  ElectricField/Vector Potential SpaceCharge
  Doping DonorConcentration AcceptorConcentration
  SRH Band2Band * Auger
  AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
  eGradQuasiFermi/Vector hGradQuasiFermi/Vector
  eEparallel hEparallel eENormal hENormal
  BandGap
  BandGapNarrowing
  Affinity
  ConductionBand ValenceBand
  eBarrierTunneling hBarrierTunneling * BarrierTunneling
  eTrappedCharge  hTrappedCharge
  eGapStatesRecombination hGapStatesRecombination
  eDirectTunnel hDirectTunnel
}


* Solver parameters
Math{
 Extrapolate
  Derivatives
  Avalderivatives
  RelErrControl
  Digits=5
  RHSmin=1e-10
  Notdamped=50
  Iterations=20
  DirectCurrent
  ExitOnFailure
  method=ILS
  TensorGridAniso
  Number_of_Solver_Threads= maximum
}


Solve{

* Initial solution
  Coupled(Iterations=100 LineSearchDamping=1e-8) { Poisson }

* Ramping of the side-gate to @Vsg@ value given in Sentaurus Workbench
* Save the state in 4 equidistant SG values (If Vsg=-3, these values
are -3,-2,-1,0)
  Quasistationary(
     InitialStep=5e-3 Increment=1.5
     MinStep=1e-15 MaxStep=0.1
     Goal{ Name="sidegate" Voltage=@Vsg@ }
     Goal{ Name="sidegate2" Voltage=@Vsg@ }
  ){ Coupled{ Poisson Electron }
```

```
    Save(FilePrefix="n@node@_Vsg" Time=(0.0;0.33;0.66;1) NoOverWrite)
  }

 #define _Vgs_ 2.0


 * Load the first Vsg case (e.g. 0)
 NewCurrentFile="Vsg0"
 Load(FilePrefix="n@node@_Vsg_0000")


 * Ramp the gate voltage to _Vgs_ = 2 (Transfer curve)
 Quasistationary(
    InitialStep=5e-3 Increment=1.35
    MinStep=1e-40 MaxStep=0.1
    Goal{ Name="gate" Voltage=_Vgs_ }
 ){ Coupled{ Poisson Electron }
    CurrentPlot( Time=(Range=(0 1) Intervals=400) )
    Plot(FilePrefix="n@node@_snap0" NoOverWrite
      Time=(0.0;0.5;1)
    )
 }


* Load the second Vsg case (e.g. -1)
 NewCurrentFile="Vsg1"
 Load(FilePrefix="n@node@_Vsg_0001")

 * Get Transfer characteristics
 Quasistationary(
    InitialStep=5e-3 Increment=1.35
    MinStep=1e-40 MaxStep=0.1
    Goal{ Name="gate" Voltage=_Vgs_ }
 ){ Coupled{ Poisson Electron }
    CurrentPlot( Time=(Range=(0 1) Intervals=400) )
    Plot(FilePrefix="n@node@_snap1" NoOverWrite
      Time=(0.0;0.5;1)
    )
 }


 * Load the third Vsg case (e.g. -2)
 NewCurrentFile="Vsg2"
 Load(FilePrefix="n@node@_Vsg_0002")

 * Transfer Curve.
 Quasistationary(
    InitialStep=5e-3 Increment=1.35
    MinStep=1e-40 MaxStep=0.1
    Goal{ Name="gate" Voltage=_Vgs_ }
 ){ Coupled{ Poisson Electron }
    CurrentPlot( Time=(Range=(0 1) Intervals=400) )
    Plot(FilePrefix="n@node@_snap2" NoOverWrite
      Time=(0.0;0.5;1)
    )
```

```
  }


  * Load the fourth Vsg case (e.g. -3)
  NewCurrentFile="Vsg3"
  Load(FilePrefix="n@node@_Vsg_0003")

  * Transfer Curve.
  Quasistationary(
     InitialStep=5e-3 Increment=1.35
     MinStep=1e-40 MaxStep=0.1
     Goal{ Name="gate" Voltage=_Vgs_ }
  ){ Coupled{ Poisson Electron }
     CurrentPlot( Time=(Range=(0 1) Intervals=400) )
     Plot(FilePrefix="n@node@_snap3" NoOverWrite
       Time=(0.0;0.5;1)
     )
  }
}
```

Output characteristics can be obtained in a similar manner by ramping the drain voltage within the 'Quasistationary' statement for multiple cases of gate biases.

For a conventional MOSFET a few things change including the number of electrodes and final ramping. Below is an example:

```
#define Vd_sat <1>
Electrode{
  { Name="source"   Voltage=0.0 }
  { Name="drain"    Voltage=0.0 }
  { Name="gate"     voltage=0.0 }
  { Name="bulk"         voltage=0.0 }

}

File{
  Grid     = "n@node|sde1@_msh.tdr"
  Plot     = "@tdrdat@"
  Current  = "@plot@"
  Output   = "@log@"
}


Physics (material="Silicon"){
  eMLDA
}
```

```
Physics{
    Mobility(
    PhuMob
    HighFieldSaturation( EparallelToInterface )
    Enormal
    )
  EffectiveIntrinsicDensity( OldSlotboom )
  Recombination(SRH(DopingDep))
}


Plot{
eDensity hDensity
  TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
  eMobility hMobility
  eVelocity hVelocity
  eQuasiFermi hQuasiFermi
  eTemperature Temperature * hTemperature
  ElectricField/Vector Potential SpaceCharge
  Doping DonorConcentration AcceptorConcentration
  SRH Band2Band * Auger
  AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
  eGradQuasiFermi/Vector hGradQuasiFermi/Vector
  eEparallel hEparallel eENormal hENormal
  BandGap
  BandGapNarrowing
  Affinity
  ConductionBand ValenceBand
  eBarrierTunneling hBarrierTunneling * BarrierTunneling
  eTrappedCharge  hTrappedCharge
  eGapStatesRecombination hGapStatesRecombination
  eDirectTunnel hDirectTunnel
}


Math{
Extrapolate
  Derivatives
  Avalderivatives
  RelErrControl
  Digits=5
  *RHSmin=1e-10
  Notdamped=50
  Iterations=20
  DirectCurrent
  ExitOnFailure
  method=ILS
  TensorGridAniso
  Number_of_Solver_Threads= maximum
}

Solve{
  Coupled(Iterations=100 LineSearchDamping=1e-8){ Poisson }

 Quasistationary(
```

```
    InitialStep=5e-6 Increment=1.15
    MinStep=1e-48 MaxStep=0.1
    Goal{ Name="drain" Voltage=@Vd_sat@ }
    ){ Coupled{ Poisson Electron }}


* Ramping DOWN the gate to -2V instead of assigning it
* as an initial condition makes convergence easier.
Quasistationary(
    InitialStep=5e-6 Increment=1.15
    MinStep=1e-48 MaxStep=0.1
    Goal{ Name="gate" Voltage=-2.0 }
    ){ Coupled{ Poisson Electron }}

 #define _Vgs_ 2.0

NewCurrentFile="NSG"
 Quasistationary(
    InitialStep=5e-6 Increment=1.15
    MinStep=1e-48 MaxStep=0.1
    Goal{ Name="gate" Voltage=_Vgs_ }
 ){ Coupled{ Poisson Electron }
    CurrentPlot( Time=(Range=(0 1) Intervals=400) )
    Plot(FilePrefix="n@node@_snap0" NoOverWrite
      Time=(0.0;0.5;1)
    )
  }
}
```

7.3 Details of Fabrication Process

This section of the appendix gives a more in-depth view of the fabrication process. Certain details might be omitted since the process was done at a commercial facility with confidential process recipes.

7.3.1 Mask Design

The masks for the photolithography process were designed using the software called Layout Editor. Macros in this software enable automated design features that were used extensively for creating arrays of transistors with increasing channel widths and lengths.

In addition to transistor arrays mentioned above, various other transistor designs with different dimensions, transistor designs assuming alternative processing steps, as well as simple circuits were designed in the mask layout. The layout assumed final printed die dimensions of 10 mm in height and 30 mm in width. After discussing various levels used in the chip design, different portions of the chip and the transistor designs will be explained.

Layout Levels

There are 8 designed levels where 6 levels are utilized in a unipolar transistor design. The levels are explained below, where the two-letter abbreviations for level names are given in brackets.

Active Level (RX): This level is used to define the transistor mesa consisting of source/drain contact pads, self-aligned source/drain regions as well as the transistor channel. Because of its high aspect ratio after mesa definition, this level also contains filler structures to avoid dishing in between transistor mesas during the chemical mechanical polishing (CMP) process that polishes away the STI dielectric.

Side-gate Contact Pad Level (SG): This level is used to define contact pads on the corner of each active area, to mask a portion of poly-silicon from being etched during the spacer RIE process that defines the side-gate structures. In some designs, this level covers the whole active area. Those designs assume an alternative fabrication scheme where all side-gate poly-silicon is removed (by extending the original spacer RIE time), keeping only regions under SG level protected. Then, the poly-silicon that envelopes the active

region is removed through a CMP process. Also in certain designs (e.g. post-modern TFT designs), this level is used as an alternative contact level.

Side-gate contact poly plug (Irrigation Hole) Level (IH): This level is used to define poly-silicon vias that connect the top of STI dielectric with the side-gate contact pad which sits under the STI. In DNA transistors fabrication scheme, this level is used to define small holes on microfluidic irrigation tunnels from which an HF solution would be administered to open those tunnels.

Gate Level (PC): This level is used to define poly-silicon gate structures of FETs. In DNA transistor designs, the contact pads of this level are exceptionally large to prevent delamination upon the clearing of the underlying gate oxide on the transistor channel.

Via Level (CA): This level is used to define via holes between the front end of line (FEOL) levels and the Metal level through the inter-layer dielectric (ILD). For conventional side-gated transistor design, 4 vias appear: 2 for source and drain, 1 for the gate, and 1 on top of the poly plug (IH) for side-gate contact.

Metal Level (M1): This level is used to define metal contact pads that are used for electrical measurements. This level is the last level used in a conventional fabrication scheme.

Irrigation Tunnels Level (IT): In DNA-sensing transistor designs, a microfluidic channel is designed based on an earlier fabrication scheme by Gokirmak [18]. The irrigation tunnels in this scheme would be made of a relatively thin layer of sacrificial

SiO_2 and would be used to deliver Hydrofluoric acid (HF) to remove SiO_2 in these tunnels as well as the SiO_2 in fluidic tunnels. This level is not used in accumulated body FETs.

Fluidic Tunnels Level (FT): Similar to IT level, this level is also used for DNA transistor design and is used to define fluidic tunnels where the DNA solution would be fed through. Its difference from IT level is that the sacrificial SiO_2 for this level is much thicker. HF administered through Irrigation Holes to Irrigation Tunnels would be used to clear the thicker oxide in Fluidic Tunnels to provide a monolithic integration of fluidic channels for DNA sensor designs. This level is not used in accumulated body FETs.

Filler Levels: RXFILL, PCFILL and M1FILL levels were created automatically by an IBM internal design tool, to avoid dishing during the CMP process, due to low coverage area of respective levels. These levels were merged with the device design levels and were printed in the mask along with them.

Other Levels: Due to requirements of the IBM design tool used to generate fillers, additional levels ($OUTLINE, NONIAG, $ALPHA) were automatically created by the same software, but were not included in the printed mask in any way. Details of these levels as well as the others are given in Table 7.1.

Table 7.1. Mask design levels, level numbers in the GDS file, the sequence of use in fabrication, purpose for the level, and the tone of the final printed mask.

Level	**Level Number**	**Build Sequence**	**Purpose**	**Tone**
RX	1	1	Active area	Light Field
SG	4	2	Side-gate contact level	Light Field
IH	5	3	Poly Plug / Irrigation Hole (DNA)	Dark Field
PC	7	4	Gate	Light Field
CA	19	5	Via	Dark Field
M1	22	6	Metal	Dark Field

IT	12	DNA/PMOS	Irrigation Tunnel / Implantation Mask	Light Field
FT	26	DNA	Fluidic Tunnel	Light Field
RXFILL	31	1	RX fillers (combined with RX mask)	Light Field
PCFILL	33	4	PC fillers (combined with PC mask)	Light Field
M1FILL	32	6	M1 fillers (combined with M1 mask)	Dark Field
$OUTLINE	3	N/A	Outline of the design (design only)	N/A
NONIAG	30	N/A	IBM-generated (design only)	N/A
$ALPHA	2	N/A	IBM-generated (design only)	N/A

It is important to note that the tone of the mask mentioned in the table is determined by the process steps involved with the specific level (always assuming positive photoresist). For example, gate (PC) level is a light field, meaning that the designed structures are chrome in the glass mask (giving the impression of a mostly see-through or 'light' mask to the naked eye). During processing, gate polysilicon is desired to be covered by photoresist, so that it will be blocked from the subsequent RIE process. In the same way, via (CA) level is defined as a dark field mask, meaning that everything in the mask will be chrome, except for the designed level (thus giving a 'dark' impression). In the via processing, we would like to cover all of the inter-layer dielectric SiO_2 with photoresist, except for the via structures, so that the RIE process would open up holes which via metal (i.e. tungsten) fills.

Transistor Designs

For practical reasons, five main parts can be distinguished in terms of the die layout (Figure 7.17). Four of those parts, comprising around 80% of the layout area, are transistor arrays of increasing channel widths (W_{design}) and gate lengths (L_{design}).

The fifth part, which is located at the center of the die, has test structures and it will be discussed in section 0.0.0.

In the first generation mask set, two types of arrays are present: the fine array, and the coarse array. One fine array and one coarse array are devoted to DNA transistors and their dimensions are identical to 'penta-gate' fine and coarse arrays.

The fine array dimensions start with W_{design} x L_{design} = 40 nm x 40 nm at upper left corner of the array. With a W_{design} increment of 2 nm per row, and an L_{design} increment of 10 nm per column, a final W_{design} x L_{design} = 104 nm x 210 nm is reached at lower right corner of the array. With 33 rows and 19 columns, the fine array, as well as the coarse array has 627 (33x19) transistors with unique dimensions.

The coarse array follows a similar algorithm in incrementing the dimensions from upper left corner to lower right corner. Starting dimensions for the coarse array are: W_{design} x L_{design} = 60 nm x 60 nm. ΔW_{design} = ΔL_{design} = 20 nm, and the final dimensions are W_{design} x L_{design} = 700 nm x 420 nm.

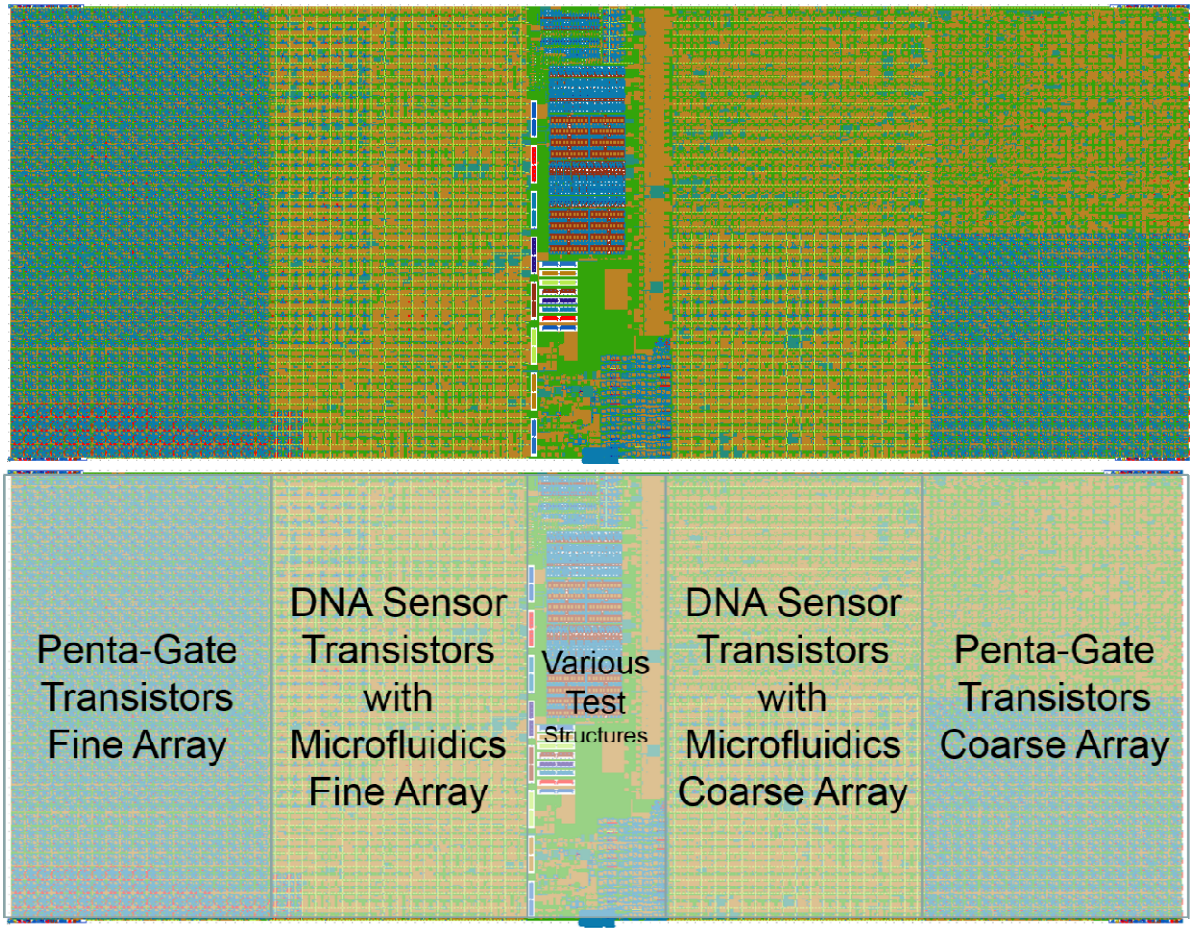


Figure 7.17. (Above) Designed chip layout with all levels visible including fillers and DNA-sensor microfluidic channel designs. (Below) Five regions of the chip labeled with each region's respective design purpose.

The design of individual transistors is similar to conventional narrow channel transistors, with the addition of a side-gate contact pad level in the corner of the active level. A second via level (polysilicon plug) provides access from STI top to the side-gate contact pad. Figure 7.18 shows a transistor-level design with the additional levels defined.

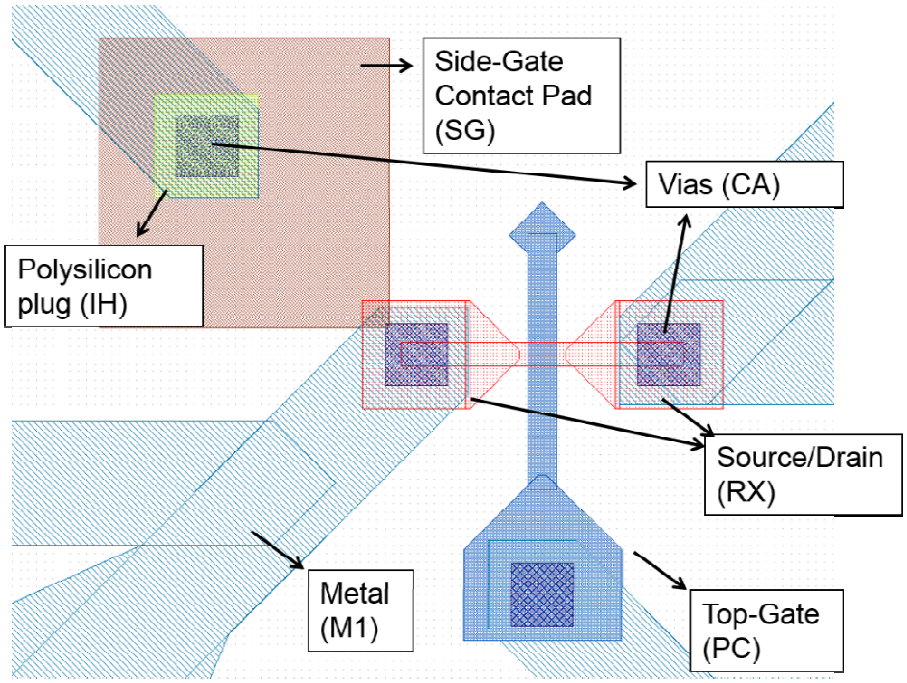


Figure 7.18. Layout of a single transistor showing the design levels and their abbreviations in parentheses.

In order to efficiently design an array of dimensions in the layout, an algorithm was devised. The algorithm, written in a pseudo-C environment of the layout tool (Layout Editor), ensures proper placement of transistors, adjusts contact spacing, and generates and places labels for easy identification under optical microscope. The flow of the algorithm is provided in Figure 7.19.

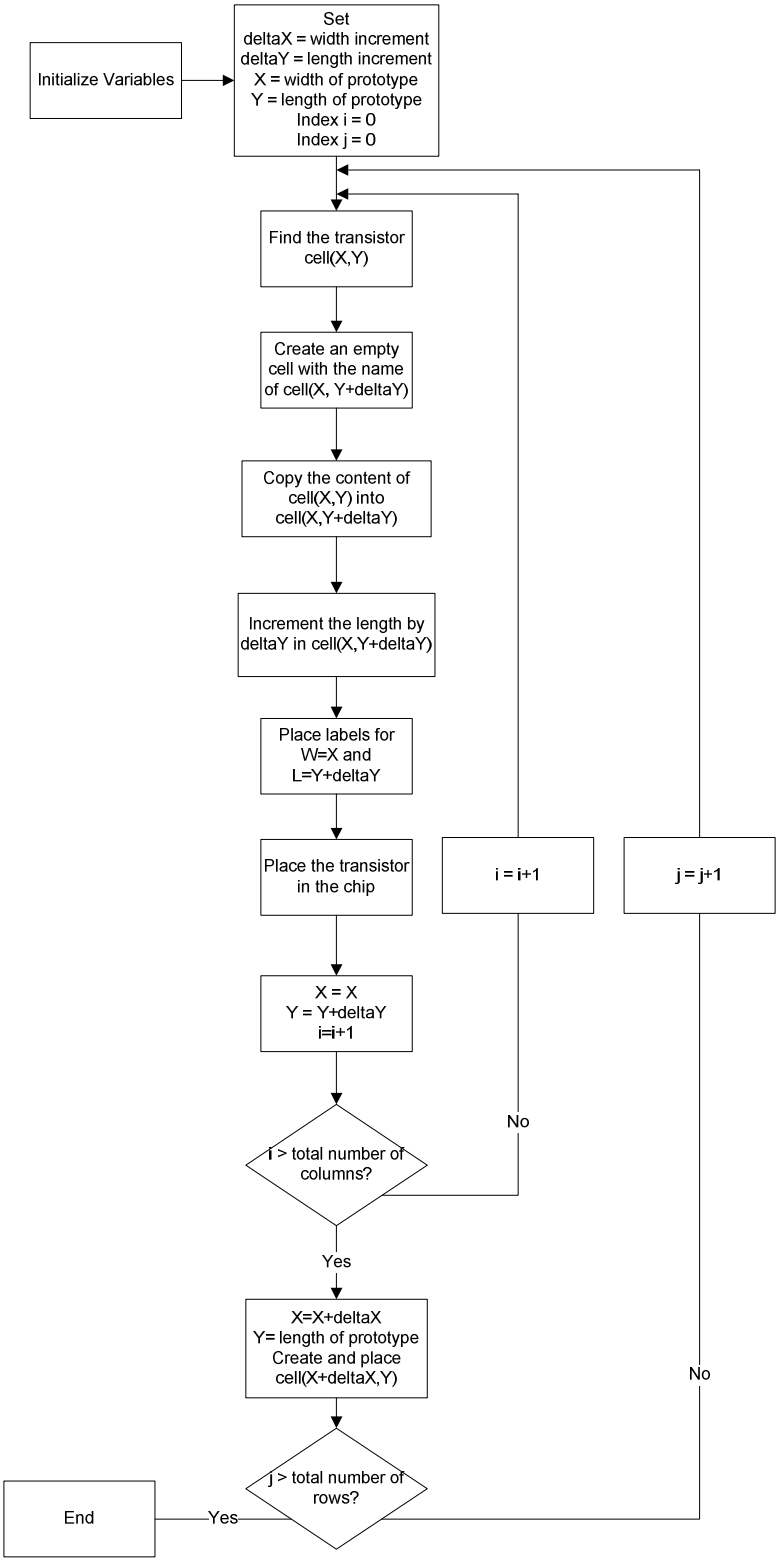


Figure 7.19. Flowchart explaining the macro used to generate an array of transistor designs with increasing gate lengths and channel widths.

Other Designs

The main transistor is one of the many designs on the layout. Other than the main transistor, within the array of varying dimensions, five more transistor layouts take place using the same dimensions of the main transistor.

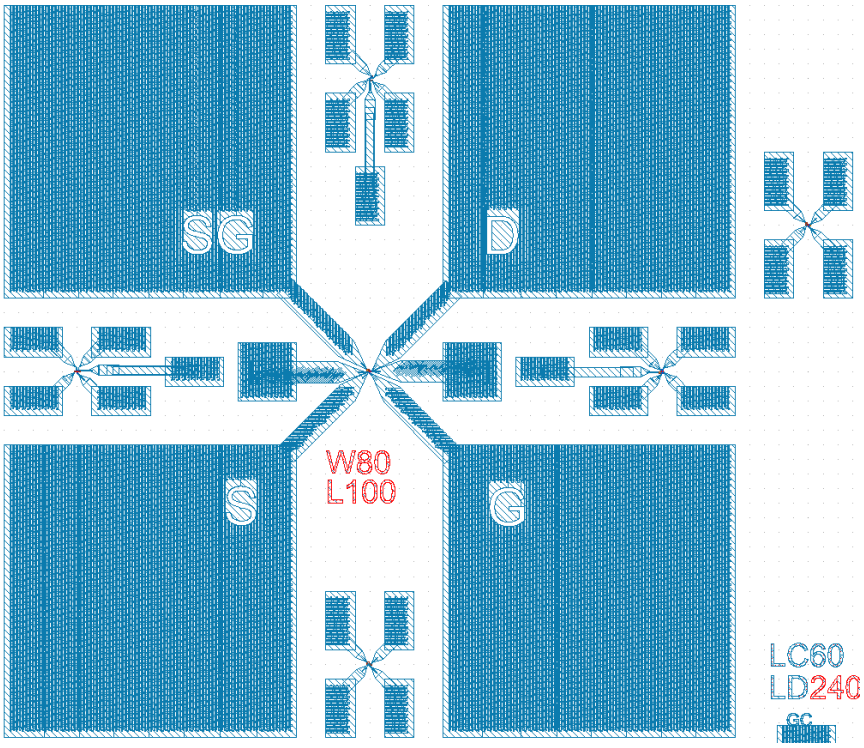


Figure 7.20. A single unit within the array of transistors with varying dimensions. The central feature is the main transistor with bigger contact pads. The other five transistor designs have smaller contact pads but they have same channel width and gate length with the central device (in this case W=80 nm, L=100 nm).

Differential pairs form an array that is embedded in between the array elements of the leftmost fine array. Each unit of the 600-element array includes two transistors that share a common source. Naming one of them the ‘main’ device and the other the

'cooling' device, each device has two L_{design} cases: 60 nm & 240 nm. The W_{design} for each is incremented from 50 nm to 275 nm with ΔW_{design} = 25 nm. Also, as the source contact via can function as a heat sink, distance of the source via to the center was varied from 0 nm in one case to 200 nm and to 500 nm. Table 7.2 describes each type of device and circuit that was included in the design.

Table 7.2. Types of devices and circuits included in the die layout.

Device	**Placement**	**Explanation**
Main Transistor	Arrays	Main transistor design.
Alternative Process Transistor	Arrays	For a process where side-gates are polished down instead of a spacer etch.
Double Side-gate	Arrays	Two side-gate contact pads at the source and drain ends.
Local Side-gate	Arrays	For the alternative process described above with side-gates only appearing under the top gate.
Double Top-gate Contacts	Arrays	Main transistor with two contacts for the gate (for gate crystallization studies)
I-MOS	Arrays	Impact Ionization MOSFET design (with a n-doping mask designed in IT level)
Differential Pairs	Dispersed within arrays	Can be used for source-cooling behavior. Varying dimensions of two transistors sharing a source.
Big/small transistors	Center	Narrow/long, wide/short and wide/long transistors
Capacitors	Center	Side-gate/body, side-gate/gate and gate/body
Ring Oscillators	Center	CMOS and NMOS
Circular FET	Center	Similar to RingFET designs.
Pinching FET	Center	To provide electrostatic pinching of the channel (did not print due to small critical dimensions)
Current Mirrors	Center	Current mirror circuits (two transistors sharing a gate)
SRAM	Center	CMOS SRAM cell
DNA Transistors	Arrays	Center 2 arrays, functions like normal transistors, FT, IT and IH levels can be used to fabricate microfluidic channels to deliver DNA molecules under the transistor gate.
Fluidic array with amplifiers	Center	DNA transistor in a differential amplifier setup with a regular transistor to amplify DNA signal
Fluidic electrodes	Center	Special microfluidic channels where fluid flow can be controlled electrostatically (SG level for bottom electrode, M1 level for top electrode)
Sensors in series	Center	4 DNA transistors sharing a gate/microfluidic channel for serial sensing.

Second Generation Mask Set

Based on various characterization results from experiments, a second generation of the mask set was designed. Five regions of the die layout still persist in this generation with some changes.

The biggest change has been that the number of unique devices has doubled by having 4 types of array in four array regions instead of 2. This was achieved, instead of repeating the fine and coarse arrays for DNA transistors, by having different ranges and increments in dimensions for all 4 regions. The dimensions used are summarized in Table 7.3.

Having a wider selection of devices increases the possibility of having working devices and enables the measurement of roll-off characteristics.

Table 7.3. MOSFET design dimensions for arrays in the old layout (first two rows) and the new layout. All units are in nm except noted.

Array	**Min. W**	**ΔW**	**Max. W**	**Min. L**	**ΔL**	**Max. L**
Fine Array (old)	40	2	104	40	10	220
Coarse Array (old)	60	20	700	60	20	420
Array I (leftmost)	60	2	124	60	10	240
Array II (center-left)	60	4	188	1 µm	5 µm	91 µm
Array III (center-right)	60	20	700	60	40	800
Array IV (rightmost)	60	10	380	60	20	420

Other than the arrays, several structures were introduced with contact pads that are big enough for electrical microprobing before metallization. Bigger areas of various levels have also been introduced in the second generation mask set to facilitate film thickness and profilometry measurements.

Components of a Unit Cell in Transistor Arrays

The following images summarize various designs listed in Table 7.2.

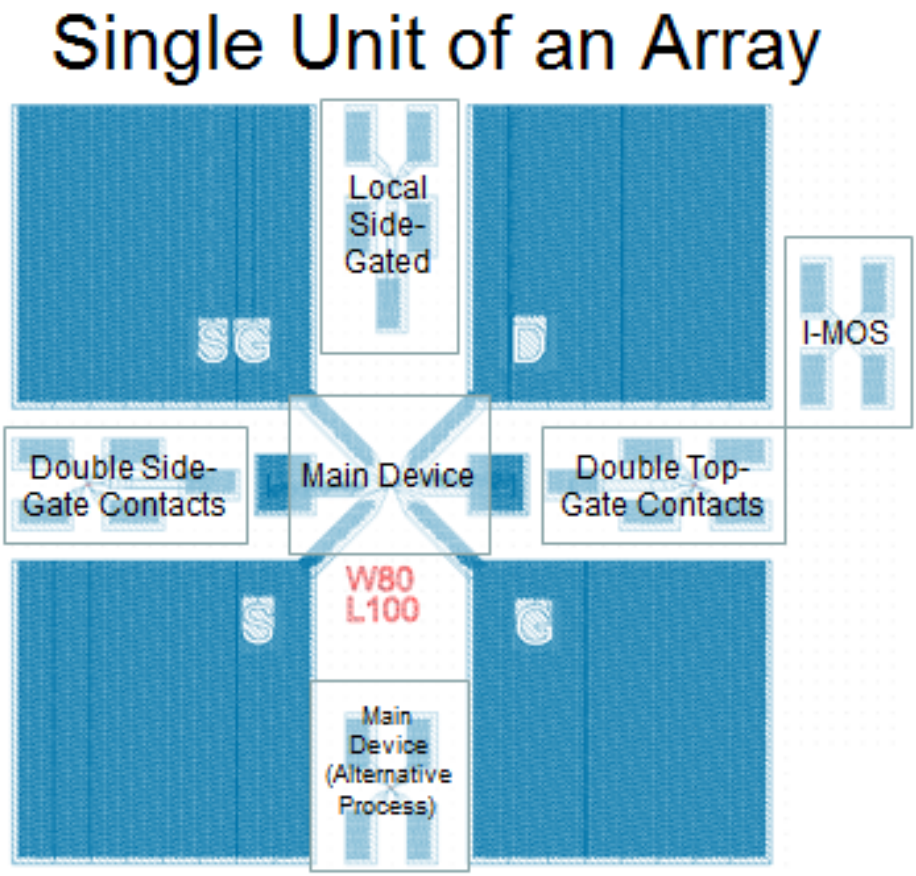


Figure 7.21. Various designs within a unit cell of a transistor array. All 6 designs share the same design width and length.

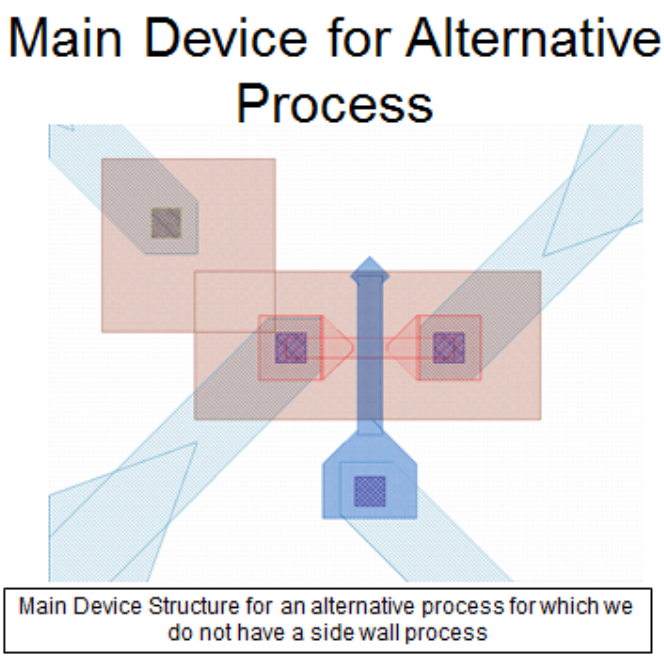


Figure 7.22. This design assumes that a polish step will be used to remove side-gate poly from the top of active region.

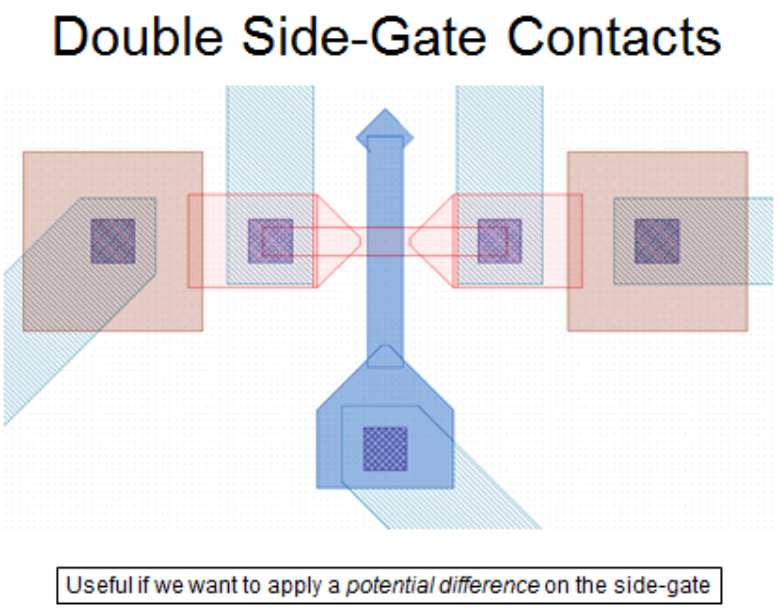


Figure 7.23. This design has two contacts for the side-gate.

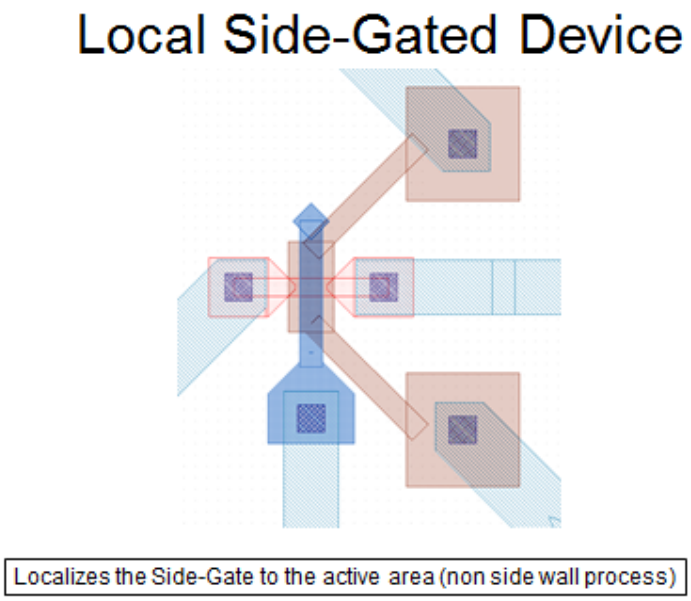


Figure 7.24. This design assumes the 'alternative' process approach. In fabricated devices, the arms connecting side-gate pads to device might not have printed because of their dimensions.

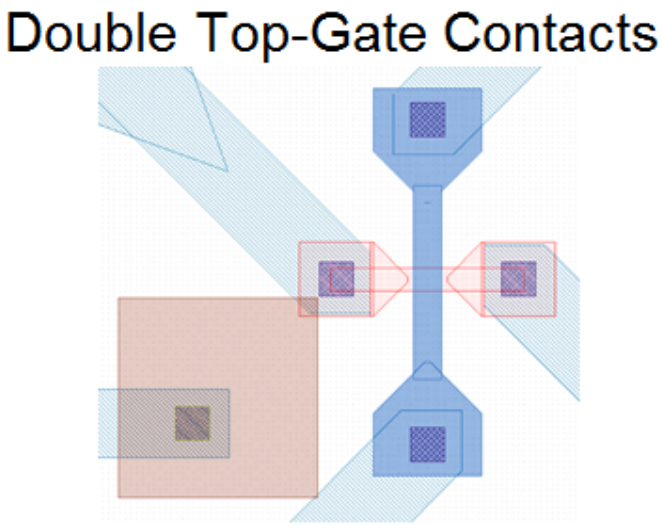


Figure 7.25. This design has two contacts for the top gate.

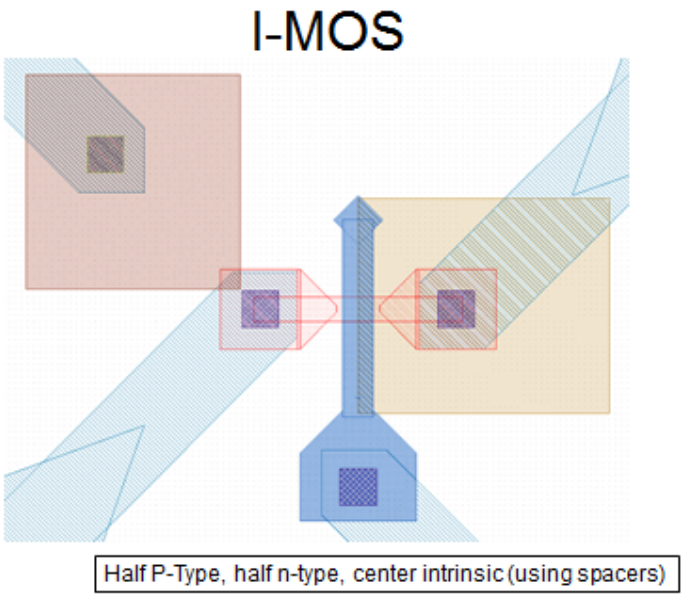


Figure 7.26. This design assumes the use of IH level to dope one half of the channel to create impact ionization MOSFETs. In fabricated devices, these work like the main device.

7.3.2 List of Fabrication Steps.

The table below lists all steps a particular wafer lot (5GATEINT3K51) went through in its processing. This lot is especially important since most electrical results discussed previously use wafer 8 from this lot.

Table 7.4. Detailed list of process steps for the 5GATEINT3K51 lot where wafer 8 provided devices with the best electrical results. On the columns to the right is the split table for the process step. For each step, "_" (green) denotes that the wafer at that slot (1-10) is processed, and "N" (red) denotes a wafer that is not processed.

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
1	CONTROL	Pull wafers		_	_	_	_	_	_	_	_	_	_
2	CONTROL	Record Wafer IDs / Attach Wafer ID Map		_	_	_	_	_	_	_	_	_	_
3	FEOL-WETS	OZONE HUANG CLEAN		_	_	_	_	_	_	_	_	_	_
4	FEOL-WETS	rinse and dry		_	_	_	_	_	_	_	_	_	_
5	I/I	Move from 42187 to I/I	Blanket implantation for body doping	_	_	_	_	_	_	_	_	_	_
6	I/I	I/I - VAR - B - 2-220KV-1.00E11-1.00E14-R1		_	_	_	_	_	_	_	_	_	_
7	I/I	I/I - VAR - B - 2-220KV-1.00E11-1.00E14-R1		_	_	_	_	_	_	_	_	_	_
8	I/I	I/I - VAR - B - 2-220KV-1.00E11-1.00E14-R1		_	_	_	_	_	_	_	_	_	_
9	I/I	Move from I/I to 42187		_	_	_	_	_	_	_	_	_	_
10	HOT	800-900 C ANNEAL		_	_	_	_	_	_	_	_	_	_
11	HOT	MEASURE Tox		_	N	N	N	N	N	N	N	_	_
12	FEOL-WETS	OZONE MOD HUANG CLEAN (X SEC DHF)		_	_	_	_	_	_	_	_	_	_
13	FEOL-WETS	rinse and dry		_	_	_	_	_	_	_	_	_	_
14	RTP	RTP sheet-rho measurement with 4pt probe		_	N	N	N	N	N	N	N	_	_
15	HOT	THIN OXIDE		_	_	_	_	_	_	_	_	_	_
16	HOT	MEASURE Tox		_	N	N	N	N	N	N	N	_	_
17	LPCVD	NITRIDE		_	_	_	_	_	_	_	_	_	_
18	LPCVD	MEASURE FILM THICKNESS/UNIFORMITY		_	_	_	_	_	_	_	_	_	_
19	LPCVD	LTO		_	_	_	_	_	_	_	_	_	_
20	LPCVD	MEASURE FILM THICKNESS/UNIFORMITY		_	_	_	_	_	_	_	_	_	_

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
21	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)		_	_	_	_	_	_	_	_	_	_
22	FEOL-WETS	rinse and dry		_	_	_	_	_	_	_	_	_	_
23	LITH	DUV DUV HM8006-14		N	N	N	N	N	N	N	N	_	_
24	LITH	DUV Confirm film thickness-Nanospec		N	N	N	N	N	N	N	N	_	_
25	LITH	DUV DUV HM8006-14		_	_	_	_	_	_	_	_	_	_
26	DIEL	42006 Wafer transport to aisle 42006 from 42187		_	_	_	_	_	_	_	_	_	_
27	DIEL	42006 200C oxide H450C		N	N	N	N	N	N	N	N	_	_
28	DIEL	42006 thickness measurement on Rudolph		N	N	N	N	N	N	N	N	_	_
29	DIEL	42006 200C oxide H450C		_	_	_	_	_	_	_	_	_	_
30	TEST-INIT	Initiator Coordination		_	_	_	_	_	_	_	_	_	_
31	LITH	193 TRANSFER WAFERS TO SCANNER	Litho Recipe creation	_	_	_	_	_	_	_	_	_	_
32	LITH	193 193-Reticle Transmission Measurement on New Mask		_	N	N	N	N	N	N	N	_	_
33	LITH	193 ASML recipe creation		N	N	N	N	N	N	N	N	_	_
34	LITH	193 5Gate RX - Integrated		N	N	N	N	N	N	_	N	_	_
35	METROLOGY	VERASEM RECIPE CREATION		N	N	N	N	N	N	_	N	_	_
36	METROLOGY	Verasem SAHD CD Meas single target		N	N	N	N	N	N	_	N	_	_
37	TEST-INIT	Initiator Coordination		N	N	N	N	N	N	_	N	_	_
38	LITH	193 TRANSFER WAFERS TO SCANNER	Process window analysis for Litho focus and exposure	N	N	N	N	N	N	N	_	_	_
39	LITH	193 Non-standard coat w/ Recipe Creation		N	N	N	N	N	N	N	_	_	_
40	LITH	193 193 ASML STEPPER FOCUS EXPOSURE MATRIX		N	N	N	N	N	N	N	_	_	_
41	METROLOGY	Verasem SAHD CD Meas single target		N	N	N	N	N	N	N	_	_	_
42	METROLOGY	Process Window Analysis		N	N	N	N	N	N	N	_	_	_

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
43	LITH	193 TRANSFER WAFERS TO 42187 Lab		N	N	N	N	N	N	N	_	_	_
44	LITH	DUV O2 plasma Gasonics		N	N	N	N	N	N	_	_	_	_
45	LITH	193 TRANSFER WAFERS TO SCANNER		N	N	N	N	N	N	_	_	_	_
46	LITH	193 Non-standard coat w/ Recipe Creation		N	N	N	N	N	N	_	N	_	_
47	LITH	193 193 ASML STEPPER FOCUS EXPOSURE MATRIX		N	N	N	N	N	N	_	N	_	_
48	METROLOGY	Focus Exposure Matrix		N	N	N	N	N	N	_	N	_	_
49	METROLOGY	Process Window Analysis		N	N	N	N	N	N	_	N	_	_
50	LITH	193 TRANSFER WAFERS TO 42187 Lab		N	N	N	N	N	N	_	_	_	_
51	LITH	193 PEB Bake		N	N	N	N	N	N	_	N	_	_
52	METROLOGY	JEOL SEM Inspection		N	N	N	N	N	N	N	_	_	_
53	LITH	DUV O2 plasma Gasonics		N	N	N	N	N	N	_	N	_	_
54	LITH	193 TRANSFER WAFERS TO SCANNER		N	N	N	N	N	N	_	_	_	_
55	LITH	193 Non-standard coat w/ Recipe Creation		N	N	N	N	N	N	_	N	_	_
56	LITH	193 193 ASML STEPPER FOCUS EXPOSURE MATRIX		N	N	N	N	N	N	_	N	_	_
57	METROLOGY	Focus Exposure Matrix		N	N	N	N	N	N	_	N	_	_
58	METROLOGY	Process Window Analysis		N	N	N	N	N	N	_	N	_	_
59	LITH	193 TRANSFER WAFERS TO 42187 Lab		N	N	N	N	N	N	_	_	_	_
60	LITH	193 TRANSFER WAFERS TO SCANNER		_	_	_	_	_	_	_	_	_	_
61	LITH	193 5Gate RX - Integrated	Monitor wafers through litho	N	N	N	N	N	N	N	_	_	_
62	METROLOGY	Verasem SAHD CD Meas single target		N	N	N	N	N	N	N	_	_	_
63	LITH	193 TRANSFER WAFERS TO 42187 Lab		_	_	_	_	_	_	_	_	_	_
64	TEST-INIT	1.5-hr test		N	N	N	N	N	N	N	_	_	_
65	LITH	DUV O2 plasma Gasonics		N	N	N	N	N	N	_	_	_	_

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
66	LITH	193 TRANSFER WAFERS TO SCANNER		N	N	N	N	N	N	_	_	_	_
67	LITH	193 5Gate RX - Integrated		N	N	N	N	N	N	_	N	_	_
68	METROLOGY	Verasem SAHD CD Meas single target		N	N	N	N	N	N	_	N	_	_
69	TEST-INIT	Initiator Coordination- 1 hr		N	N	N	N	N	N	_	N	_	_
70	LITH	193 5Gate RX - Integrated		_	_	_	_	_	_	N	_	_	_
71	METROLOGY	Verasem CD Meas 1 target		_	N	N	N	N	N	N	N	_	_
72	TEST-INIT	Initiator Coordination- 1 hr		N	N	N	N	N	N	N	N	_	_
73	LITH	193 TRANSFER WAFERS TO 42187 Lab		_	_	_	_	_	_	_	_	_	_
74	RIE	42218 Y56A DPS II Cold Cathode Experimental	Monitor wafers through RIE	N	N	N	N	N	N	_	N	_	_
75	ANALYSIS	Pull Wafer for SEM		N	N	N	N	N	N	_	N	_	_
76	ANALYSIS	SEM TOP DOWN Low Voltage		N	N	N	N	N	N	_	N	_	_
77	ANALYSIS	Transport Wafers to 42187		N	N	N	N	N	N	_	N	_	_
78	TEST-INIT	Initiator Coordination		N	N	N	N	N	N	_	N	_	_
79	RIE	42218 Y56A DPS II Cold Cathode Experimental		N	N	N	N	N	N	N	_	_	_
80	TEST-INIT	4-hr test		N	N	N	N	N	N	N	_	_	_
81	LITH	DUV O2 plasma Gasonics		N	N	N	N	N	N	N	_	_	_
82	TEST-INIT	4-hr test		N	N	N	N	N	N	N	_	_	_
83	RIE	42218 Y56A DPS II Cold Cathode Experimental		_	_	N	N	N	N	N	N	_	_
84	RIE	42218 Y56A DPS II Cold Cathode Experimental		N	N	_	_	N	N	N	N	_	_
85	RIE	42218 Y56A DPS II Cold Cathode Experimental	STI Etching	N	N	N	N	_	_	N	N	_	_
86	LITH	DUV O2 plasma Gasonics		_	_	_	_	_	_	N	_	_	_
87	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		_	_	_	_	_	_	N	_	_	_
88	FEOL-WETS	SPIN,RINSE AND DRY		_	_	_	_	_	_	N	_	_	_
89	RIE	42187 Y58 P-15 Profilometry (No Metals)		_	_	_	_	_	_	N	_	_	_

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
		Tencor 42187											
90	TEST-INIT	4-hr test		_	_	_	_	_	_	_	_	_	_
91	METROLOGY	JEOL SEM Inspection		_	_	_	_	_	_	N	_	_	_
92	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)		_	_	_	_	_	_	N	_	_	_
93	FEOL-WETS	SPIN,RINSE AND DRY		_	_	_	_	_	_	N	_	_	_
94	HOT	THICK OXIDE	Oxidation for device thinning (100, 130, 50 nm respectively)	_	_	N	N	N	N	N	N	_	_
95	HOT	MEASURE Tox		N	N	N	N	N	N	N	N	_	_
96	HOT	THICK OXIDE		N	N	_	_	_	N	N	N	_	_
97	HOT	MEASURE Tox		N	N	N	N	N	N	N	N	_	_
98	HOT	THICK OXIDE		N	N	N	N	N	_	N	N	_	_
99	HOT	MEASURE Tox		N	N	N	N	N	N	N	N	_	_
100	TEST-INIT	4-hr test		N	N	N	N	N	N	N	N	_	_
101	FEOL-WETS	0.417361111111111 DHF ETCH		N	N	_	N	N	N	N	N	_	_
102	FEOL-WETS	rinse and dry		N	N	_	N	N	N	N	N	_	_
103	TEST-INIT	Initiator Coordination		N	N	_	N	N	N	N	N	_	_
104	FEOL-WETS	0.417361111111111 DHF ETCH		N	_	N	N	N	N	N	N	_	_
105	FEOL-WETS	rinse and dry		N	_	N	N	N	N	N	N	_	_
106	FEOL-WETS	0.417361111111111 DHF ETCH		N	N	N	N	_	N	N	N	_	_
107	FEOL-WETS	rinse and dry		N	N	N	N	_	N	N	N	_	_
108	TEST-INIT	Initiator Coordination		N	_	N	N	_	N	N	N	_	_
109	FEOL-WETS	0.417361111111111 DHF ETCH		N	_	N	N	_	N	N	N	_	_
110	FEOL-WETS	rinse and dry		N	_	N	N	_	N	N	N	_	_
111	TEST-INIT	Initiator Coordination		N	_	N	N	_	N	N	N	_	_
112	RTCVD	Exploratory process development	Hydrogen annealing	N	N	N	_	N	N	N	N	_	_

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
113	TEST-INIT	1.5-hr test		N	N	N	_	N	N	N	N	_	_
114	ANALYSIS	Pull Wafer for SEM		N	N	N	_	N	N	N	N	_	_
115	ANALYSIS	SEM TOP DOWN Low Voltage		N	N	N	_	N	N	N	N	_	_
116	ANALYSIS	Transport Wafers to 42187		N	N	N	_	N	N	N	N	_	_
117	FEOL-WETS	Post-SEM Spin Rinse Dry and Return to Box		N	N	N	_	N	N	N	N	_	_
118	FEOL-WETS	Post-SEM Spin Rinse Dry and Return to Box		_	N	N	N	N	N	N	N	_	_
119	TEST-INIT	1.5-hr test		N	N	N	_	N	N	N	N	_	_
120	I/I	Move from 42187 to I/I		N	N	_	N	N	N	N	N	_	_
121	I/I	I/I - VAR - B - 2-220KV-1.00E11-1.00E14-R4		N	N	_	N	N	N	N	N	_	_
122	I/I	Move from I/I to 42187		N	N	_	N	N	N	N	N	_	_
123	RTP	Ch C RTA: uniform backside, no metals		N	N	_	N	N	N	N	N	_	_
124	TEST-INIT	Initiator Coordination	Additional body doping	N	N	_	N	N	N	N	N	_	_
125	I/I	Move from 42187 to I/I		_	N	N	N	_	_	N	N	_	_
126	I/I	I/I - VAR - B - 2-220KV-1.00E11-1.00E14-R4		_	N	N	N	_	_	N	N	_	_
127	I/I	Move from I/I to 42187		_	N	N	N	_	_	N	N	_	_
128	RTP	Ch C RTA: uniform backside, no metals		_	N	N	N	_	_	N	N	_	_
129	TEST-INIT	Initiator Coordination		_	N	N	N	_	_	N	N	_	_
130	HOT	GSC - FURNACE OXIDE	coordination step	_	_	_	N	N	_	N	_	_	_
131	FEOL-WETS	OZONE MOD HUANG CLEAN (X SEC DHF)	oxidation pre-clean	_	_	_	N	N	_	N	_	_	_
132	FEOL-WETS	SPIN,RINSE AND DRY		_	_	_	N	N	_	N	_	_	_
133	RTP	Ch C GATE OXIDE - DRY	9 nm oxide	_	_	_	N	N	_	N	_	_	_
134	RTP	MEASURE FILM THICKNESS/UNIFORMITY		N	N	N	N	N	N	N	N	N	N
135	RTCVD	Exploratory process development	50 nm pre-doped poly	_	_	_	N	N	_	N	_	_	_
136	RTCVD	MEASURE FILM THICKNESS/UNIFORMITY		N	N	N	N	N	N	N	N	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
137	HOT	GSC - FURNACE OXIDE	coordination step (ONO)	N	N	N	_	_	N	N	N	_	_
138	FEOL-WETS	OZONE MOD HUANG CLEAN (X SEC DHF)	oxidation pre-clean	N	N	N	_	_	N	N	N	_	_
139	FEOL-WETS	SPIN,RINSE AND DRY		N	N	N	_	_	N	N	N	_	_
140	RTP	Ch C GATE OXIDE - DRY	4 nm oxide	N	N	N	_	_	N	N	N	_	_
141	RTP	MEASURE FILM THICKNESS/UNIFORMITY		N	N	N	N	N	N	N	N	_	_
142	RTCVD	Ch A Metal Gate Nitride	10 nm nitride	N	N	N	_	_	N	N	N	_	_
143	HOT	GSC - FURNACE OXIDE		N	N	N	_	_	N	N	N	_	_
144	RTCVD	Ch A Metal Gate Oxide SiH4-N2O	3 nm oxide	N	N	N	_	_	N	N	N	_	_
145	RTCVD	Exploratory process development	50 nm pre-doped poly	N	N	N	_	_	N	N	N	_	_
146	RTCVD	MEASURE FILM THICKNESS/UNIFORMITY		N	N	N	N	N	N	N	N	_	_
147	TEST-INIT	4-hr test		N	N	N	_	_	N	N	N	_	_
148	RTP	541C RTA		_	_	_	_	_	_	N	_	_	_
149	FEOL-WETS	OZONE HUANG CLEAN		_	_	_	_	_	_	N	_	_	_
150	FEOL-WETS	SPIN,RINSE AND DRY		_	_	_	_	_	_	N	_	_	_
151	LITH	193 TRANSFER WAFERS TO SCANNER	Litho experiments for SG level.	_	_	_	_	_	_	N	_	_	_
152	LITH	193 5Gate SG - Integrated		N	N	N	N	N	N	N	_	_	_
153	METROLOGY	Verasem SAHD CD Meas single target		N	N	N	N	N	N	N	_	_	_
154	TEST-INIT	Initiator Coordination		_	_	_	_	_	_	N	N	_	_
155	LITH	DUV O2 plasma Gasonics		N	N	N	N	N	N	N	_	_	_
156	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		N	N	N	N	N	N	N	_	_	_
157	LITH	193 TRANSFER WAFERS TO SCANNER		N	N	N	N	N	N	N	_	_	_
158	LITH	193 5Gate SG - Integrated		N	N	N	N	N	N	N	_	_	_
159	TEST-INIT	1.5-hr test		N	N	N	N	N	N	N	N	_	_
160	LITH	DUV O2 plasma Gasonics		N	N	N	N	N	N	N	_	_	_

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	8	9	10
161	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		N	N	N	N	N	N	N	_	_	_
162	FEOL-WETS	rinse and dry		N	N	N	N	N	N	N	_	_	_
163	LITH	193 TRANSFER WAFERS TO SCANNER		N	N	N	N	N	N	N	_	_	_
164	LITH	193 5Gate SG - Integrated		N	N	N	N	N	N	N	_	_	_
165	METROLOGY	TRANSFER WAFERS TO 42187		_	_	_	_	_	_	N	_	_	_
166	METROLOGY	JEOL SEM Inspection		_	_	_	_	_	_	N	_	_	_
167	RIE	42218 Y56A DPS II Cold Cathode Experimental	side-gate poly spacer etch	N	N	N	N	N	N	N	N	N	N
168	RIE	42218 Y56A DPS II Cold Cathode Experimental		N	N	N	N	N	N	N	_	_	_
169	ANALYSIS	Pull Wafer for SEM		N	N	N	N	N	N	N	_	_	_
170	ANALYSIS	SEM TOP DOWN Low Voltage		N	N	N	N	N	N	N	_	_	_
171	ANALYSIS	Transport Wafers to 42187		N	N	N	N	N	N	N	_	_	_
172	TEST-INIT	Initiator Coordination		N	N	N	N	N	N	N	_	_	_
173	LITH	DUV O2 plasma Gasonics		N	N	N	N	N	N	N	_	_	_
174	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		N	N	N	N	N	N	N	_	_	_
175	FEOL-WETS	rinse and dry		N	N	N	N	N	N	N	_	_	_
176	TEST-INIT	4-hr test		N	N	N	N	N	N	N	_	_	_
177	METROLOGY	JEOL SEM Inspection		N	N	N	N	N	N	N	_	_	_
178	LITH	193 TRANSFER WAFERS TO SCANNER		_	_	_	_	_	_	N	N	_	_
179	LITH	193 5Gate SG - Integrated		_	_	_	_	_	_	N	N	_	_
180	METROLOGY	TRANSFER WAFERS TO 42187		_	_	_	_	_	_	N	N	_	_
181	TEST-INIT	Initiator Coordination		_	_	_	_	_	_	N	N	N	N
182	LITH	DUV O2 plasma Gasonics		_	_	_	_	_	_	N	N	N	N
183	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		_	_	_	_	_	_	N	N	N	N
184	FEOL-WETS	SPIN,RINSE AND DRY		_	_	_	_	_	_	N	N	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
185	LITH	193 TRANSFER WAFERS TO SCANNER		_	_	_	_	_	_	N	N	N	N
186	LITH	193 5Gate SG - Integrated		_	_	_	_	_	_	N	N	N	N
187	METROLOGY	TRANSFER WAFERS TO 42187		_	_	_	_	_	_	N	N	N	N
188	TEST-INIT	Initiator Coordination		_	_	_	_	_	_	N	N	N	N
189	RIE	42218 Y56A DPS II Cold Cathode Experimental		_	_	_	_	_	_	N	N	_	_
190	TEST-INIT	4-hr test		_	_	_	_	_	_	N	N	_	_
191	ANALYSIS	Pull Wafer for SEM		N	N	_	N	N	N	N	N	N	N
192	ANALYSIS	SEM TOP DOWN Low Voltage		N	N	_	N	N	N	N	N	N	N
193	ANALYSIS	Transport Wafers to 42187		N	N	_	N	N	N	N	N	N	N
194	LITH	DUV O2 plasma Gasonics		_	_	_	_	_	_	N	N	_	_
195	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		_	_	_	_	_	_	N	N	_	_
196	FEOL-WETS	SPIN,RINSE AND DRY		_	_	_	_	_	_	N	N	_	_
197	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)		_	_	_	_	_	_	N	_	_	_
198	FEOL-WETS	rinse and dry		_	_	_	_	_	_	N	_	_	_
199	ANALYSIS	Pull Wafer for SEM		_	N	N	N	N	N	N	N	_	_
200	ANALYSIS	SEM TOP DOWN Low Voltage		_	N	N	N	N	N	N	N	_	_
201	ANALYSIS	Transport Wafers to 42187		_	N	N	N	N	N	N	N	_	_
202	TEST-INIT	1.5-hr test		_	N	N	N	N	N	N	N	_	_
203	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)		_	_	_	_	_	_	N	_	_	_
204	FEOL-WETS	rinse and dry		_	_	_	_	_	_	N	_	_	_
205	RTP	Ch C GATE OXIDE - DRY	oxidation to cure etch damage	_	_	_	_	_	_	N	_	_	_
206	RTP	MEASURE FILM THICKNESS/UNIFORMITY		N	N	N	N	N	N	N	N	_	_
207	FILMS	42006 wafer transport from 42187 ingating	STI Oxide deposition (900 nm)	_	_	_	_	_	_	N	_	_	_
208	FILMS	42006 STI HDP OXIDE H449B ~600C		N	N	N	N	N	N	N	N	_	_

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
209	FILMS	42006 thickness measurement		N	N	N	N	N	N	N	N	N	N
210	FILMS	42006 STI HDP OXIDE H449B ~600C		_	_	_	_	_	_	N	_	_	_
211	FILMS	42006 wafer transport from 42006 to 42187 in gating		_	_	_	_	_	_	N	_	_	_
212	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)		_	_	_	_	_	_	N	_	_	_
213	FEOL-WETS	rinse and dry		_	_	_	_	_	_	N	_	_	_
214	HOT	800-900 C ANNEAL	HDP densification	_	_	_	_	_	_	N	_	_	_
215	POLISH	Pre STI CMP-Wafer Transport to CMP lab	Pre-plug STI CMP	_	_	_	_	_	_	N	_	_	_
216	POLISH	CMP...PLEASE READ FIRST		N	N	N	N	N	N	N	N	N	N
217	POLISH	** CMP ONLY ** - UV1280 Thickness Measurement		_	_	_	_	_	_	N	_	_	_
218	POLISH	Development for CA oxide polish		_	_	_	_	_	_	N	_	_	_
219	POLISH	LEICA Optical Inspection (Ebara)		_	_	_	_	_	_	N	_	_	_
220	POLISH	** CMP ONLY ** - UV1280 Thickness Measurement		_	_	_	_	_	_	N	_	_	_
221	POLISH	Post STI CMP- Wafer Transport to 42187 Changeroom		_	_	_	_	_	_	N	_	_	_
222	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		_	_	_	_	_	_	N	_	_	_
223	FEOL-WETS	SPIN,RINSE AND DRY		_	_	_	_	_	_	N	_	_	_
224	LITH	193 TRANSFER WAFERS TO SCANNER		_	_	_	_	_	_	N	_	_	_
225	LITH	193 Dry Align (no resist) to test alignment		_	N	N	N	N	N	N	N	N	N
226	LITH	193 5Gate IH - Integrated	IH level Litho experiments	_	N	N	N	N	N	N	N	_	_
227	METROLOGY	Q7 RECIPE CREATION		_	N	N	N	N	N	N	N	N	N
228	METROLOGY	Q7 OVERLAY MEASURE with Mean Plus 2-Sigma		_	N	N	N	N	N	N	N	_	_
229	METROLOGY	VERASEM RECIPE CREATION		_	N	N	N	N	N	N	N	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
230	METROLOGY	Verasem SAHD CD Meas single target		_	N	N	N	N	N	N	N	_	_
231	TEST-INIT	1.5-hr test		N	N	N	N	N	N	N	N	N	N
232	LITH	193 5Gate IH - Integrated		N	_	N	N	N	N	N	N	N	N
233	METROLOGY	Q7 RECIPE CREATION		N	_	N	N	N	N	N	N	N	N
234	METROLOGY	Q7 OVERLAY MEASURE with Mean Plus 2-Sigma		N	_	N	N	N	N	N	N	_	_
235	METROLOGY	Verasem CD Meas 1 target		N	_	N	N	N	N	N	N	_	_
236	LITH	193 5Gate IH - Integrated		N	N	_	_	_	_	N	_	N	N
237	METROLOGY	Q7 OVERLAY MEASURE with Mean Plus 2-Sigma	Overlay measurement	N	N	_	N	N	N	N	N	N	N
238	METROLOGY	Verasem CD Meas 1 target	Critical dim. meas.	N	N	_	N	N	N	N	N	N	N
239	METROLOGY	TRANSFER WAFERS TO 42187		_	_	_	_	_	_	N	_	_	_
240	RIE	42187 Y12B - IPS - Experimental	Etch-SEM-Etch-SEM cycles for the etching of STI for polysilicon plug (via)	_	_	_	_	_	_	N	_	_	_
241	TEST-INIT	24-hour test		_	_	_	_	_	_	N	_	N	N
242	RIE	42187 Y12B - IPS - Experimental		_	N	N	N	N	N	N	N	N	N
243	TEST-INIT	1.5-hr test		_	N	N	N	N	N	N	N	N	N
244	RIE	42187 Y12B - IPS - Experimental		_	N	N	N	N	N	N	N	N	N
245	RIE	42187 Y58 P-15 Profilometry (No Metals) Tencor 42187		_	N	N	N	N	N	N	N	N	N
246	TEST-INIT	1.5-hr test		_	N	N	N	N	N	N	N	N	N
247	RIE	42187 Y12B - IPS - Experimental		_	N	N	N	N	N	N	N	N	N
248	TEST-INIT	1.5-hr test		_	N	N	N	N	N	N	N	N	N
249	RIE	42187 Y12B - IPS - Experimental		N	N	N	N	N	N	N	_	N	N
250	TEST-INIT	1.5-hr test		N	N	N	N	N	N	N	_	N	N
251	RIE	42187 Y12B - IPS - Experimental		N	N	N	N	N	N	N	_	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
252	TEST-INIT	1.5-hr test		N	N	N	N	N	N	N	_	N	N
253	RIE	42187 Y12B - IPS - Experimental		N	_	_	_	_	_	N	N	N	N
254	TEST-INIT	1.5-hr test		N	_	_	_	_	_	N	N	N	N
255	RIE	42187 Y12B - IPS - Experimental		N	_	_	_	N	N	N	N	N	N
256	RIE	42187 Y12B - IPS - Experimental		N	N	N	N	_	N	N	N	N	N
257	RIE	42187 Y12B - IPS - Experimental		N	N	N	N	N	_	N	N	N	N
258	FEOL-WETS	Post-SEM Spin Rinse Dry and Return to Box		_	_	_	_	_	_	N	_	N	N
259	TEST-INIT	1.5-hr test		N	_	_	_	_	_	N	N	N	N
260	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)		_	_	_	_	_	_	N	_	N	N
261	FEOL-WETS	OZONE MOD HUANG CLEAN (X SEC DHF)		N	N	_	N	N	N	N	N	N	N
262	FEOL-WETS	rinse and dry		_	_	_	_	_	_	N	_	_	_
263	TEST-INIT	1.5-hr test		N	N	_	N	N	N	N	N	N	N
264	LITH	DUV O2 plasma Gasonics		_	_	N	_	_	_	N	_	N	N
265	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		_	_	N	_	_	_	N	_	N	N
266	FEOL-WETS	rinse and dry		_	_	N	_	_	_	N	_	N	N
267	TEST-INIT	1.5-hr test		_	_	N	_	_	_	N	_	N	N
268	TEST-INIT	24-hour test		N	N	N	N	N	N	N	N	N	N
269	RTCVD	EPI COORDINATION		N	N	N	N	N	N	N	_	N	N
270	FEOL-WETS	OZONE MOD HUANG CLEAN (X SEC DHF)		N	N	N	N	N	N	N	_	N	N
271	FEOL-WETS	rinse and dry		N	N	N	N	N	N	N	_	N	N
272	RTCVD	Exploratory process development	Poly plug deposition (250 nm)	N	N	N	N	N	N	N	_	N	N
273	RTCVD	MEASURE FILM THICKNESS/UNIFORMITY		N	N	N	N	N	N	N	N	_	_
274	TEST-INIT	1.5-hr test	CMP to clear excess poly	N	N	N	N	N	N	N	_	N	N
275	POLISH	Pre STI CMP-Wafer Transport to CMP lab		N	N	N	N	N	N	N	_	N	N
276	POLISH	CMP...PLEASE READ FIRST		N	N	N	N	N	N	N	_	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
277	POLISH	** CMP UV1280 Film Measurement & Recipe Creation		N	N	N	N	N	N	N	_	N	N
278	POLISH	Polish 1 - Poly-Si		N	N	N	N	N	N	N	_	N	N
279	POLISH	LEICA Optical Inspection (Westech)		N	N	N	N	N	N	N	_	N	N
280	POLISH	** CMP ONLY ** - UV1280 Thickness Measurement		N	N	N	N	N	N	N	_	N	N
281	POLISH	Post STI CMP- Wafer Transport to 42187 Changeroom		N	N	N	N	N	N	N	_	N	N
282	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		N	N	N	N	N	N	N	_	N	N
283	FEOL-WETS	rinse and dry		N	N	N	N	N	N	N	_	N	N
284	LITH	DUV O2 plasma Gasonics	reworking of two wafers from STI up.	N	N	_	N	N	N	N	N	N	N
285	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		N	N	_	N	N	N	N	N	N	N
286	FEOL-WETS	SPIN,RINSE AND DRY		N	N	_	N	N	N	N	N	N	N
287	TEST-INIT	24-hour test		N	N	_	N	N	N	N	N	N	N
288	FEOL-WETS	OZONE HUANG CLEAN		N	N	_	N	N	_	N	N	N	N
289	FEOL-WETS	rinse and dry		N	N	_	N	N	_	N	N	N	N
290	HOT	THIN OXIDE		N	N	_	N	N	_	N	N	N	N
291	FEOL-WETS	OZONE MOD HUANG CLEAN (X SEC DHF)		N	N	_	N	N	_	N	N	N	N
292	FEOL-WETS	rinse and dry		N	N	_	N	N	_	N	N	N	N
293	HOT	GSC - FURNACE OXIDE		N	N	_	N	N	_	N	N	N	N
294	FEOL-WETS	OZONE MOD HUANG CLEAN (X SEC DHF)		N	N	_	N	N	_	N	N	N	N
295	FEOL-WETS	SPIN,RINSE AND DRY		N	N	_	N	N	_	N	N	N	N
296	RTP	Ch C GATE OXIDE - DRY		N	N	_	N	N	_	N	N	N	N
297	RTP	MEASURE FILM THICKNESS/UNIFORMITY		N	N	_	N	N	_	N	N	N	N
298	RTCVD	Exploratory process development		N	N	_	N	N	_	N	N	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
299	RTCVD	MEASURE FILM THICKNESS/UNIFORMITY		N	N	_	N	N	_	N	N	N	N
300	TEST-INIT	4-hr test		N	N	_	N	N	_	N	N	N	N
301	RTP	541C RTA		N	N	_	N	N	_	N	N	N	N
302	FEOL-WETS	OZONE HUANG CLEAN		N	N	_	N	N	_	N	N	N	N
303	FEOL-WETS	SPIN,RINSE AND DRY		N	N	_	N	N	_	N	N	N	N
304	LITH	193 TRANSFER WAFERS TO SCANNER		N	N	_	N	N	_	N	N	N	N
305	LITH	193 5Gate SG - Integrated		N	N	_	N	N	_	N	N	N	N
306	METROLOGY	TRANSFER WAFERS TO 42187		N	N	_	N	N	_	N	N	N	N
307	TEST-INIT	Initiator Coordination		N	N	_	N	N	_	N	N	N	N
308	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)		_	_	N	_	_	N	N	N	N	N
309	FEOL-WETS	SPIN,RINSE AND DRY		_	_	N	_	_	N	N	N	N	N
310	TEST-INIT	1.5-hr test		_	_	N	_	_	N	N	_	N	N
311	RTCVD	EPI COORDINATION		_	_	N	_	_	N	N	N	N	N
312	TEST-INIT	24-hour test		N	N	N	N	N	N	N	N	N	N
313	RTCVD	EPI COORDINATION		_	_	N	_	_	N	N	N	N	N
314	FEOL-WETS	OZONE MOD HUANG CLEAN (X SEC DHF)		_	_	N	_	_	N	N	N	N	N
315	RTCVD	Exploratory process development	Poly plug deposition	_	_	N	_	_	N	N	N	N	N
316	TEST-INIT	1.5-hr test	CMP to clear excess poly and more polish into STI	_	_	N	_	_	N	N	N	N	N
317	POLISH	Pre STI CMP-Wafer Transport to CMP lab		_	_	N	_	_	N	N	_	_	_
318	POLISH	CMP...PLEASE READ FIRST		_	_	N	_	_	N	N	N	N	N
319	POLISH	** CMP UV1280 Film Measurement & Recipe Creation		_	_	N	_	_	N	N	N	N	N
320	POLISH	Polish 1 - Poly-Si		_	_	N	_	_	N	N	N	N	N
321	POLISH	LEICA Optical Inspection (Westech)		_	_	N	_	_	N	N	N	N	N
322	POLISH	Pre STI CMP-Wafer Transport to CMP lab		_	_	N	_	_	N	N	_	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
		** CMP ONLY ** - UV1280 Thickness		N	_	N	N	_	N	N	_	N	N
323	POLISH	Measurement											
324	POLISH	STI CMP Atlas/Raptor Baseline-Send Ahead Polish		N	_	N	N	_	N	N	_	N	N
325	POLISH	LEICA Optical Inspection (Ebara)		N	_	N	N	_	N	N	_	N	N
326	POLISH	** CMP ONLY ** - UV1280 Thickness Measurement		N	_	N	N	_	N	N	_	N	N
327	POLISH	** CMP ONLY ** - UV1280 Thickness Measurement		_	N	N	_	N	N	N	N	N	N
328	POLISH	STI CMP Atlas/Raptor Baseline-Send Ahead Polish		_	N	N	_	N	N	N	N	N	N
329	POLISH	LEICA Optical Inspection (Ebara)		_	N	N	_	N	N	N	N	N	N
330	POLISH	** CMP ONLY ** - UV1280 Thickness Measurement		_	N	N	_	N	N	N	N	N	N
331	POLISH	CMP...PLEASE READ FIRST		N	_	N	N	_	N	N	_	N	N
332	POLISH	STI CMP : Generic		N	_	N	N	_	N	N	_	N	N
333	POLISH	** CMP ONLY ** - UV1280 Thickness Measurement		N	_	N	N	_	N	N	_	N	N
334	POLISH	Post STI CMP- Wafer Transport to 42187 Changeroom		_	_	N	_	_	N	N	_	N	N
335	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)		_	_	N	_	_	N	N	_	N	N
336	FEOL-WETS	SPIN,RINSE AND DRY		_	_	N	_	_	N	N	_	N	N
337	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		_	_	N	_	_	N	N	_	N	N
338	FEOL-WETS	SPIN,RINSE AND DRY		_	_	N	_	_	N	N	_	N	N
339	TEST-INIT	4-hr test		N	N	N	N	N	N	N	N	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
340	CONTROL	Pull wafers	Bringing 2 wafers from another lot.	N	N	N	N	N	N	N	N	_	_
341	CONTROL	Wafer Remap		_	_	N	_	_	N	N	_	_	_
342	HOT	GSC - GATE Centura CH C	Gate coordination	_	_	N	_	_	N	N	_	_	_
343	FEOL-WETS	OZONE MOD HUANG CLEAN (X SEC DHF)	gate pre-clean	_	_	N	_	_	N	N	_	_	_
344	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_
345	RTP	Ch C RTNH3 + reox, recipe RTNH3700O2835, 30s ea(ta	2.7 nm oxynitride	_	_	N	_	_	N	N	_	_	_
346	RTP	MEASURE FILM THICKNESS/UNIFORMITY		N	N	N	N	N	N	N	N	N	N
347	LPCVD	POLY - 100 NM	Gate poly	_	_	N	_	_	N	N	_	_	_
348	LPCVD	MEASURE FILM THICKNESS/UNIFORMITY		N	N	N	N	N	N	N	N	N	N
349	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)		_	_	N	_	_	N	N	_	_	_
350	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_
351	I/I	Move from 42187 to I/I	Gate doping	_	_	N	_	_	N	N	_	_	_
352	I/I	I/I - AMT - P- 5-10KV-3.00E15-3.99e15-TA<10-R1		_	_	N	_	_	N	N	_	_	_
353	I/I	Move from I/I to 42187		_	_	N	_	_	N	N	_	_	_
354	TEST-INIT	8-hr test		_	_	N	_	_	N	N	_	_	_
355	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)		_	_	N	_	_	N	N	_	_	_
356	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_
357	LITH	DUV DUV HM8006-14	Tri-layer coating for lithography.	N	N	N	N	N	N	N	N	N	N
358	LITH	DUV Confirm film thickness-Nanospec		N	N	N	N	N	N	N	N	N	N
359	LITH	DUV DUV HM8006-14		_	_	N	_	_	N	N	_	_	_
360	DIEL	42006 Wafer transport to aisle 42006 from 42187		_	_	N	_	_	N	N	_	_	_
361	DIEL	42006 200C oxide H450C		N	N	N	N	N	N	N	N	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
362	DIEL	42006 thickness measurement on Rudolph		N	N	N	N	N	N	N	N	N	N
363	DIEL	42006 200C oxide H450C		_	_	N	_	_	N	N	_	_	_
364	DIEL	42006 Wafer transport to 42187 from 42006		_	_	N	_	_	N	N	_	_	_
365	LITH	193 TRANSFER WAFERS TO SCANNER		_	_	N	_	_	N	N	_	_	_
366	LITH	193 5Gate PC - Integrated		_	N	N	N	N	N	N	N	N	N
367	METROLOGY	Q7 OVERLAY MEASURE with Mean Plus 2-Sigma		_	N	N	N	N	N	N	N	N	N
368	METROLOGY	Verasem SAHD CD Meas single target		_	N	N	N	N	N	N	N	N	N
369	LITH	193 5Gate PC - Integrated		N	_	N	_	_	N	N	_	_	_
370	METROLOGY	Q7 OVERLAY MEASURE with Mean Plus 2-Sigma		N	_	N	_	_	N	N	_	_	_
371	METROLOGY	Verasem CD Meas 1 target		N	N	N	N	_	N	N	N	N	N
372	METROLOGY	TRANSFER WAFERS TO 42187		_	_	N	_	_	N	N	_	_	_
373	RIE	42218 Y56A PC Soft Mask - Nonstandard	Etching and cleaning.	_	_	N	_	_	N	N	_	_	_
374	RIE	42218 Y56C Axiom Experimental		_	_	N	_	_	N	N	_	_	_
375	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		_	_	N	_	_	N	N	_	_	_
376	FEOL-WETS	SPIN,RINSE AND DRY		_	_	N	_	_	N	N	_	_	_
377	RIE	42187 Y72WB Post-Si 4.16736111111111 HF Dip Poly Gate		_	_	N	_	_	N	N	_	_	_
378	RIE	42187 HF MIS BENCH SRD		_	_	N	_	_	N	N	_	_	_
379	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF,NO MEGS)		_	_	N	_	_	N	N	_	_	_
380	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_
381	HOT	GATE OXIDE - DRY - 3.5nm poly sidewall	Oxide spacer	_	_	N	_	_	N	N	_	_	_
382	HOT	MEASURE Tox		N	N	N	N	N	N	N	N	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
383	RTCVD	Ch A Nitride	Nitride spacer	_	_	N	_	_	N	N	_	_	_
384	RTCVD	MEASURE FILM THICKNESS/UNIFORMITY		N	N	N	N	N	N	N	N	N	N
385	RIE	42187 Y12A - SPACER 15 nm NITRIDE SPACER	spacer etch	_	_	N	_	_	N	N	_	_	_
386	LITH	DUV O2 plasma Gasonics		_	_	N	_	_	N	N	_	_	_
387	FEOL-WETS	4.16736111111111 DHF ETCH		_	_	N	_	_	N	N	_	_	_
388	FEOL-WETS	SPIN,RINSE AND DRY		_	_	N	_	_	N	N	_	_	_
389	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF,NO MEGS)		_	_	N	_	_	N	N	_	_	_
390	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_
391	TEST-INIT	Initiator Coordination		_	N	N	N	N	N	N	N	N	N
392	I/I	Move from 42187 to I/I	Source/Drain implantation	_	_	N	_	_	N	N	_	_	_
393	I/I	I/I - AMT - GE-10-20KV-3.00E14-5.00E14-TA<10-R1		_	_	N	_	_	N	N	_	_	_
394	I/I	I/I - AMT - AS-20-80KV-3.00E15-4.00E15-TA<10-R1		_	_	N	_	_	N	N	_	_	_
395	I/I	Move from I/I to 42187		_	_	N	_	_	N	N	_	_	_
396	RTP	Ch C RTA: uniform backside, no metals		_	_	N	_	_	N	N	_	_	_
397	LITH	DUV Front side protect	Back-side CMP	_	_	N	_	_	N	N	_	_	_
398	LITH	DUV Front side protect		_	_	N	_	_	N	N	_	_	_
399	POLISH	Pre CMP-Process Development-Transport to CMP lab		_	_	N	_	_	N	N	_	_	_
400	POLISH	Development - Used by pre-approval only		_	_	N	_	_	N	N	_	_	_
401	POLISH	ONTRAK Brush Clean for FEOL (Westech)		_	_	N	_	_	N	N	_	_	_
402	POLISH	LEICA Optical Inspection (Westech)		_	_	N	_	_	N	N	_	_	_
403	POLISH	Post CMP-Process Development-Transport to 42187		_	_	N	_	_	N	N	_	_	_

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
404	LITH	DUV O2 plasma Gasonics		_	_	N	_	_	N	N	_	_	_
405	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF,NO MEGS)		_	_	N	_	_	N	N	_	_	_
406	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_
407	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		_	_	N	_	_	N	N	_	_	_
408	FEOL-WETS	SPIN,RINSE AND DRY		_	_	N	_	_	N	N	_	_	_
409	BEOL-WETS	HF/EG at 80C		_	_	N	_	_	N	N	_	_	_
410	BEOL-WETS	spin, rinse, dry		_	_	N	_	_	N	N	_	_	_
411	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF,NO MEGS)		_	_	N	_	_	N	N	_	_	_
412	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_
413	METAL	42006 NiPt Coordination		_	_	N	_	_	N	N	_	_	_
414	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF,NO MEGS)		_	_	N	_	_	N	N	_	_	_
415	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_
416	METAL	42006 wafer transport to 42006		_	_	N	_	_	N	N	_	_	_
417	METAL	42006 4.16736111111111 DHF non-metal		_	_	N	_	_	N	N	_	_	_
418	METAL	42006 post-etch SRD		_	_	N	_	_	N	N	_	_	_
419	METAL	42006 Ni plus TiN deposition	Silicide metal dep.	_	_	N	_	_	N	N	_	_	_
420	METAL	42006 wafer transport to 42187 in gating		_	_	N	_	_	N	N	_	_	_
421	RTP	RTA metals other than Co & Ti silicides	Silicide anneal	_	_	N	_	_	N	N	_	_	_
422	RTP	DILUTE AQUA REGIA (ETCH Ni/Pt ALLOYS)	remove excess metal	_	_	N	_	_	N	N	_	_	_
423	RTP	SPIN,RINSE AND DRY		_	_	N	_	_	N	N	_	_	_
424	FEOL-WETS	HUANG B ONLY CLEAN (NO MEGS)		_	_	N	_	_	N	N	_	_	_
425	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
426	HOT	Metal ANNEAL O2 free B3 only	further anneal	_	_	N	_	_	N	N	_	_	_
427	FILMS	42006 480C Low Stress Nitride H450A	etch stop nitride dep.	N	N	N	N	N	N	N	N	N	N
428	FILMS	42006 thickness measurement		N	N	N	N	N	N	N	N	N	N
429	FILMS	42006 480C Low Stress Nitride H450A		_	_	N	_	_	N	N	_	_	_
430	FILMS	42006 IMD HDP OXIDE H449A ~400C	Inter-level dielectric deposition	N	N	N	N	N	N	N	N	N	N
431	FILMS	42006 thickness measurement		N	N	N	N	N	N	N	N	N	N
432	FILMS	42006 IMD HDP OXIDE H449A ~400C		_	_	N	_	_	N	N	_	_	_
433	FILMS	42006 wafer transport from 42006 to 42187 in gating	ILD CMP	_	_	N	_	_	N	N	_	_	_
434	POLISH	Pre CA oxide CMP- Transport to CMP lab		_	_	N	_	_	N	N	_	_	_
435	POLISH	UV1280 Thickness Measurements		_	_	N	_	_	N	N	_	_	_
436	POLISH	RAPTOR/ATLAS CA oxide-Send ahead polish		_	N	N	N	N	N	N	N	N	N
437	POLISH	** CMP ONLY ** - UV1280 Thickness Measurement		_	N	N	N	N	N	N	N	N	N
438	POLISH	RAPTOR/ATLAS CA oxide cmp		N	_	N	_	_	N	N	_	_	_
439	POLISH	** CMP ONLY ** - UV1280 Thickness Measurement		N	_	N	_	_	N	N	_	_	_
440	POLISH	Post CA oxide CMP- Transport to 42187 Changeroom		_	_	N	_	_	N	N	_	_	_
441	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)	Cleaning before litho	_	_	N	_	_	N	N	_	_	_
442	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_
443	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		_	_	N	_	_	N	N	_	_	_
444	FEOL-WETS	SPIN,RINSE AND DRY		_	_	N	_	_	N	N	_	_	_
445	LITH	193 TRANSFER WAFERS TO SCANNER		_	_	N	_	_	N	N	_	_	_
446	LITH	193 5Gate CA - Integrated		_	N	N	N	N	N	N	N	N	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	8	9	10
447	METROLOGY	Q7 OVERLAY MEASURE with Mean Plus 2-Sigma		_	N	N	N	N	N	N	N	N	N
448	METROLOGY	Verasem SAHD CD Meas single target		_	N	N	N	N	N	N	N	N	N
449	LITH	193 5Gate CA - Integrated	Via definition	N	_	N	_	_	N	N	_	_	_
450	METROLOGY	Q7 OVERLAY MEASURE with Mean Plus 2-Sigma		N	_	N	_	_	N	N	_	_	_
451	LITH	193 TRANSFER WAFERS TO 42187 Lab		_	_	N	_	_	N	N	_	_	_
452	METROLOGY	Verasem CD Meas 1 target		N	_	N	_	N	N	N	N	_	N
453	RIE	42218 Y56D Enabler Experimental	Via etch	_	_	N	_	_	N	N	_	_	_
454	LITH	DUV O2 plasma Gasonics		_	_	N	_	_	N	N	_	_	_
455	FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics		_	_	N	_	_	N	N	_	_	_
456	FEOL-WETS	SPIN,RINSE AND DRY		_	_	N	_	_	N	N	_	_	_
457	FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF,NO MEGS)		_	_	N	_	_	N	N	_	_	_
458	FEOL-WETS	rinse and dry		_	_	N	_	_	N	N	_	_	_
459	METAL	42006 wafer transport to 42006	Metal liner deposition	_	_	N	_	_	N	N	_	_	_
460	METAL	42006 MOL liner		N	N	N	N	N	N	N	N	N	N
461	METAL	42006 Baseline Rs check on CA liner		N	N	N	N	N	N	N	N	N	N
462	METAL	42006 MOL liner		_	_	N	_	_	N	N	_	_	_
463	METAL	42006 wafer transport to 42187 in gating	Tungsten deposition	_	_	N	_	_	N	N	_	_	_
464	METAL	42187 Sequence: W_395C_Si5_04K		N	N	N	N	N	N	N	N	N	N
465	METAL	42187 Baseline CA W Rs measurement		N	N	N	N	N	N	N	N	N	N
466	METAL	42187 Sequence: W_395C_Si5_04K	Via CMP	_	_	N	_	_	N	N	_	_	_
467	POLISH	Pre MOL W CMP- Transport to CMP lab		_	_	N	_	_	N	N	_	_	_
468	POLISH	W CMP		_	_	N	_	_	N	N	_	_	_

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
469	POLISH	CMP ONLY//ONTRAK Brush Clean for MOL		_	_	N	_	_	N	N	_	_	_
470	POLISH	LEICA Optical Inspection (Westech)		_	_	N	_	_	N	N	_	_	_
471	POLISH	W Liner CMP		_	_	N	_	_	N	N	_	_	_
472	POLISH	CMP ONLY//ONTRAK Brush Clean for MOL		_	_	N	_	_	N	N	_	_	_
473	POLISH	LEICA Optical Inspection (Westech)	Via touchup etch	_	_	N	_	_	N	N	_	_	_
474	BEOL-WETS	4.16736111111111 DHF HiK		_	_	N	_	_	N	N	_	_	_
475	BEOL-WETS	spin, rinse, dry		_	_	N	_	_	N	N	_	_	_
476	BEOL-WETS	Ammonium Hydroxide etches		_	_	N	_	_	N	N	_	_	_
477	BEOL-WETS	spin, rinse, dry		_	_	N	_	_	N	N	_	_	_
478	RIE	42126 Y14PM1 9400 W Touchup - Baseline		_	_	N	_	_	N	N	_	_	_
479	BEOL-WETS	4.16736111111111 DHF HiK		_	_	N	_	_	N	N	_	_	_
480	BEOL-WETS	spin, rinse, dry		_	_	N	_	_	N	N	_	_	_
481	BEOL-WETS	Ammonium Hydroxide etches		_	_	N	_	_	N	N	_	_	_
482	BEOL-WETS	spin, rinse, dry		_	_	N	_	_	N	N	_	_	_
483	DIEL	42187 Hex543A SiO2 xxxA	ILD for Metal	N	N	N	N	N	N	N	N	N	N
484	DIEL	42187 monitor thickness measurement		N	N	N	N	N	N	N	N	N	N
485	DIEL	42187 Hex543A SiO2 xxxA		_	_	N	_	_	N	N	_	_	_
486	LITH	193 TRANSFER WAFERS TO SCANNER		_	_	N	_	_	N	N	_	_	_
487	LITH	193 5Gate M1 - Integrated		_	N	N	N	N	N	N	N	N	N
488	METROLOGY	Q7 OVERLAY MEASURE with Mean Plus 2-Sigma		_	N	N	N	N	N	N	N	N	N
489	METROLOGY	Verasem SAHD CD Meas single target		_	N	N	N	N	N	N	N	N	N
490	LITH	193 5Gate M1 - Integrated		_	_	N	_	_	N	N	_	_	_
491	METROLOGY	Q7 OVERLAY MEASURE with Mean Plus 2-Sigma		N	_	N	N	N	N	N	N	_	N

Step #	Sector	Process	Notes	1	2	3	4	5	6	7	**8**	9	10
492	METROLOGY	Verasem CD Meas 1 target		N	_	N	N	N	N	N	N	_	N
493	LITH	193 TRANSFER WAFERS TO 42187 Lab		_	_	N	_	_	N	N	_	_	_
494	RIE	42126 Y14PM2 - 4520XL Mx Oxide - Nonstandard	Metal trench open	_	_	N	_	_	N	N	_	_	_
495	BEOL-WETS	DI water rinse		_	_	N	_	_	N	N	_	_	_
496	BEOL-WETS	20.8340277777778 DHF		_	_	N	_	_	N	N	_	_	_
497	BEOL-WETS	DI water rinse		_	_	N	_	_	N	N	_	_	_
498	BEOL-WETS	spin, rinse, dry		_	_	N	_	_	N	N	_	_	_
499	TEST-INIT	Initiator Coordination	Inspect if vias are exposed.	_	_	N	_	_	N	N	_	_	_
500	METROLOGY	JEOL SEM Inspection		_	N	N	N	N	N	N	N	N	N
501	METAL	42187 11S baseline M1 liner-seed		_	_	N	_	_	N	N	_	_	_
502	PLATING	pre transport from 42187 to 01-022		_	_	N	_	_	N	N	_	_	_
503	PLATING	Copper Plate 0.76um	electroplating of Cu	_	N	N	N	N	N	N	N	N	N
504	PLATING	film thickness Measurement		_	N	N	N	N	N	N	N	N	N
505	PLATING	Copper Plate 0.76um		N	_	N	_	_	N	N	_	_	_
506	PLATING	Optically inspect plated wafer.		_	_	N	_	_	N	N	_	_	_
507	PLATING	4 Point probe measurement analysis.		_	_	N	_	_	N	N	_	_	_
508	PLATING	post transport from 01-022 to 42187		_	_	N	_	_	N	N	_	_	_
509	PLATING	YKT MRL Cu Anneal		_	_	N	_	_	N	N	_	_	_
510	POLISH	Pre Copper CMP-Wafer Transport to CMP lab		_	_	N	_	_	N	N	_	_	_
511	POLISH	Development CMP for Copper polish		_	_	N	_	_	N	N	_	_	_
512	POLISH	LEICA Optical Inspection (Westech)		_	_	N	_	_	N	N	_	_	_
513	POLISH	Post Copper CMP- Transport to 42187 Changeroom		_	_	N	_	_	N	N	_	_	_

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