

12-30-2014

Modeling, Fabrication, and Characterization of Memristors

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Modeling, Fabrication, and Characterization of Memristors

Anas Mazady, Ph.D.
University of Connecticut, 2014

The term “memristor” was coined by L. Chua from its two distinct functional characteristics, memory and resistor. From the symmetry argument of the circuit element and circuit variable matrix, memristor is deemed as the fourth fundamental circuit element, after resistor, capacitor, and inductor. Memristor switching and observed I-V characteristics are explained utilizing the underlying physics of the device in terms of the formation and rupture of filaments. Three different conduction mechanisms, namely - filament assisted tunneling current, bulk tunneling current and currents flowing through low and high conductivity filaments give rise to the total current in memristive systems. DC and RF performance of memristor circuits, including transient behavior, is developed by taking into account these current contributions arising from different conduction mechanisms. The DC circuit model explains the observed I-V hysteresis and most importantly allows scaling and optimization. RF analysis suggests for a maximum allowable frequency of 7.5 GHz beyond which TiO_2 memristors can no longer be used as RRAMs. Transient performance of memristors employing different material systems is investigated and experimentally verified using ZnO nanowire memristors. ZrO_x memristors showed the shortest switching delay owing to its high mobility of $370 \text{ cm}^2/\text{V-s}$. Upon scaling devices down to 50 nm, the delay decreases by 3-4 orders of magnitude. Bipolar resistive switching with $R_{\text{OFF}}/R_{\text{ON}}$ ratio of 684 and rise and fall times shorter than $7\mu\text{s}$ and $10\mu\text{s}$, respectively, is demonstrated for $2 \mu\text{m}$ ZnO nanowire memristors. Use of nanowire instead of thin films allows high packing density and as a result high bit

density. Experimental demonstration of a 1-bit memristor PUF is reported for the first time implementing ZnO memristors showing 50% uncertainty and high reliability of the response bit for a given challenge. The physics based circuit model of memristors was also implemented to accurately determine the simulation time required for randomly selected polyominoes from a 3D array of memristors. The proposed model provides higher degree of complexity and results in 7 orders of increase in simulation time for an attacker than the previous best report. Operation of a material IMP logic has been demonstrated using only two ZnO memristors that is functional for 5 μ s logic pulses. Designing logics using memristors allows the use of the same physical unit as multiple functional units, such as – memory, logic, and interconnect. This approach has the potential to redefine the traditional computer architecture to advanced architectures overcoming the “von Neumann bottleneck” of throughput. Chaotic circuit was constructed using only 2 elements, a memristor and a series resistor, which is the most compact form of chaotic circuits ever reported, and demonstrated perfect chaos in its phase-space trajectory with the highest Lyapunov exponent being 61.57s⁻¹.

Modeling, Fabrication, and Characterization of Memristors

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A Dissertation

Submitted in Partial Fulfillment of the

Requirements for the Degree of

Doctor of Philosophy

at the

University of Connecticut

2014

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APPROVAL PAGE

Doctor of Philosophy Dissertation

Modeling, Fabrication, and Characterization of Memristors

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2014

“If we knew what it was we were doing, it would not be called research, would it?”

—Albert Einstein

Dedicated to my elder sister, *Mima*.

We started school together, soon to find out she was an intellectually challenged child. However, she never ceased to make us happy with her innocent smiles, sometimes for no apparent reason.

ACKNOWLEDGMENTS

I would like to take this opportunity to express my gratitude to those people without whom this work would not be possible. At first, I would like to thank my academic supervisor Dr. Mehdi Anwar for his active guidance and support. I am grateful to Abdiel Rivera, Pik-Yiu Chan, and David Kriz for their help in various device fabrication steps. Thanks to Dr. Domenic Forte and Touhidur Rahman for their constructive suggestions writing the memristor based physical unclonable function manuscript.

I am indebted to my loving wife Farzana Sharmin and my father in law Ansarul Haque for being so supportive and taking care of me during the course of my Ph.D. career. Credit goes to my parents, Majedur Rahman and Roushon Majed, for instilling the confidence in me that continued to illuminate the path of my success.

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Chapter 1 : Introduction

1.1 Motivation

The concept of memristor was first proposed in the early 70's by Chua [1] based upon symmetry arguments requiring a relationship to exist between the magnetic flux and electric charge similar to the relationship between voltage and current that defines resistance. A renewed interest in memristors has emerged since Strukov *et al.* [2] reported hysteresis in the I-V characteristic, typical of memristors, of a Pt/TiO₂/Pt two terminal device in the absence of any applied magnetic field. The non-requirement of a magnetic field allows possible implementations of memristors in resistance-switching random access memory (RRAM) [3] as well as a host of other application platforms. Memristors were demonstrated to be used as non-volatile memory due to their ability to retain the states in the absence of any applied bias.

To keep pace with the growing demand for miniaturization, conventional memory technologies, such as DRAM, SRAM, and NAND flash, are fast approaching their fundamental limitation. It is critically important to have a feature size larger than 16 nm for those devices as they must have 16 electrons for a single level cell operation (1 bit/cell). In contrast, being able to be scaled down to 8 nm technology nodes while maintaining its distinct features, memristor has been identified as one of the most promising candidates for future generation memory technology in the 2010 International Technology Roadmap for Semiconductor (ITRS) workgroups meeting [4]. Having 3D stacking capabilities in crossbar arrays [5], low power consumption [6], and low cost per

bit [4], memristors outweigh the existing technologies. Memristors were also reported to perform as logic gates [7, 8]. Borghetti *et al.* [8] performed a fundamental Boolean logic operation pIMPq (p implies q) and showed that memristors can function both as logic (gates) and memory (latches). Use of memristors was also demonstrated in programmable analog circuits [9, 10]. Pershin *et al.* [10] demonstrated analog circuits, such as – threshold comparators, programmable gain amplifiers, and digital potentiometers employing memristors. The dynamical behavior of memristors has also prompted researchers to investigate the possibilities of designing electronic synapses and cellular neural networks (CNN) using memristors [11, 12]. Having a compact cell structure TiO_2 thin film memristors can model a synapse as small as $50 \times 50 \times 50 \text{ nm}^3$ [11]. Memristors can be implemented to realize chaotic circuits that can modulate the signal using perfect chaos theory, thus making it immune to interception [13]. A communication system based on this technique finds its applications in military, defense, and other areas where higher level of encryption is required. These circuits can also be used to study different non-linear circuit properties such as period doubling bifurcations, period adding sequences, quasi-periodicity and intermittent transitions which is observed in a number of physical circuits and systems [14].

1.2 Background and Recent Developments

Memristors or memristive systems are deemed as one of the promising candidates for future generation memory technologies due to their scalability, non-volatility, lower power consumption, lower cost per bit, and 3D stacking capability etc. [4]. Recent progresses in memristor research have also demonstrated their potential use in

neuromorphic computing [15], programmable logic [8], and analyzing non-linear circuits [14] among other applications.

In recent years, in-depth scrutiny of memristor operation, utilizing different technological tools (AFM, STM, TEM, XRD etc.) has provided a better understanding of the underlying physics as reported by Mazady *et al.* [16]. However, dynamical analysis of memristors that can explain carrier dynamics and associated transients in memristor is largely absent in the literature due to the difficulty in obtaining an exact closed form solution of the coupled electronic-ionic conduction model. The dynamics of memristive systems have mainly been studied by means of either numerical simulations [17] or empirical equations [18]. Using a linear ionic drift model Georgiou *et al.* [19] identified the governing differential equations to fall in the category of Bernoulli Differential Equation (BDE). Cai *et al.* [20] analyzed TiO₂ memristor with an arbitrary order of window function that conforms to the Abel Differential Equations (ADE) and reported a closed form solution. However, these formulations were based upon the mathematical model of oxygen vacancy movement as a front, proposed by Strukov *et al.* [2] and are valid only for the particular class of memristors that satisfied BDE and ADE. In contrast, development of dynamical model in this thesis follows the inherent physics of these devices as outlined by Mazady *et al.* [16].

1.3 Challenges for Memristor Technology

Among the emerging technology solutions for next generation memory architectures, memristor is preferred over Phase Change Random Accesses Memory (PCRAM) due to

faster operation and non-requirement for an additional TiN based heating element. Compared to magnetic memories, such as MRAM and STT-RAM, memristors promise smaller and simpler cell structure. Unlike the MOS-accessed memory cells, memristor not requiring an access device can be fabricated using crossbars resulting in high packing density [21]. Nevertheless, several challenges associated with applicability of memristor are hindering its mass production and can be classified into two broad categories: fundamental limitations and practical challenges. Endurance of memristor based RRAMs is directly affected by electromigration of electrode materials (such as Ag and Au) as has been observed by other researchers, and is a fundamental limitation of oxygen vacancy migration based physics of the device. Endurance values, the number of cycles the memristor can be reversibly switched, in the range 10 to 10^6 is most common with the highest ever reported value of 10^{10} cycles by HP Labs for Pt/TaO_x/Ta memristors where the Ta top electrode serves as an oxygen vacancy reservoir [22]. Search for suitable materials for contact electrodes that do not undergo oxidation followed by migration and is yet inexpensive in contrast to the Pt electrode based memristors, is an ongoing research. One approach to address this issue is to articulate a WRITE operation protocol such that the memristor is refreshed after a number of READ/WRITE cycles using a negative pulse of comparatively higher amplitude. There are various practical challenges for memristor applications as well, such as integration of memristors in cross-bar architecture. During WRITE operations, when a memristor is selected from an array of memristors, memristors that share the same top or bottom electrode get *half selected* thereby creating sneak paths that increase the leakage current. The number of memristive elements that can be incorporated in the crossbar is limited by the write driver current

capability. The requirement on the driver current can be calculated for the worst case scenario when all the memristors are in LRS, as:

$$I_{driver} = I_{reset} + (N - 1) \times I\left(\frac{V_{reset}}{2}\right)$$

where, V_{reset} and I_{reset} are the reset voltage and current, respectively, and N is the number of elements connected to the selected bus. Practical routes to address sneak path issue is to (i) introduce access devices, that require larger chip area marring the benefits of device scaling, or (ii) utilize materials that have significant nonlinearity in their ON characteristics [23], or (iii) develop a two-step WRITE protocol that would cost additional power consumptions.

1.4 Dissertation Organization

The dissertation has been organized in the following manner. The underlying physics, electrochemistry, and the associated conduction processes are detailed in Chapter 2. Circuit models to simulate DC, transient, and RF characteristics of memristors are developed in Chapter 3 based on the physics of the device. Fabrication and characterization of ZnO nanowire based memristors are discussed in chapter 4 and the design of experiment for switching transient measurements are also shown. The first experimental demonstration of memristor nano-PUF is shown in Chapter 5 while fabrication of digital logics using memristors is demonstrated in Chapter 6. Chaotic circuit using only 2-elements, memristor and a series resistor, is demonstrated in Chapter 7.

Chapter 2 : The Underlying Physics and Conduction Mechanism of Memristors

2.1 Introduction

The optimization of memristors to address different applications demands identification and correct interpretation of underlying physical mechanisms, and for that researchers have adopted both mathematics and physics based analyses. Strukov *et al.* [2] had provided a qualitative explanation of the observed hysteresis by introducing a window function that was later improved by others [5-7]. However, such an approach avoids the physics of operation, which is more involved as indicated by other researchers. Kwon *et al.* [24] reported the presence of conducting Magneli phase Ti_4O_7 filaments in Pt/ TiO_2 /Pt memristors in case of unipolar resistance switching (URS) by using conductive AFM and correlated the current through these two terminal devices with the conduction through filaments. Based on High Resolution TEM (HRTEM) images the diameters of the filaments were estimated to be around 15 nm at the cathode and tapering to 3 nm at the anode. Kim *et al.* [5] proposed a qualitative model to explain bipolar resistance switching (BRS) using electron trapping/detrapping mechanisms in the ruptured region of URS filaments and correlated it with a varying compliance current during electroformation. Jo *et al.* [25], while discussing Si-based memristors with Ag-top electrode, provided a qualitative explanation of the observed I-V characteristics in terms of filament assisted tunneling. Memory action in Ta_2O_5 and Nb_2O_5 was attributed to metallic filaments in the early 70's [26]. This filamentary nature is also supported by

Beaulieu [27], Choi [28], Rossel [29], Ogimoto [30] while investigating VO_2 , TiO_2 , $\text{SrZrO}_3\text{:Cr}$, SrTiO_3 , respectively, where the ON resistance was found uncorrelated with the cross sectional area of the contact pads. Electrocoloration [31] and C-AFM images verify filament formation in SrTiO_3 while infrared thermal studies indicate the presence of filaments in $\text{SrZrO}_3\text{:Cr}$.

Demonstration of memristive action using organic compounds often makes use of Al as the top electrode which easily gets oxidized facilitating switching [32]. Kevorkian *et al.* [33] identified electromigration of soft metal electrodes as the mechanism for filament formation. Cölle *et al.* [34] reported infrared photographs to establish the existence of filaments and the growth and rupture dynamics in MIM structures. Karthaus *et al.* [32] report that increasing pad size by a factor of 18 from 0.013 mm^2 to 0.233 mm^2 decreases the ON resistance only by a factor of 2.2, from 420Ω to 190Ω , thereby, demonstrating the absence of any correlation between overall device resistance and cross-sectional area of contact pads while favoring an explanation in terms of filaments. The multitude of experimental data suggests the presence of filaments responsible for the observed switching behavior in memristors. However, a conclusive understanding based upon the underlying physical and chemical processes, that explain both qualitatively and quantitatively the observed memristor behavior, is yet to be reported.

2.2 Physics of Operation

2.2.1 Metal/Insulator/Metal Memristor

Yang *et al.* [35] reported I-V characteristics of a $\text{Pt/TiO}_2\text{/Pt}$ memristor, with cross-

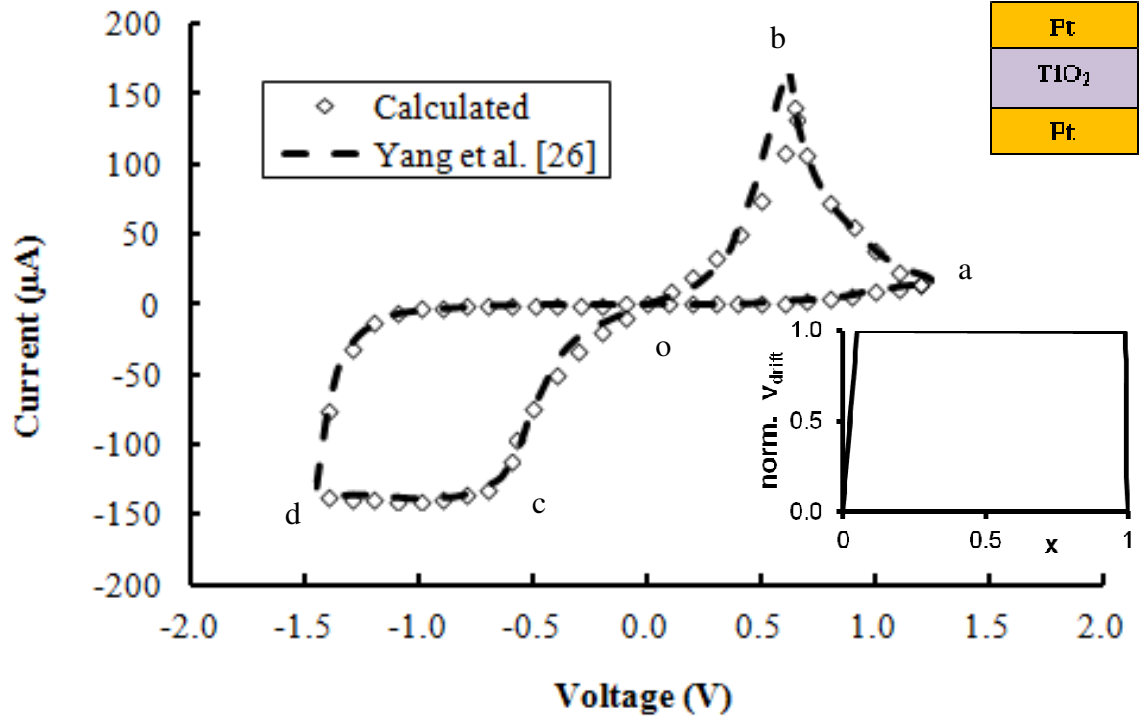


Figure 2.1. Calculated and measured I-V characteristics of a Pt/TiO₂/Pt structure. Inset: normalized drift velocity of the carriers with respect to position and the device structure.

sectional area of 50nm×50nm and TiO₂ layer thickness of 50 nm. Fig. 2.1 compares the theoretical I-V characteristics obtained using the present model with the reported experimental data showing good agreement. With the applied voltage, V_{APPL} , increasing from zero in the positive direction along oa (see Fig. 2.1), three different conduction processes, namely, (a) bulk tunneling (I_{TUN}), (b) filament assisted tunneling (I_{FA}), and (c) ohmic conduction through low conductivity filaments (I_{LC}) become active as depicted in Fig. 2.2 (a).

I_{TUN} represents the typical bulk tunneling current between the anode and cathode of the memristor. Calculation of I_{TUN} follows the treatment suggested by Simmons [36, 37] for the determination of tunneling current in MIMs with similar metal electrodes.

$$I_{TUN} = J_0 A \left[\left(\phi_0 - \frac{V_{APPL}}{2} \right) \exp \left(-C \sqrt{\phi_0 - \frac{V_{APPL}}{2}} \right) - \left(\phi_0 + \frac{V_{APPL}}{2} \right) \exp \left(-C \sqrt{\phi_0 + \frac{V_{APPL}}{2}} \right) \right] \dots (1)$$

where, $J_0 \equiv \frac{q^2}{2\pi\hbar d_{eff}^2}$, A is the cross sectional area and $C \equiv \frac{4\pi d_{eff} \sqrt{2m_e^* q}}{\hbar}$, with d_{eff} being

the bias dependent tunnel width that equals the oxide layer thickness d ($= 50$ nm) at zero bias. q and \hbar are the elementary electron charge and Plank's constant, respectively.

Barrier height at zero bias (ϕ_0) and effective mass of electrons (m_e^*) in TiO_2 are assumed to be 1.37 V and $3m_0$ respectively, where m_0 is the free electron mass [38].

I_{FA} represents the filament assisted tunneling component of the total current, flowing from the tip of the growing filament to the opposite contact and depends upon the redox chemistry at the contacts as discussed in the following. With the application of a positive

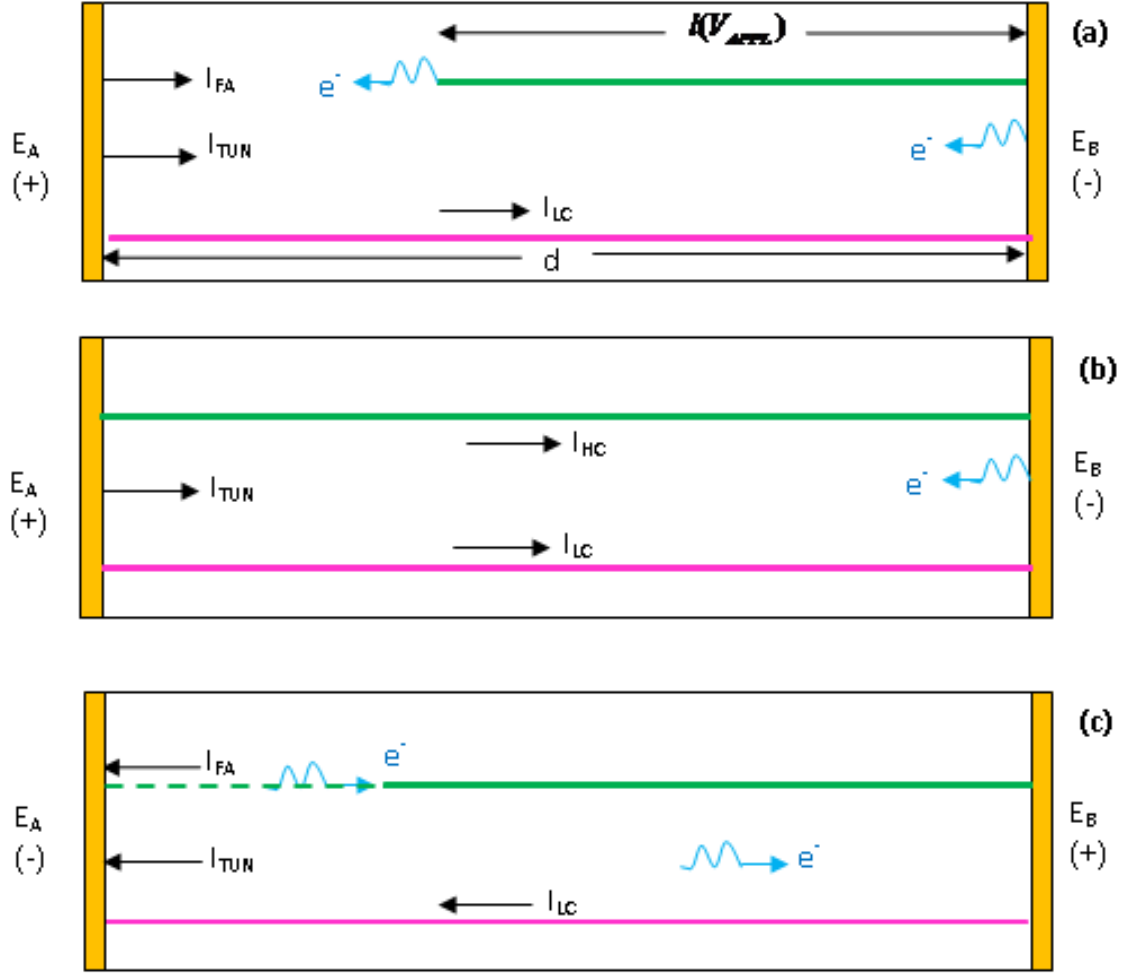


Figure 2.2. The different current components active during memristor operation (a) under a positive bias voltage (curve *oa* of Fig. 2.1), (b) during ON state (curve *boc* of Fig. 2.1), and (c) under negative applied bias (curve *cdo* of Fig. 2.1). I_{TUN} , I_{FA} , I_{LC} and I_{HC} represent the bulk tunneling current, filament assisted tunneling current, current through the low and high conductivity filaments, respectively.

bias voltage to electrode E_A (see Fig. 2.2a), a reduction of Ti^{+4} (TiO_2) into Ti^{+3} ($Ti_4O_5^{+2}$) takes place near that electrode: $8TiO_2 \rightarrow 2Ti_4O_5^{+2} + 3O_2 + 4e^-$. Experimentally observed phenomena, such as oxidation of anode and electrode deformation may be attributed to similar reduction chemistry [39]. The positively charged $Ti_4O_5^{+2}$ ions (oxygen vacancies) drift towards electrode E_B and react with O^{2-} ions: $Ti_4O_5^{+2} + O^{2-} \rightarrow 2Ti_2O_3$. Ti_2O_3 being a metastable phase of titanium oxide, accumulates at the cathode (electrode E_B) and starts to grow toward the anode (electrode E_A) forming high conductivity filaments. Depending on the cross sectional area, multiple filaments may grow simultaneously inside the device. In a voltage induced circuit, as soon as some filaments are formed, the voltage across the device would drop. The drop in electric field results in incomplete filaments inside the device which is confirmed through HRTEM images of a Pt/ TiO_2 /Pt memristor [24]. However, current contribution from these incomplete filaments (I_{FA}) is negligible compared to the current flowing through the completed filaments. It is to be noted that while TiO_2 is insulating, the loss of O_2 forms highly conductive Ti_2O_3 filament that allows current crowding facilitating the flow of filament assisted tunneling current. It is possible that instead of $Ti_4O_5^{+2}$ the loss of O_2 results in the formation of other non-stoichiometric compounds of Ti-O material system such as Ti_3O_5 , TiO_{2-x} or Magneli phase Ti_nO_{2n-1} [40]. The computation of filament assisted tunneling current requires an estimation of the number of filaments, their cross sectional areas and the bias dependence of the length of the filaments. The calculation of I_{FA} proceeds by replacing d_{eff} , in Eqn. (1), with $d - l(V_{APPL})$, where $l(V_{APPL})$ is the applied bias dependent length of the filament. The generic analytical expression to calculate the growth rates of the filaments are derived in Sec. III. The growth rates are dependent on parameters such as, device length,

applied bias, and traps/ impurities in the material. For this particular case of Ti_2O_3 filaments, growth rates are calculated in Sec. 2.3. The physics-based model presented here is accurate enough to quantitatively explain the dynamics of memristors with different material structures by taking the growth rates derived in Sec. 2.3 as the fitting parameters. Here for simplicity the filament growth rates are assumed to be linear, being 30 nm/V below 0.5 V and 0.2 nm/V above 0.5 V. The assumed growth rates allow fitting the experimental data while permitting a detailed analysis correlating the filament growth mechanism to the rate of redox processes in the presence of an applied electric field as discussed in Sec. 2.3. The total cross sectional area of the filaments, A_{FIL} , is estimated by assuming an inter-filament distance of 0.1 μm and an average filament diameter of 10 nm [24]. This results in the presence of one conducting filament with a cross-sectional area of 78.5 nm^2 for the 50nm \times 50nm device reported by Yang *et al.* [35].

The third component of current, I_{LC} , is due to the presence of low conductivity filaments (shown in pink in Fig. 2.2a), formed during electroformation and may be identified as Ti_3O_5 or a mix of Ti_3O_5 and Magneli phase materials. It has been reported that these materials are bound by monoclinic Ti_3O_5 on one side and by reduced rutile (TiO_{2-x}) on the other side [40]. Assuming a conductivity of 10^3 S/m for the low conductivity filaments, the resistance is calculated as $R_{LC} = 637$ k Ω [41]. The total current along *oa* (see Fig. 2.1) is dominated by current through the low conductivity filaments for applied voltages less than 0.6 V while the filament (high conductivity) assisted tunneling current dominates for voltages greater than 0.6 V which may be attributed to the reduction in tunneling distance with increasing applied bias. For an applied bias of 1.2 V the filament

assisted tunneling current is an order of magnitude higher than current flowing through the low conductivity filaments. The typical tunneling current I_{TUN} is not significant in this sample due to the large tunneling distance of 50 nm.

With the applied voltage still being positive but decreasing, the filaments continue to grow but at a different rate of 0.3 nm/V (see Fig. 2.1). Filament assisted tunneling current continues to dominate along ab being two orders of magnitude higher than current flowing through low conductivity filaments. Once the high conductivity filament is in contact with the counter electrode (see Fig. 2.2b), the total current along boc is dictated by (a) the current through the contacts modeled as two Schottky diodes connected back-to-back and (b) currents through the high and low conductivity filaments. This is similar to the recent finding that identifies Ti_nO_{2n-1} filaments bridging the two electrodes during the ON state [24]. Assuming a conductivity of 10^4 S/m the resistance of the high conductivity filaments R_{HC} is calculated as 63.7 k Ω . The incorporation of Schottky current along boc requires some clarification. Schottky barriers form if metal work function is higher than that of the n-type semiconductor. With the application of a positive bias voltage, oxygen vacancies are formed near the anode increasing the work function of the adjacent oxide layer making the Pt/titanium oxide junction ohmic. This ohmic resistance has been incorporated in the calculation of I_{LC} . With Ti_2O_3 filaments reaching the counter electrode the work function difference between the filament (~2.5 eV) and that of the Pt (~5.5 eV) electrode results in a Schottky contact contributing to the total current along boc . It is to be noted that in other regions (oa , ab , cd , do), the presence of oxygen vacancies makes the contact ohmic. The modeled diode has a saturation

current of 10 μA and emission coefficient of 10. Different metal contacts will shape this behavior differently and the Schottky phenomenon may not be evident in some material combinations, Al/Ti/LB/Pt structure [42] being an example. I_{LC} is two orders of magnitude lower than currents through the diode and high conductivity filament.

With the applied voltage becoming negative (E_A – negative and E_B – positive), current along oc is due to (a) conduction through the high conductivity filaments modified by the back-to-back Schottky contacts and (b) current through the low conductivity filaments which is two orders of magnitude smaller. However, beyond a certain negative voltage threshold (location c), the high conductivity filaments start to rupture initiating the flow of filament assisted tunneling current with increasing tunneling distance (Fig. 2.2c). The rate increase of the tunneling distance or the rate of filament rupture is assumed to be 0.05 nm/V. The low conductivity filaments, grown during electroformation, do not rupture during this phase as they were grown using high current compliance. This is in accordance with Rhode *et al.* [43] that stability of filaments is proportional to the power dissipated during the forming process. With the applied voltage becoming less negative and upon reaching -1.5 V, the current along do is still mostly due to filament assisted tunneling, I_{FA} , for $V_{APPL} < -1$ V but with a filament rupture rate of 0.4 nm/V. For $V_{APPL} > -1$ V, current through low conductivity filaments dominates the total current and as it approaches 0 V the filament assisted tunneling component becomes four orders of magnitude lower than I_{LC} . The inset in Fig. 2.1 shows the calculated normalized velocity profile of the ions as a function of position resembling the assumed window functions required for non-linear analysis [44]. The velocity is extracted by equating the current,

obtained using the present model, to qnv , where n and v are the ionic concentration and velocity, respectively. For simplicity, the computation is carried out by assuming a constant ion concentration of $1.2 \times 10^{21} \text{ cm}^{-3}$ [45]. An exact determination of the extracted ion velocity will require the position dependent calculation of ionic concentration. It is to be noted, that the inclusion of the window functions for non-linear analysis, artificially introduces carrier dynamics in the mathematical formulation.

2.2.2 Organic Memristor

Fig. 2.3 shows the two hysteresis loops in the I-V curves of Langmuir-Blodgett (LB) material sandwiched between Ti and Pt [42]. Al on top of Ti was used as the top electrode and Pt was used as the bottom electrode. I-V characteristic generated based upon the underlying physical processes as discussed previously shows good agreement with the experimental data.

The switching mechanism is explained by identifying two separate processes at the Al/Ti and Ti/LB interfaces (see Fig. 2.3 inset). At the Ti/LB interface, Ti gets oxidized to TiO_2 as metallic Ti exposed to LB through aqueous sub-phase for a prolonged period of time (>45 minutes) results in an oxide layer [42]. This oxidation process is facilitated by the presence of singlet oxygen in LB layer [46]. Ti also reacts with the LB monolayer of eicosanoic acid ($\text{C}_{19}\text{H}_{39}\text{COOH}$) and forms titanium-carbon complexes at the interface [42]. The titanium-carbon layer prevents further penetration of Ti into the LB layer suggesting that the oxide layer is formed inside the Ti layer. The second process

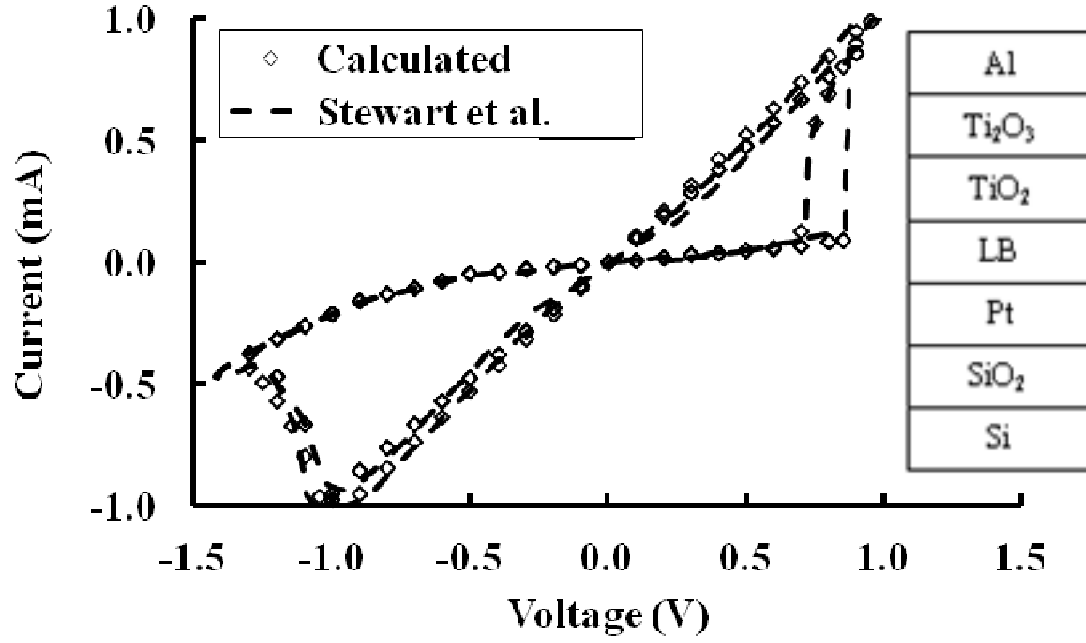


Figure 2.3. Calculated and measured hysteresis in the I-V curves of a Pt/LB/Ti/Al structure for two consecutive iterations. Inset: proposed material layers required to explain memristor action.

responsible for switching in Al/Ti/LB/Pt memristor takes place at the Al/Ti interface with the Al getting oxidized to Al_2O_3 . Cölle *et al.* [34] reported the formation of 2-4 nm of Al_2O_3 at the surface even when water and oxygen concentration is less than 1 ppm. Al_2O_3 interacts with Ti at the interface and gets reduced to metallic Al. In this process Ti is converted to Ti_2O_3 and TiO_2 as shown in the inset of Fig. 2.3 [47]. Upon application of a positive voltage to the Al electrode, a process similar to that discussed to explain Fig. 2.1, takes place, i.e. a reduction of $\text{Ti}^{+4}(\text{TiO}_2)$ to $\text{Ti}^{+3}(\text{Ti}_4\text{O}_5^{+2})$ and its conversion to Ti_2O_3 upon reaching the Pt electrode. It is to be noted that the Ti_2O_3 filaments formed inside LB remain intact and do not participate in switching. Though LB, as any other organic material, is not directly responsible for the observed switching it, however, creates the necessary precondition for the metal/organic/metal system to switch.

The organic layer also plays a major role in controlling $R_{\text{OFF}}/R_{\text{ON}}$ ratio by dictating R_{OFF} . Here, R_{ON} is the resistance during the ON state of the device which is a parallel combination of R_{LC} and R_{HC} , ignoring the effect of bulk conduction. R_{OFF} , on the other hand, is the resistance during the OFF state of the device which is a parallel combination of R_{LC} and R_{FA} , with R_{FA} being the resistance of the remnant ruptured filaments at $V_{\text{APPL}}=0$ V. During OFF state, a thicker LB layer produces enough singlet oxygen to convert Ti_2O_3 to TiO_2 in the Ti layer, thereby, increasing the OFF state resistance. Assuming TiO_2 layer thickness of 2.8 nm, a filament diameter of 7 nm and filament to filament distance of 0.12 μm , the 10 μm^2 cross sectional area of the device accommodates 693 filaments. Assuming conductivities of 200 S/m and 20 S/m, R_{HC} and R_{LC} are calculated to be 1.05 k Ω and 10.5 k Ω , respectively [40]. The observed I-V

characteristic in Fig. 2.3 is explained in a manner similar to that used to describe Fig. 2.1. With $+V_{APPL}$ increasing from 0 V, there are three components of currents (I_{TUN} , I_{FA} , I_{LC}) that add up to the total current flowing through the device with filament growth rate of 3 nm/V. As the applied voltage decreases the I-V characteristic remains ohmic until a negative threshold value of -1 V is reached subsequently rupturing the high conductivity filaments due to oxidation. The rupture rate is assumed to be 0.3 nm/V as the applied bias continues to become more negative until it reaches -1.5 V. Upon reaching -1.5 V, as the applied bias traverse towards zero, the barrier width keeps increasing at a rate of 2 nm/V. It is conjectured that sudden rise in current at large positive (negative) voltages is due to the filaments making (rupturing) contacts at the counter electrode – in that sense the number of such jumps will be correlated to the number of filaments present in the memristor.

The subsequent application of a positive voltage results in a second hysteresis loop validating the efficacy of the proposed physics based explanation of memristor behavior. The second I-V loop starts with some residual filaments and thus has a lower threshold voltage than that during the first I-V swing. The presence of the residual filaments is due to inability of the barrier to go back to the pre-filament formation stage as the filament rupture rate is smaller than their growth rate. An analysis similar to that required to explain the first I-V hysteresis loop with identical filament growth and rupture rates is adopted to generate the second I-V hysteresis as shown in Fig. 2.3.

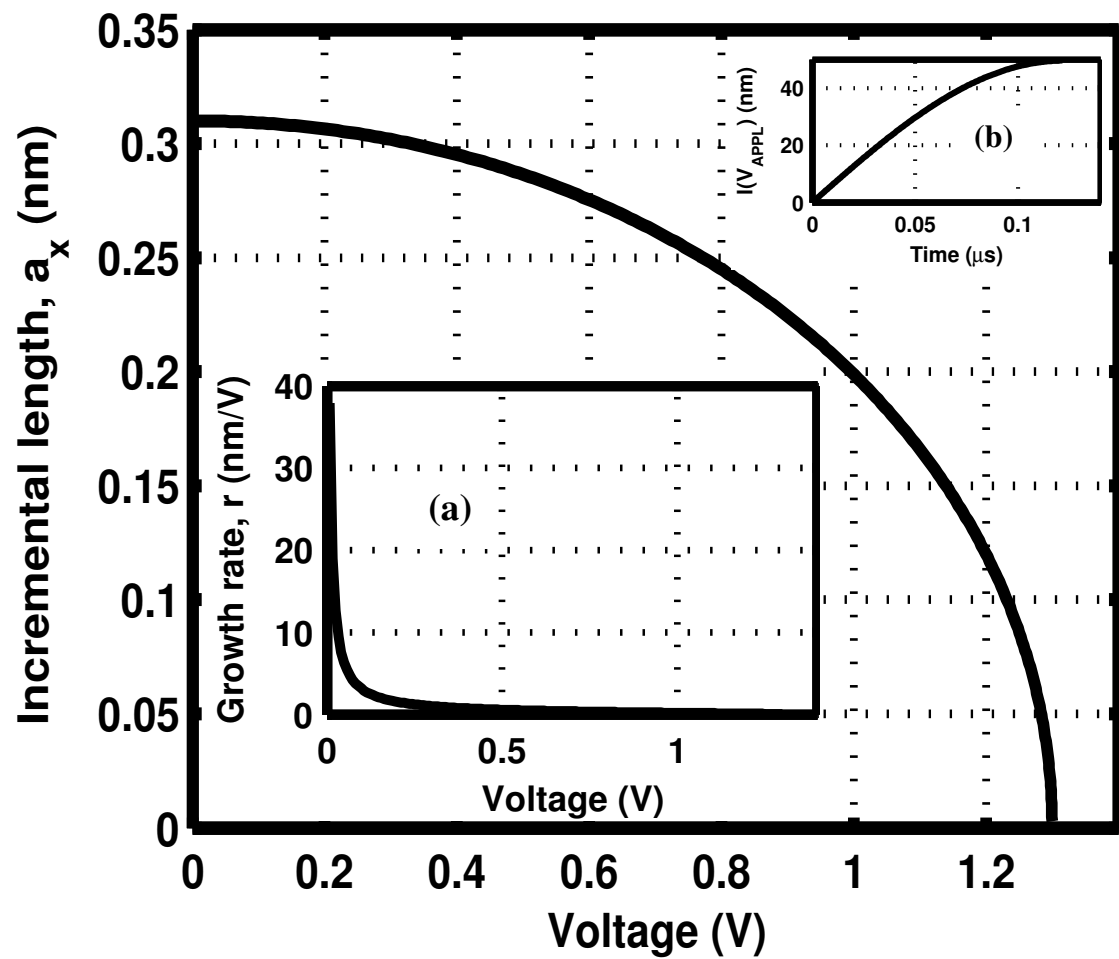


Figure 2.4. Incremental length of filament as a function of applied bias for a Pt/TiO₂/Pt memristor. Inset: (a) filament growth rate as a function of applied bias, (b) total length of filament as a function of time.

2.3 Analytical Derivation of Filament Growth Rates

The Understanding of the dynamics of filament growth and rupture rates is essential towards formulating observed memristor characteristics. With the application of an electric field E across the memristor terminals, TiO_2 oxidizes near the anode into $\text{Ti}_4\text{O}_5^{+2}$ ions (oxygen vacancies) and drift toward cathode to get reduced and form Ti_2O_3 filaments. The force exerted on the ions due to the applied electric field is expressed as,

$$F = qE = m^* \frac{dv}{dt} + m^* \frac{v}{\tau} \dots\dots\dots(2)$$

where, m^* is the effective mass of the charged ions, i.e. oxygen vacancies, and equals 4.5×10^{-22} gm, and τ is the mean free time between two successive collisions.

Assuming a sinusoidal applied bias, $V_{APPL} = V_0 \sin(\omega t)$, Eqn. (2) is solved for velocity of ions to yield the following expression:

$$v = \frac{q}{m^* d} \frac{\tau}{1 + \omega^2 \tau^2} V_0 [\sin(\omega t) - \omega \tau \cos(\omega t)] \dots\dots\dots(3)$$

It is to be noted that velocity v also depends upon the rate at which the oxygen vacancies are created and hence is a function of temperature. Assuming a single step reaction, the reaction rate constant, κ is given by the Arrhenius equation, $\kappa = A e^{-E_{ac}/RT}$. Here, $A = 10^6 \text{ s}^{-1}$ and $E_{ac} = 2 \text{ kJ}$ are the pre-exponential factor and activation energy of TiO_2 , respectively, $R = 8.314 \text{ JK}^{-1} \text{ mol}^{-1}$ is the gas constant, and T is the temperature in K [48].

Taking the above into consideration Eqn. (3) is modified as follows,

$$v = \kappa \frac{q}{m^* d} \frac{\tau}{1 + \omega^2 \tau^2} V_0 [\sin(\omega t) - \omega \tau \cos(\omega t)] \dots \dots \dots (4)$$

The filament growth rate is formulated by assuming that the first set of ions travel distance d towards the cathode in Δt seconds to form a filament of length a_1 . The subsequent ions originating at the anode travel shorter distances due to the lengthening of the filament. The second set of ions travel a distance $d - a_1$ in the second Δt time interval and adds to the filament length by a_2 with the total length becoming $a_1 + a_2$. Proceeding in this manner after m th Δt interval the filament length becomes $l(V_{APPL}) = \sum_m a_i$. It is

to be noted that a quasi-DC voltage applied for duration exceeding $\frac{d^2}{2\mu_v V_0} \frac{R_{OFF}}{R_{ON}}$ seconds

will allow the last ion to travel toward cathode, get reduced, and complete the filament formation process with the total length of filament becoming d [2]. Using Eqn. (2) and

equating it to $d = \frac{1}{2} \frac{dv}{dt} (\Delta t)^2$, and assuming zero initial ion velocity at the anode, for

the first two sets of ions we can write,

$$d = \frac{1}{2} \left(\frac{qE_0}{m^*} - \frac{v_0}{\tau} \right) (\Delta t)^2 \dots \dots \dots (5)$$

$$d - a_1 = \frac{1}{2} \left(\frac{qE_1}{m^*} - \frac{v_1}{\tau} \right) (\Delta t)^2 \dots \dots \dots (6)$$

where, E_0 and E_1 are the electric fields, v_0 and v_1 are the velocities for the first and second sets of ions, respectively. The incremental length a_1 is obtained by subtracting Eqn. (6) from Eqn. (5):

$$a_1 = \frac{1}{2} \left[\frac{q}{m^*} (E_0 - E_1) - \frac{1}{\tau} (v_0 - v_1) \right] (\Delta t)^2 \dots\dots\dots(7)$$

We can generalize the incremental length due to the traversal of the x th ion as,

$$a_x = \frac{1}{2} \left[\frac{q}{m^*} (E_{x-1} - E_x) - \frac{1}{\tau} (v_{x-1} - v_x) \right] (\Delta t)^2 \dots\dots\dots(8)$$

With the assumption $d - (a_1 + a_2 + \dots\dots\dots + a_{x-1}) \approx d - (a_1 + a_2 + \dots\dots\dots + a_x)$, which is valid

for smaller length of the filaments, Eqn. (8) takes the following form,

$$a_x = \frac{1}{2} \frac{qV_0}{m^*} \left[\frac{1}{d - (a_1 + a_2 + \dots\dots\dots + a_{x-1})} (\sin \omega t_{x-1} - \sin \omega t_x) - \frac{\kappa}{1 + (\omega\tau)^2} \frac{1}{d} \right] (\Delta t)^2 \dots\dots\dots(9)$$

$$\left\{ (\sin \omega t_{x-1} - \omega\tau \cos \omega t_{x-1}) - (\sin \omega t_x - \omega\tau \cos \omega t_x) \right\}$$

The incremental filament length described by Eqn. (9) satisfies the constraints that filaments stop growing if at least one of the following conditions are satisfied:

- i) $\Delta t = 0$: in this case the allowed duration for the ions to travel becomes zero,
- ii) $V_0 = 0$: in this case the applied bias V_{APPL} becomes zero, or
- iii) $\omega = 0$: in this case the term within the parentheses reduces to zero.

The room temperature variation of a_x as a function of the applied bias is plotted in Fig. 2.4 for the structure shown in Fig. 2.1. The frequency f , period, V_0 , τ , and Δt are assumed to be 2 MHz, 0.5 μ s, 1.3 V, 1 ps, and 0.5 ns, respectively [49]. Fig. 2.4 suggests that the incremental length a_x becomes zero as the applied bias reaches the maximum and the high conductivity filaments approach the counter electrode. The filament growth rate r is calculated by dividing a_x by the applied bias and is plotted as a function of the applied

bias in the inset (a) of Fig. 2.4. The growth rate decreases from 38 nm/V at 8 mV to 0.6 nm/V at 0.5 V, which for the sake of simplicity was assumed constant at 30 nm/V in the calculations reported in Sec. 2.2.1. The growth rate decreases from 0.6 nm/V to 2 pm/V at 1.3 V as the filament approaches the counter electrode. This growth rate was assumed constant at 0.2 nm/V in Sec. 2.2.1. The total filament length $l(V_{APPL})$ is shown as a function of time in inset (b). As time progresses the high conductivity filaments reach the counter electrode and after 0.13 μ s the total length becomes d . It is to be noted that assuming an ionic concentration of $8.5 \times 10^{19} \text{ cm}^{-3}$ $\frac{d^2}{2\mu_V V_0} \frac{R_{OFF}}{R_{ON}}$ equals 0.13 μ s re-confirming validity of the approach.

2.4 Thermal Effects

Having very high current densities through the filaments, heating of filaments in a memristor device is unavoidable [50] as is evident from the thermal imaging reported by Cölle *et al.* [34]. The effect of higher temperature on carrier transport is described by Eqn. (4) of the manuscript. The increase in temperature increases the redox reaction rate constant characterized by Arrhenius equation (Sec. 2.3) which in turn increases the filament growth and rupture rates. A 33% increase in the filament growth and rupture rates, due to elevated temperature, would increase the filament assisted tunneling component I_{FA} , calculated from Eq. (1), at a higher rate. It is to be noted that calculation of thermal effects presented here builds upon the method outlined by Sato *et al.* [50] and does not consider interface effects and grain boundary induced scattering. This is also in accordance with Knauth *et al.* [51] that diffusion of ions is slower through grain

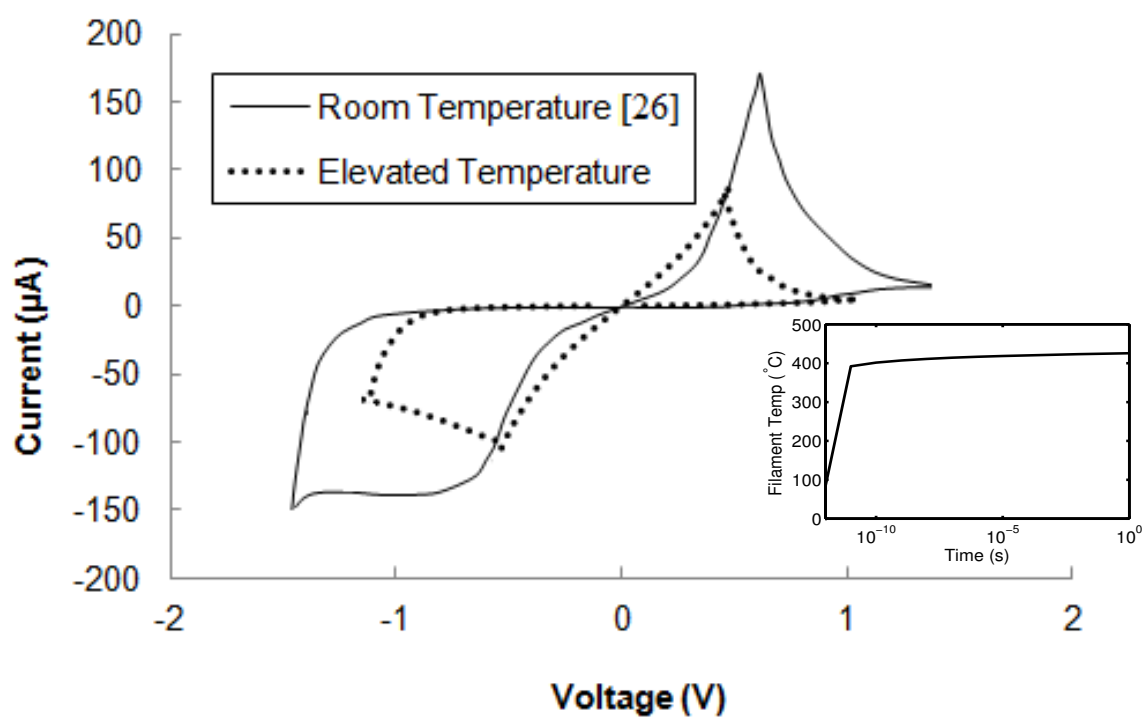


Figure 2.5. Temperature dependence of hysteresis in the I-V characteristics of Pt/TiO₂/Pt structures. The increase in filament temperature with respect to time has been shown in the inset.

boundaries in nanocrystalline TiO₂ at higher temperature. Modified I-V characteristic due to thermal effects is shown in Fig. 2.5. The structure simulated is the Pt/TiO₂/Pt memristor shown in Fig. 2.1. With increasing temperature the threshold voltage required for switching is observed to decrease. Moreover, R_{ON} increases with temperature lowering the R_{OFF}/R_{ON} ratio. It is important to note that R_{ON} and R_{OFF} are controlled by separate physical processes and, thereby, reasonable R_{OFF}/R_{ON} ratio may be maintained by having a structure with a thicker organic layer. The determination of temperature due to the flow of current follows the method outlined by Sato *et al.* [50] where the increase in temperature, ΔT , due to the longitudinal and radial components of the thermal conductivity is formulated as:

$$\Delta T = \frac{1}{K_R + K} \frac{V^2}{R} \dots\dots\dots (10)$$

where, K is the filament thermal conductance and K_R is the radial thermal conductance in TiO₂.

$$K_R = \frac{2\pi k' d / 4}{\ln(r_2 / r_1)} \dots\dots\dots (11)$$

Here k' is the thermal conductivity of TiO₂ and equals 6.69 W/m-K, d is the thickness of the oxide layer, r_1 is the filament radius, r_2 is the radius of the cylindrical region where the temperature drops down to $1/e$ of the temperature at the filament center line [50]. r_2 is estimated using the following relationship [50]:

$$r_2 = r_1 + \Delta r = r_1 + \sqrt{\frac{4k'}{S'd'}} t \dots\dots\dots (12)$$

Here t is the heating time, $S' = 0.6894 J / gm - K$ and $d' = 4.13 g / cm^3$ are the specific heat and density, respectively, of TiO₂ [52, 53]. The longitudinal thermal conductance

$K = \frac{k\pi r_1^2}{d/2}$, where k is the thermal conductivity of Ti_2O_3 filaments and is assumed to be 4

W/m-K [54]. The increase in filament temperature as a function of time is plotted in the inset of Fig. 2.5, demonstrating an initial rapid increase that settles around 425 °C. The resulting I-V characteristic is shown in Fig. 2.5. It is important to note that rise in temperature has detrimental effect on the performance of a memristor. With an increase in temperature R_{ON} also increases making R_{OFF}/R_{ON} ratio smaller. Hence at high temperature RRAM employing memristors demands for a more sensitive detection circuitry.

2.5 Reliability

A higher filament growth rate as compared to rupture rate results in the formation of residual filaments the number of which increases with each cycle of the I-V swing. This leads us to believe that if the bias voltage traverses a number of cycles, fragmented high conductivity filaments may fill the entire device driving it to a low resistance state with no observable switching, however, at this time we do not have a clear understanding of the failure mechanism in such devices. This assertion is supported by Hsiung *et al.* [55] reporting the presence of Ag droplets in Ag/ TiO_2 /Pt structure after repeated I-V swings. Sawa *et al.* [46] reported collapse in the I-V hysteresis after 10^6 cycles. It is possible that the I-V hysteresis may be restored by exposing the device to oxygen or CO_2 at elevated temperatures [22] $2Ti_2O_3 + O_2 \rightarrow 4TiO_2$ or $2Ti_2O_3 + CO_2 \rightarrow 4TiO_2 + C$.

2.6 Conclusion

The observed hysteresis in two terminal memristor devices is attributed to the presence of filaments. Analytical derivation of filament growth rate is provided. Currents through high and low conductivity filaments as well as filaments assisted tunneling current are used to explain the observed I-V characteristics. Memristors employing organics are explained using the same physical mechanism demonstrating that the organic layer is not directly responsible for switching.

Chapter 3 : DC, Transient, and RF Circuit Models

3.1 Introduction

Several attempts [9, 17, 56] have been made, utilizing constituent equations or charge-flux relationship, to develop behavioral models of memristors that can be implemented in circuit simulation tools such as SPICE, Spectre, Verilog etc. Bendarli *et al.* [56] and Biolek *et al.* [17] implemented circuits using SPICE, based upon oxygen vacancy movement model proposed by Strukov *et al.* [2]. The boundary conditions were incorporated using different methods -- the former proposed a clipping circuit while the latter formulated a window function. Zhang *et al.* [57], on the other hand, proposed a circuit model assuming a piecewise linear charge-flux characteristic and validated the model by simulating a chaotic circuit. A behavioral model, based upon reported I-V data, was reported by Mazady *et al.* [58] to investigate circuit performance of memristors which does not identify the different conduction mechanisms present in the device. The model is modified in this chapter where different current components, identified following the discussion in [16], are represented as different circuit components.

Behavioral models provide an overview of the expected characteristics but fail to provide an insight into the various process dependent parameters that can be tweaked to optimize the device and enhance circuit performances. A circuit model based upon the underlying physics of the device, on the other hand, allows optimization of circuit performance by tweaking physical structures and bias conditions (example – device dimension,

temperature etc.) of memristor and is the topic of the present chapter. Moreover, the present work is the only work of this sort that is not based on a behavioral model rather based on the underlying physics of the device that takes into account the physical current components associated with the material chemistry.

Widespread adoption of memristors in various applications requires a transient model allowing the determination of key performance parameters, namely – switching speed and frequency response. A carrier dynamics based model permits the determination of the time required by the device to stabilize to a state (SET, RESET), for applications ranging from RRAMs to neural networks. In an attempt to develop transient models utilizing carrier dynamics in a memristor, Pickett *et al.* [18] proposed an empirical relationship based upon the time rate of change of the tunneling width while Abdallah *et al.* [59] developed a SPICE circuit representation of memristor based on the model. For a Pt/TiO₂(50nm)/Pt structure, the reported relationship assumes a minimum tunneling distance of 1.1 nm that contradicts the experimentally determined tunneling distance of 0 nm during ON state when the high conductivity filaments connect both electrodes [24]. Moreover, the required fitting parameters needed by the empirical equations to perform calculations are valid only for the chosen device. Chung *et al.* [60] reported transient response of TiN/TiO_x/HfO_x/TiN and noted that tunneling through TiO_x, rather than through HfO_x, was responsible for resistance switching. Unlike Pickett *et al.* they correctly assumed a 0 nm tunneling distance during ON state of the device and reported the change in tunneling distance as a function of time for different reset voltages. The switching time was found to be related to the ionized charge (oxygen vacancy) migration

and the rate of redox reaction for filament formation/rupture. However, the model proposed by Chung *et al.* is applicable when the tunneling distance is large and applied electric field is small. The assumption of a small applied electric field is valid for small read voltages but not for operations where the device changes state (SET, RESET).

In this chapter, dynamical behavior of memristors is developed based on the underlying physics [16]. Tunneling barrier width (or filament length) is used as the state variable that decreases to 0 nm during the ON state of the device. The formulation explains the coupled electronic and ionic conduction observed in such devices [2] and is validated through simulations. The developed analytical model of the memristor dynamics allows predicting the transient and RF characteristics and more importantly identifies the dominating factors responsible for such behavior. We also develop circuit representations, extracted from the dynamic characteristics of memristive systems, for transient and RF analysis.

3.2 DC Circuit Model

3.2.1 Metal/Insulator/Metal Memristors

Development of a circuit model representing memristor's operation poses several challenges. Firstly, the differential equations governing the memristor behavior are non-linear and cross-coupled and hence finding a closed form solution is a formidable task. Secondly, transformation of these equations into Fourier or Laplace domain is also not as straightforward as it is for linear circuit components.

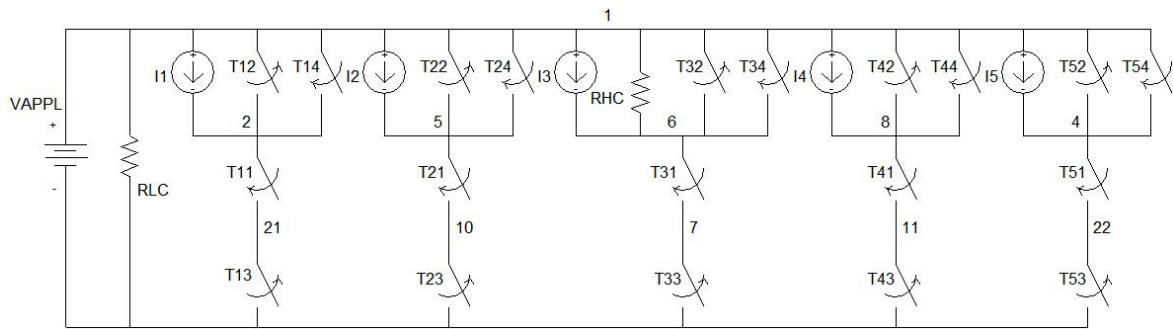


Figure 3.1. Proposed DC circuit model of memristors. I1 through I5 represent filament assisted tunneling currents in different regions of operation. RHC and RLC represent resistances of the high and low conductivity filaments

The proposed circuit model as shown in Fig. 3.1 builds upon the physical characteristics of a memristor as described in [16]. Currents I_1 , I_2 , I_4 , and I_5 are obtained by fitting the filament assisted tunneling currents in regions oa , ab , cd , and do (Fig. 3.2). Calculation of the filament assisted tunneling currents follows the method outlined by Mazady *et al.* [16] which is dependent on the related electro-chemistry for these devices. The memristor remains in SET state during region boc . Conduction through high conductivity filaments modeled using R_{HC} together with current through Schottky contacts modeled as I_3 gives the total current in this region. The parametric representations of currents I_1 through I_5 , calculated based upon the physics of the conduction processes, are tabulated in Table 3.1. R_{LC} and R_{HC} represent the resistances of the low conductivity and high conductivity filaments and are calculated to be 637 k Ω and 63.7 k Ω , respectively [16]. T_{i1} and T_{i4} are time dependent normally open switches and T_{i2} and T_{i3} are time dependent normally closed switches (where $i = 1$ to 5). The switches are designed (Table 3.2) such that I_1 through I_5 remain active only during appropriate regions of operation of the I-V characteristics. A triangular wave of 50 Hz, as shown in the inset of Fig. 3.2, is used as the applied voltage, V_{APPL} , to simulate the quasi-DC hysteresis characteristics of the memristor in PSPICE. The parametric equations used to calculate the time at which the switch will get energized is given in Table 3.3. The circuit representation is general enough to be applicable to any memristor irrespective of material types and geometries. This can be achieved by suitable modification of the voltage coefficients of the parametric equations of Table 3.1 and the switching transition times of Table 3.2.

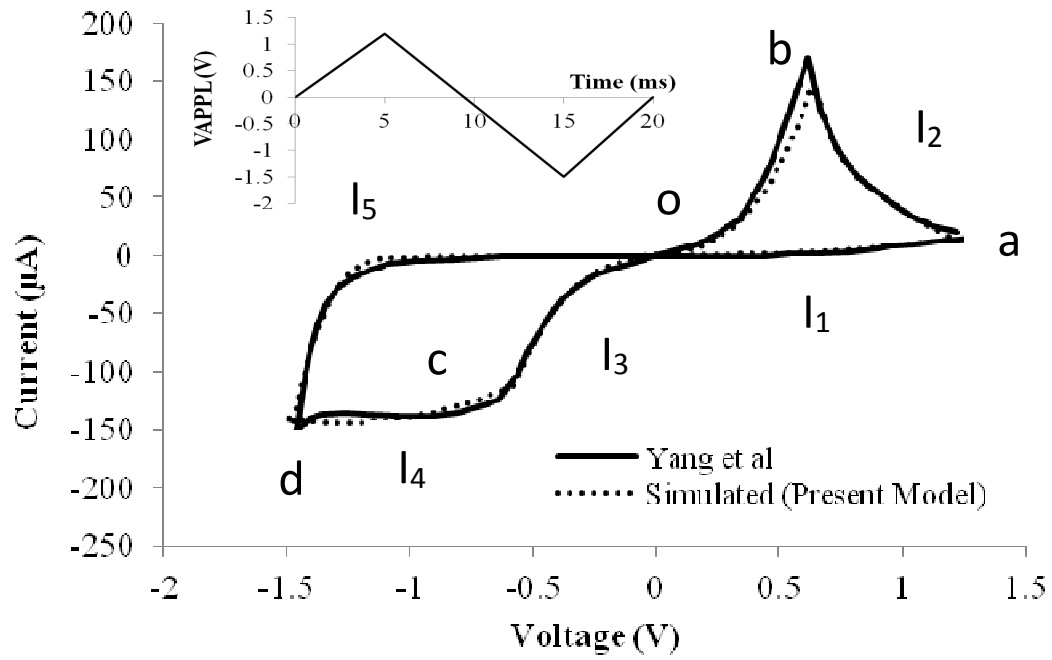


Figure 3.2. Simulated I-V characteristic of a Pt/TiO₂/Pt memristor with TiO₂ thickness of 50 nm along with experimental data. Inset: Applied voltage across the memristor terminals. Filament assisted tunneling currents I_1 through I_5 are active during regions *oa*, *ab*, *boc*, *cd*, and *do*.

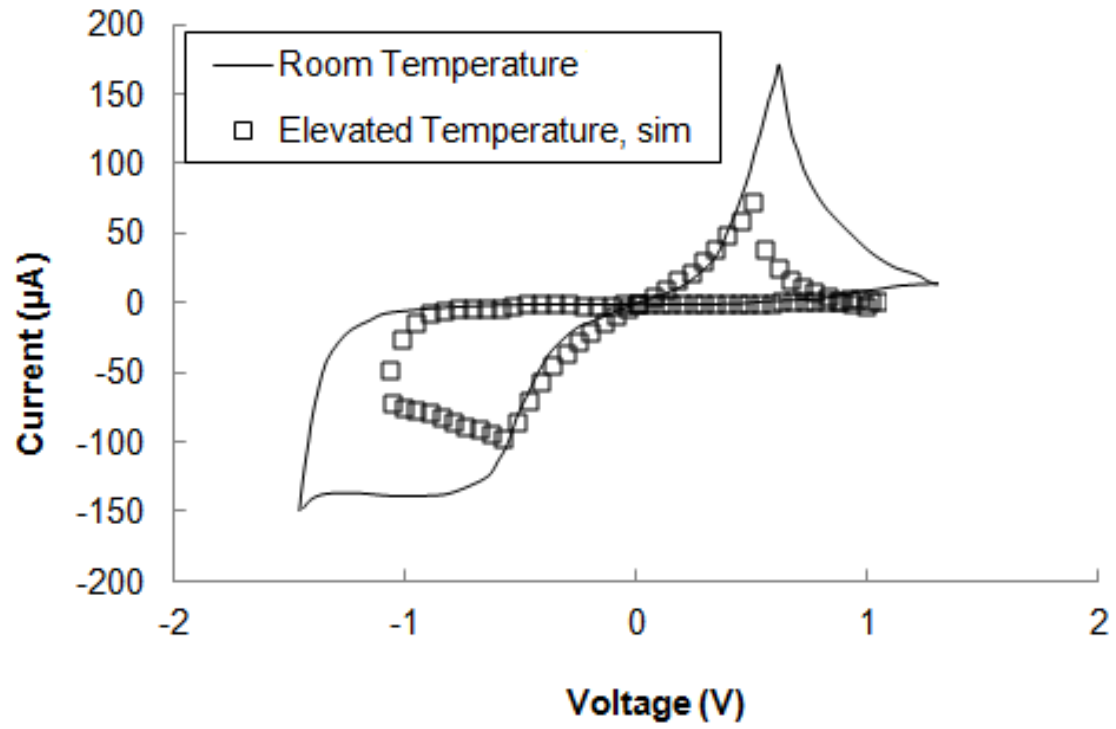


Figure 3.3. Simulation of thermal effects of memristors. Increased temperature decreases the threshold voltages required for SET and RESET switching.

Table 3.1. Parametric representation of filament assisted tunneling currents at room temperature and elevated temperature

	Room temperature	Elevated temperature
$I_1(\mu A)$	$-1.18V_{APPL}^4 + 354V_{APPL}^3 - 236V_{APPL}^2 + 7.8V_{APPL} - 0.4$	$266V_{APPL}^3 - 514V_{APPL}^2 + 359V_{APPL} - 8.4$
$I_2(mA)$	$-4.8V_{APPL}^4 - 187V_{APPL}^3 + 276V_{APPL}^2 - 181V_{APPL} + 4.6$	$2.7V_{APPL}^4 - 8.8V_{APPL}^3 + 109V_{APPL}^2 - 6.1V_{APPL} + 1.3$
$I_3(\mu A)$	$500V_{APPL}^3 + 0.5V_{APPL}^2 + 1.16V_{APPL} - 0.05$	$2542V_{APPL}^3 - 2.7V_{APPL}^2 + 70V_{APPL} + 0.2$
$I_4(\mu A)$	$69V_{APPL}^2 + 172V_{APPL} - 345$	$-243V_{APPL}^2 - 943V_{APPL} - 1427$
$I_5(mA)$	$-2.1V_{APPL}^4 - 8V_{APPL}^3 - 1.15V_{APPL}^2 - 7.3V_{APPL} - 1.7$	$1.5V_{APPL}^5 + 3.9V_{APPL}^4 + 3.7V_{APPL}^3 + 1.6V_{APPL}^2 + 0.3V_{APPL} + 0.02$

Table 3.2. Switching transition times

	Room Temperature (ms)	Elevated Temperature (ms)	Organic Layer (ms)
T₁₁	> 0.83	> 2.08	>0.42
T₁₂	< 0.83	< 2.08	<0.42
T₁₃	< 5	< 4.17	<3.75
T₁₄	> 5	> 4.17	>3.75
T₂₁	> 5	> 5.74	>20
T₂₂	< 5	< 5.74	>0
T₂₃	< 7.04	< 7.59	>0
T₂₄	> 7.04	> 7.59	>20
T₃₁	> 7.04	> 7.59	>6.11
T₃₂	< 7.04	< 7.59	<6.11
T₃₃	< 11.56	< 11.48	<13.15
T₃₄	> 11.56	> 11.48	>13.15
T₄₁	> 11.56	> 11.48	>13.15
T₄₂	< 11.56	< 11.48	<13.15
T₄₃	< 15	< 13.51	<14.26
T₄₄	> 15	> 13.51	>14.26
T₅₁	> 15	> 16.33	>15.67
T₅₂	< 15	< 16.33	<15.67
T₅₃	< 17.33	< 19.66	<20
T₅₄	> 17.33	> 19.66	>20

Table 3.3. Equations to translate V_{APPL} into time

Time range	Equation
0 to 5 ms	$t = V_{APPL}/0.24$
5 to 15 ms	$t = -3.7 \times (V_{APPL} - 2.55)$
15 to 20 ms	$t = (V_{APPL} + 1.5)/0.3 + 15$

Table 3.4. Parametric representation of filament assisted tunneling currents in Pt/LB/Ti/Al memristors

	Room temperature
$I_1 (\mu A)$	$1.5 \times 10^{-23} \exp(67.6 V_{APPL})$
$I_2 (\mu A)$	0
$I_3 (\mu A)$	0
$I_4 (\mu A)$	$-5.3 V_{APPL}^2 - 14.2 V_{APPL} - 9.8 mA$
$I_5 (\mu A)$	$-255.1 V_{APPL}^2 - 156.2 V_{APPL} - 19.07 \mu A$

The presented circuit model allows simulating the heating effects in memristors. Upon suitable modification of I_1 through I_5 (see Table 3.1) and the switches (see Table 3.2), the SPICE simulation successfully generates the I-V characteristic (see Fig. 3.3) demonstrating the versatility of the method [16].

3.2.2 Organic Memristors

A method similar to that mention in Section A is applied to investigate DC performance of organic memristors. The Pt/LB/Pt structure reported by Stewart *et al.* is considered in the analysis [42]. The resistance of the low and high conductivity filaments, R_{LC} and R_{HC} for this structure, are assumed to be 10.5 k Ω and 1.05 k Ω , respectively [16]. Currents I_1 , I_4 , and I_5 (Table 3.4) are obtained by fitting the filament assisted tunneling currents in regions *oab*, *cd*, and *do*, respectively (Fig. 3.4). A rather thin active region of 2.8 nm makes I_1 dominant making I_2 insignificant in comparison allowing it to be neglected. Current I_3 can also be neglected due to the absence of any observed Schottky effect in organic layer based memristors [16]. The switching transition times are given in Table 3.2. The present model shows good correlation with the reported data, as evident from Fig. 3.4.

Being physics based, the proposed circuit model can account for the changes in the I-V characteristics in the subsequent cycles of the applied bias. The filament assisted tunneling currents calculated for subsequent I-V excursion loops are represented by a set of parametric equations obtained by fitting the experimental data. For the n th I-V sweep, the filament assisted tunneling currents I_1 , I_4 and I_5 are expressed as follows:

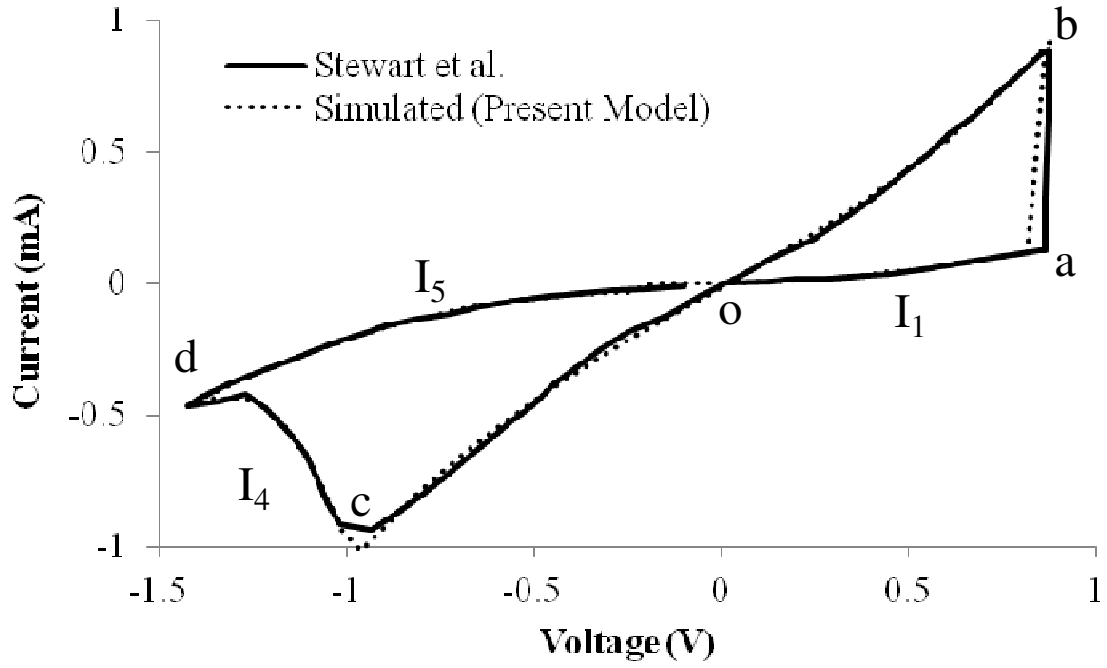


Figure 3.4. Experimental and simulated I-V characteristic of a Al/Ti/LB/Pt memristor. I_1 , I_4 , and I_5 are filament assisted tunneling currents in regions oab , cd , and do respectively. Current in region boc is determined by R_{HC} .

$$I_1 = A_1 \exp(B_1 V_{APPL}) \quad (1)$$

where $A_1 = 1.82 \times 10^{-29} n^{39.42}$ and $B_1 = -22.11n + 88.81$

$$I_4 = A_4 V_{APPL}^2 + B_4 V_{APPL} + C_4 \quad (2)$$

where, $A_4 = 4.55 \times 10^{-4} n^2 - 1.39 \times 10^{-3} n - 4.35 \times 10^{-3}$,

$B_4 = 1.095 \times 10^{-3} n^2 - 3.72 \times 10^{-3} n - 1.16 \times 10^{-2}$,

and $C_4 = 6.55 \times 10^{-4} n^2 - 2.54 \times 10^{-3} n - 7.95 \times 10^{-3}$.

$$I_5 = A_5 V_{APPL}^3 + B_5 V_{APPL}^2 + C_5 V_{APPL} + D_5 \quad (3)$$

where, $A_5 = 5.96 \times 10^{-5} n + 1.58 \times 10^{-5}$,

$B_5 = -7.78 \times 10^{-5} n^2 + 4.39 \times 10^{-4} n - 4.72 \times 10^{-4}$,

$C_5 = -5.49 \times 10^{-5} n^2 + 2.97 \times 10^{-4} n - 3.15 \times 10^{-4}$,

and $D_5 = -3.89 \times 10^{-6} n^2 + 2.06 \times 10^{-5} n - 2.42 \times 10^{-5}$.

The corresponding switching times (in ms) using a 50 Hz input signal are as follows:

$$T_{11}/T_{12} = 0.42 \quad , \quad T_{13}/T_{14} = -0.5n + 4.18 \quad , \quad T_{31}/T_{32} = 0.82 \ln(n) + 6.13 \quad ,$$

$$T_{33}/T_{34}/T_{41}/T_{42} = 0.095n^2 - 0.11n + 13.16 \quad , \quad T_{43}/T_{44} = 14.26 \quad , \quad T_{51}/T_{52} = 15.67 \quad ,$$

$$T_{53}/T_{54} = 20$$

I-V characteristics, using these parametric equations, for the first five consecutive voltage sweeps are shown in Fig. 3.5. The calculations of subsequent I-V curves incorporate

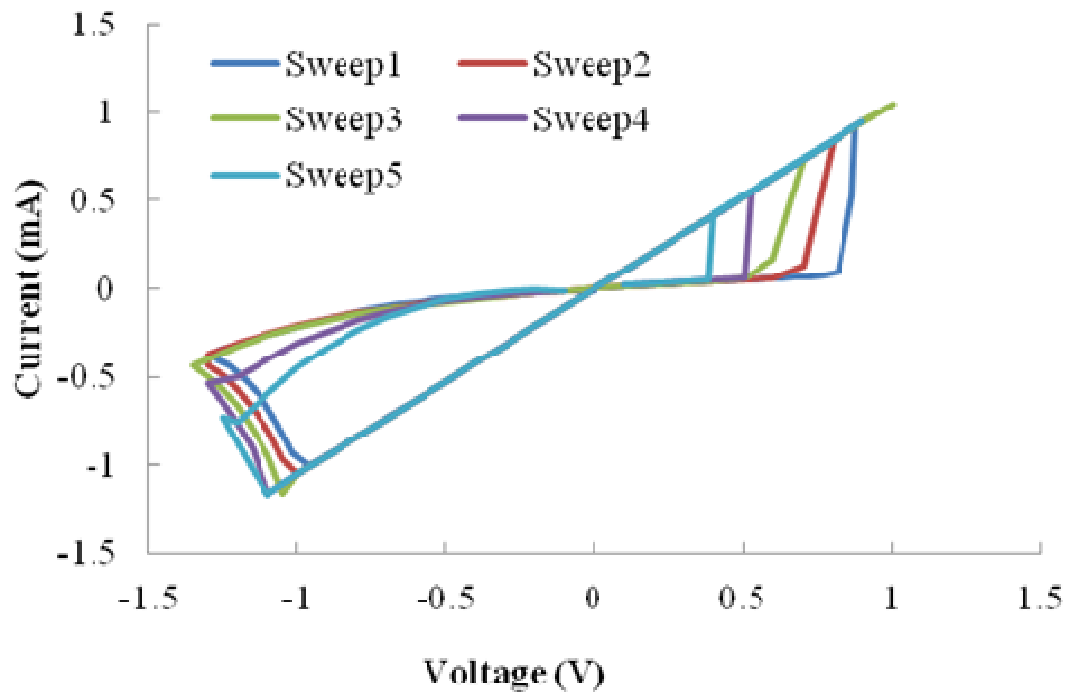


Figure 3.5. Simulated I-V characteristics of a Al/Ti/LB/Pt memristor for 5 consecutive voltage sweeps. Fragmented filaments remaining after each sweep result in decreased threshold voltages.

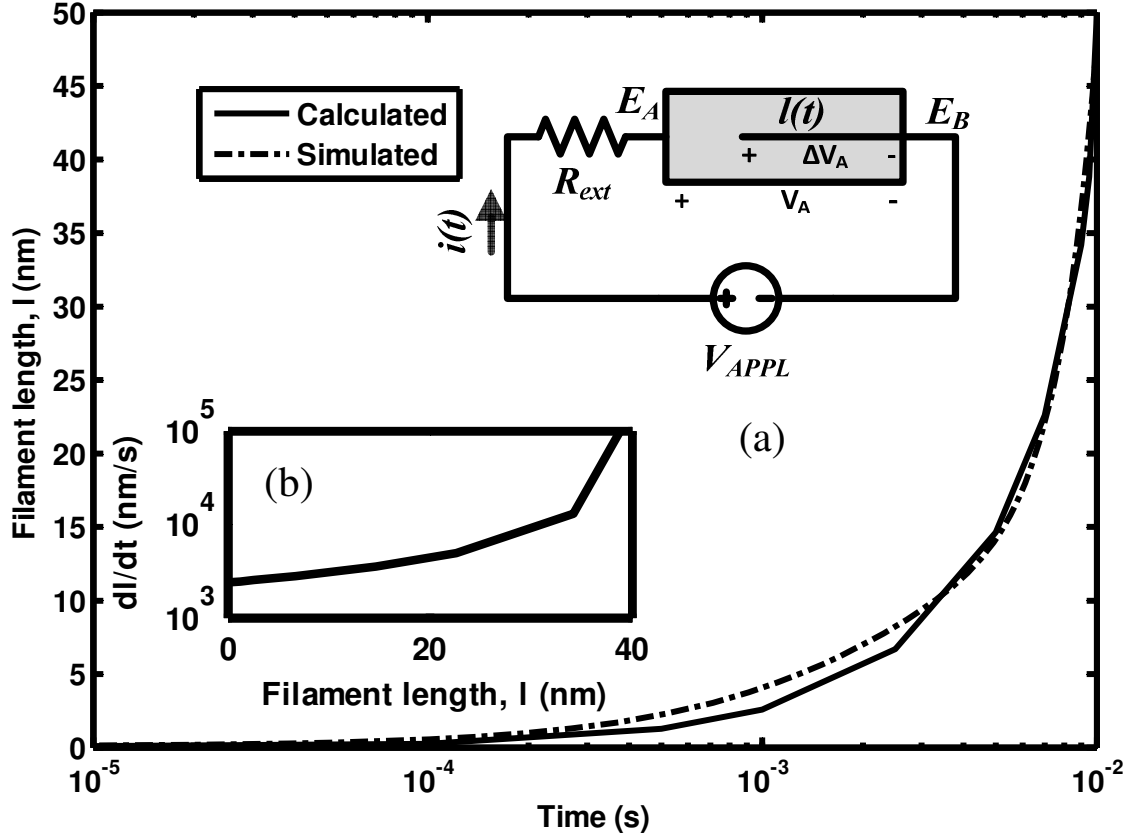


Figure 3.6. Filament length as a function of time during SET transition calculated (solid line) using Eqn. (11) and simulated (dashed line) using Cadence. Filament length increases from 0 nm. As the length increases, filament grows more rapidly owing to a higher electric field. Inset: (a) Schematic diagram of memristor under an applied bias V_{APPL} . (b) Filament growth rate as a function of filament length during SET transition calculated using Eqn. (12).

changes in the filament assisted currents and threshold voltages arising from residual filaments remaining after the completion of previous cycles. Threshold voltage is defined as the voltage where transition from a to b (Fig. 3.4) takes place. Memristors employing different organic compounds would require modifications of the parametric equations to calculate coefficient A 's through D 's and the switching transition times.

3.3 Dynamic analysis of memristors

3.3.1 Transition to ON State

Schematic of a memristor under the application of a positive applied bias to electrode E_A is shown in inset (a) of Fig. 3.6. The total current flowing through the device can be expressed as,

$$i = \frac{V_A - \Delta V_A}{\rho_{OFF} \frac{d - l(t)}{A}} \quad (4)$$

Where, V_A is the (internal) voltage drop across the memristor, ΔV_A is the voltage drop across the high conductivity filament, ρ_{OFF} is the resistivity of TiO_2 , A is the cross sectional area of the device, and $l(t)$ is the length of the high conductivity filament. R_{ext} is the resistance external to the memristor and accounts for resistances due to the electrodes, wires and interconnects, and the internal resistance of the source. It is important to note that device parasitics such as lead inductance, electrode to electrode bulk capacitance etc. is ignored in these calculations assuming electrically shorter lengths of the external wires, and typical lengths of the device (> 50 nm).

The voltage drop across the high conductivity filament can be expressed as,

$$\Delta V_A = \frac{l(t)}{k_1(d-l(t))+l(t)} V_A \quad (5)$$

where, $k_1 = \rho_{OFF} / \rho_{ON}$ with ρ_{ON} being the resistivity of the Ti_2O_3 filaments.

Using the expression $V_A = V_{APPL} - iR_{ext}$ and substituting (4) results in,

$$\Delta V_A = \left(\frac{d-l(t)}{k_2} + 1 \right) V_A - \frac{d-l(t)}{k_2} V_{APPL} \quad (6)$$

Here, $k_2 = AR_{ext} / \rho_{OFF}$. Equating equations (5) and (6) the relationship between the internal voltage drop and the applied bias is obtained.

$$V_A = \frac{\frac{d-l(t)}{k_2}}{1 + \frac{d-l(t)}{k_2} - \frac{l(t)}{k_1(d-l(t))+l(t)}} V_{APPL} \quad (7)$$

The growth rate of the high conductivity filaments can be written as,

$$\frac{dl}{dt} = \mu_{ON} \frac{V_A - \Delta V_A(t)}{d-l(t)} \quad (8)$$

where μ_{ON} is the mobility of ions that create the high conductivity filaments. It is to be noted that for filament lengths much shorter compared to the thickness of the oxide layer ($l(t) \ll d$) (valid for small bias voltages), ΔV_A is negligible and equation (8) reduces to

$$l = \frac{\mu_{ON}}{d} \int V_A dt . \quad \text{Under this condition } l \text{ becomes a linear function of the flux linkage}$$

$\phi = \int V_A dt$ and is the basis of the models reported by Jo *et al.* and Chung *et al.* [15, 60].

Substituting Eqn. (5) into Eqn. (8) followed by an integration from $t = 0$ to t , yields,

$$\left(1 - \frac{1}{k_1}\right)l^2 - 2dl + 2\mu_{ON}V_A t = 0 \quad (9)$$

Assuming $k_1 \gg 1$ (i.e. $\rho_{OFF} \gg \rho_{ON}$), equation (9) can be simplified to,

$$l^2 - 2dl + 2\mu_{ON}V_A t = 0 \quad (10)$$

Substituting V_A [equation (7)] in (10) and re-arranging the terms results in a polynomial equation allowing the determination of $l(t)$

$$\begin{aligned} & (k_1 - 1)l^4 - (k_1 k_2 + 4k_1 d - 3d)l^3 + \left\{ 3k_1 k_2 d + (5k_1 - 2)d^2 \right. \\ & \quad \left. + 2(k_1 - 1)\mu_{ON}V_{APPL}t \right\} l^2 \\ & - \left\{ 2k_1 d^2 (k_2 + d) + 2\mu_{ON}d(2k_1 - 1)V_{APPL}t \right\} l + 2\mu_{ON}k_1 d^2 V_{APPL}t = 0 \end{aligned} \quad (11)$$

Eqn. (11) relates the filament length or tunneling width to time and is plotted in Fig. 3.6 for an applied bias of 1.25V. A , R_{ext} , ρ_{OFF} , k_1 , d , m , and μ_{ON} are assumed to be 50nm×50nm, 15 Ω , 10^7 Ω -cm, 100, 50 nm, 4.5×10^{-22} gm, and 10^{-9} cm²/(V-s), respectively. As observed, the filament grows very slowly during the first 1 ms and may be explained as follows. Initially, oxygen vacancies are created near the anode and they travel toward the cathode in response to the applied bias. As a result, filament growth depends upon the rate of redox reaction and temperature. Once enough $Ti_4O_5^{+2}$ ions come in contact with the tip of the already formed high conductivity filaments, the filament growth rate increases due to reduced tunneling distance followed by a concomitantly increasing electric field. The time-varying filament length is modeled as a voltage source in Cadence and the results are plotted in Fig. 3.6 showing good agreement with calculated data. For a practical device with $k_1 > 100$, Eqn. (11) can be simplified as:

$$(5k_1d^2 + k_3t)l^2 + 2dk_3tl + d^2k_3t = 0$$

where, $k_3 = 2k_1\mu_{ON}V_{APPL}$

The filament growth rate can be obtained by differentiating Eqn. (11) with respect to time.

$$\begin{aligned} \frac{dl}{dt} = & \left[\frac{4(k_1-1)l^3 - 3(k_1k_2 + 4k_1d - 3d)l^2 + 2\{3k_1k_2d + (5k_1-2)d^2\}l}{+ 4(k_1-1)\mu_{ON}V_{APPL}tl - \{2k_1d^2(k_2+d) - 2\mu_{ON}d(2k_1-1)V_{APPL}t\}} \right]^{-1} \\ & \times \left[(1-k_1)\mu_{ON}V_{APPL}l^2 + 2\mu_{ON}d(2k_1-1)V_{APPL}l - 2\mu_{ON}k_1d^2V_{APPL} \right] \end{aligned} \quad (12)$$

A plot of the filament growth rate as a function of the existing filament length is shown in Fig. 3.6 inset (b). As the filament length increases, the growth rate is assisted by the increase in electric field due to a reduced tunneling length. This in turn results in another fold increase in the filament growth rate. Eventually the high conductivity filaments reach the counter electrode reducing the tunneling distance to zero and the filament stops growing any further.

3.3.2 Transition to OFF State

With the application of a negative bias the high conductivity filament begins to retract following the electrochemistry described in [16]. The high conductivity Ti_2O_3 filaments dissolve into insulating TiO_2 by a thermally activated oxidation process. As a result, the tunneling distance $d_{eff}(t)=d-l(t)$ increases from 0 to some positive value. Following a treatment similar to that as outlined in section 3.3.1, the relationship between the internal and applied bias voltages can be expressed as,

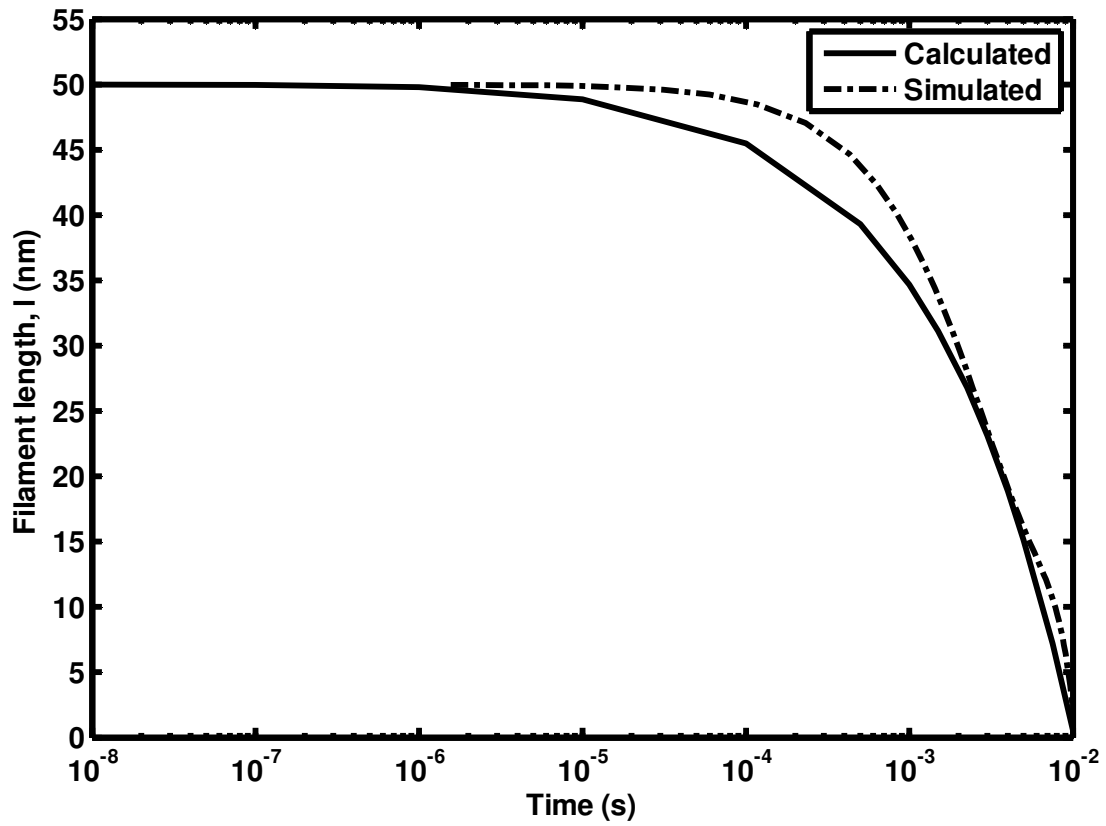


Figure 3.7. Filament length as a function of time during RESET transition, calculated using equation (17) and simulated using Cadence. Once V_{APPL} of -1.25 V is applied, the high conductivity filament starts to rupture after 1 μ s and the devices transition to RESET state.

$$V_A = \frac{\frac{d_{eff}(t)}{k_2}}{1 + \frac{d_{eff}(t)}{k_2} - \frac{d - d_{eff}(t)}{k_1 d_{eff}(t) + d - d_{eff}(t)}} V_{APPL} \quad (13)$$

The rupture rate of the high conductivity filament can be written as:

$$\frac{dd_{eff}(t)}{dt} = \mu_{ON} \frac{V_A - \Delta V_A(t)}{d_{eff}(t)} \quad (14)$$

which after some manipulations can be re-written as follows:

$$\int \left\{ \left(1 - \frac{1}{k_1} \right) d_{eff}(t) + \frac{d}{k_1} \right\} dd_{eff}(t) = \int \mu_{ON} V_A dt \quad (15)$$

Under the assumption that $k_1 \gg 1$ ($\rho_{OFF} \gg \rho_{ON}$), Eqn. (15) results in

$$d_{eff}^2(t) + 2 \frac{d}{k_1} d_{eff}(t) - 2 \mu_{ON} V_A t = 0 \quad (16)$$

Substituting V_A from (13), equation (17) can be re-arranged as follows:

$$\begin{aligned} & (k_1 - 1) d_{eff}^3(t) - \left\{ k_2(k_1 - 1) + \left(3 - \frac{2}{k_1} \right) d \right\} d_{eff}^2(t) \\ & + 2 \left\{ k_2 d + \frac{d^2}{k_1} - \mu_{ON} V_{APPL} t (k_1 - 1) \right\} d_{eff}(t) - 2 d \mu_{ON} V_{APPL} t = 0 \end{aligned} \quad (17)$$

Eqn. (17) can be solved numerically to investigate the dependence of the tunneling distance on different parameters during the RESET process. Filament length as a function of time during RESET is plotted in Fig. 3.7. Values of the different parameters are assumed to be the same as that used for SET transition. Prior to the onset of the RESET process, the high conductivity filaments bridge both the electrodes separated by the thickness of the TiO_2 layer - 50 nm in this case. Once the applied bias voltage

exceeds (becomes more negative) -1.25 V across the electrodes, filaments start to rupture with time due to thermally assisted redox reaction at the cathode [16]. If the polarity of the bias voltage remains unchanged, all the high conductivity filaments are dissociated into TiO_2 bringing the filament length to 0 nm. For a practical device with $k_I > 100$, Eqn. (17) can be simplified as:

$$k_1 d_{eff}^3 - k_3 d_{eff} t + \frac{d}{k_1} t = 0$$

3.4 Circuit Representation for Transient Analysis

Based upon the formulation developed to study carrier dynamics, in memristors, a circuit allowing the study of its transient behavior can be realized. Fig. 3.8 inset, shows such a transient circuit representing Pt/ TiO_2 (50nm)/Pt memristor.

The development of the transient circuit proceeds by identifying the physical processes as described in [16] and correlating them to different circuit parameters. It is evident from [16] that there are stored charges adjacent to the electrode E_A and also near the tips of the filaments in the form of oxygen vacancies giving rise to capacitance, $C(t) = \epsilon_{\text{TiO}_2} A_{fil} / d_{eff}(t)$, where $\epsilon_{\text{TiO}_2} = 110 \epsilon_0$ is the permittivity of TiO_2 and ϵ_0 is the permittivity of free space. The series resistance, R_{ext} accounts for the series combination of resistances due to (i) the electrodes, (ii) the wires and interconnects, and (iii) internal resistance of the source. L_1 and L_2 represent the anode and cathode lead inductances. C_b is the geometrical capacitance arising from separation of contact electrodes by an insulating TiO_2 matrix.

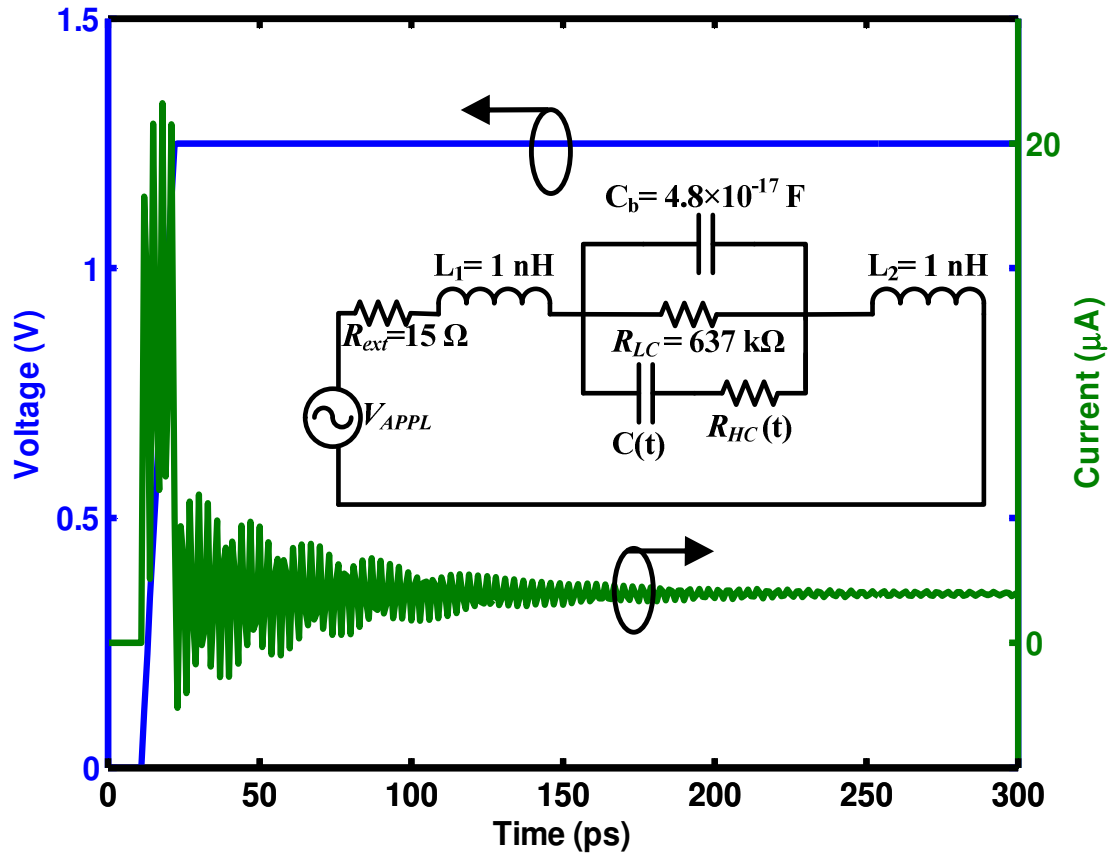


Figure 3.8. Simulated transient characteristics during SET process. It takes approximately 210 ps for the device to reach steady state for SET transition. Inset: Schematic circuit representation of a 50 nm TiO₂ memristor for transient analysis.

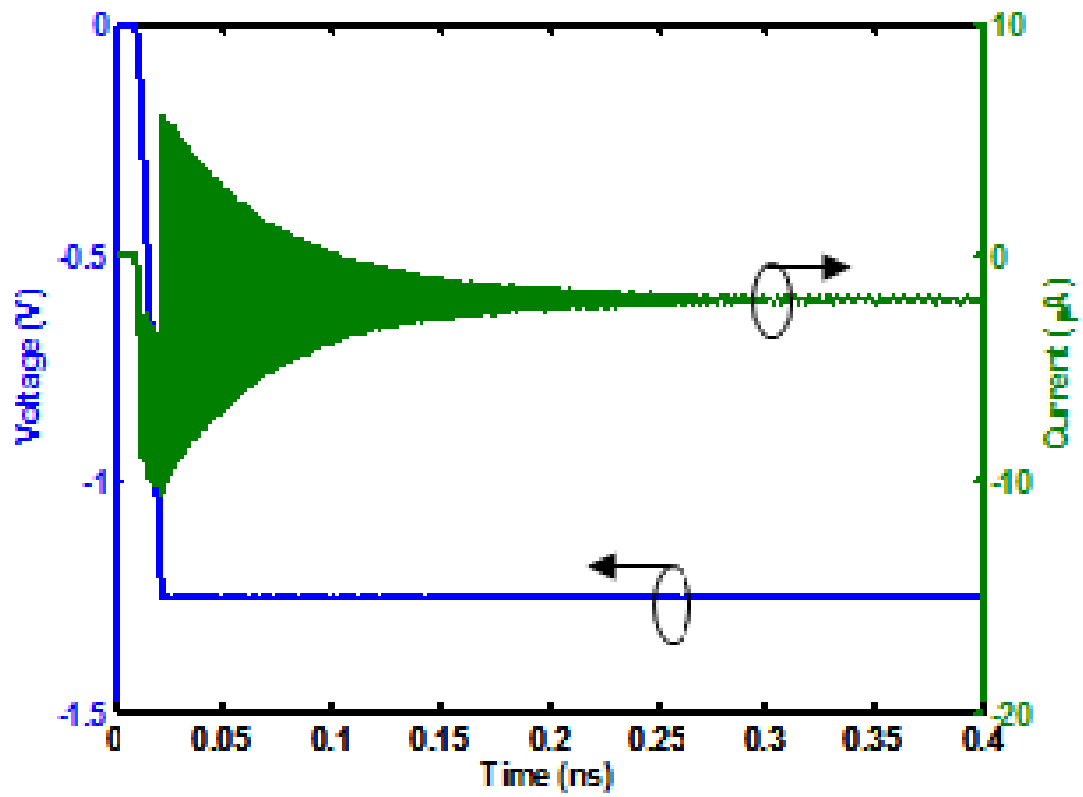


Figure 3.9. Simulated transient characteristics during RESET process. It takes approximately 210 ps for the device to reach steady state for RESET transition.

It is important to note that the component values of $R_{HC}(t) = \rho_{ON} l(t) / A_{fil}$ and $C(t)$ change dynamically with time as their magnitudes depend on the filament length $l(t)$ [see Fig. 3.6]. The subcircuits emulating these components as voltage dependent voltage sources are reported in [61]. The time dependent filament length is incorporated in the simulation by fitting the data points calculated using Eqns. (12) and (17).

The simulated current and voltage profiles for the SET operation are shown in Fig. 3.8 as a function of time. A positive step voltage V_{APPL} is applied by ramping the voltage from 0 to 1.25 V in 11 ps. The transient in current profile is due to the variation of capacitance and resistance as a result of the change in filament length as a function of time. After 10 ms (Fig. 3.6), the high conductivity filaments reach the counter electrode making the tunneling distance zero. With d_{eff} equaling zero, capacitance $C(t)$ approaches a very large value and the voltage drop across it becomes insignificant. At this stage, the device is turned ON and the memristor equivalent circuit contains only R_{LC} and R_{HC} , provided that $C_b = 4.8 \times 10^{-17}$ F is negligible. This is in agreement with the observation of ohmic characteristics of memristors during ON state.

RESET transient is investigated using, $d_{eff}(t) = d - l(t)$, with $l(t)$ being calculated using Eqn. (17). The simulated values of $l(t)$, modeled as a voltage source in Cadence, are plotted in Fig. 3.7 demonstrating excellent agreement with the analytical data. The same equivalent circuit as shown in Fig. 3.8 inset is used to simulate transient characteristics during RESET and the results are shown in Fig. 3.9. It is observed that current transient takes approximately 210 ps to reach 90% of the steady state value during SET and RESET

processes resulting in a switching delay of 210 ps [$0.5 \times (\text{rise time} + \text{fall time})$] or a switching speed of 4.76 Gbit/sec. By increasing the cross sectional area from 50nm×50nm crossbar architecture to 100 nm×100 nm, the switching delay decreases to 20 ps, thereby increasing the switching speed to 50 Gbit/sec. It should be mentioned that the system provides symmetric write/erase times which for the 100nm×100nm memristor equals 20 ps. Switching speed also depends upon material as higher permittivity results in slower switching speeds. As an example using 50nm×50nm SrTiO₃ memristors with a relative permittivity of 310 increases the switching delay to 522 ps or a switching speed of 1.9 Gbits/sec.

3.5 RF Analysis

Memristors have been used in different RF circuits, reconfigurable frequency selective surface (FSS) being an example [62]. An RF model allows the determination of the critical frequency of the RF excitation required for switching. The RF analysis also provides a relationship for a given operating frequency and array size to the material parameters required for a specific $Z_{\text{OFF}}/Z_{\text{ON}}$ ratio. This allows the identification of a material system that will ensure the highest storage density at any specific frequency. The RF analysis proceeds by taking the Laplace transform of the passive circuit elements shown in Fig. 3.8 inset, and exciting the circuit with a sinusoidal source as shown in Fig. 3.10 inset. A simple KVL allows the formulation of the impedance seen by the source:

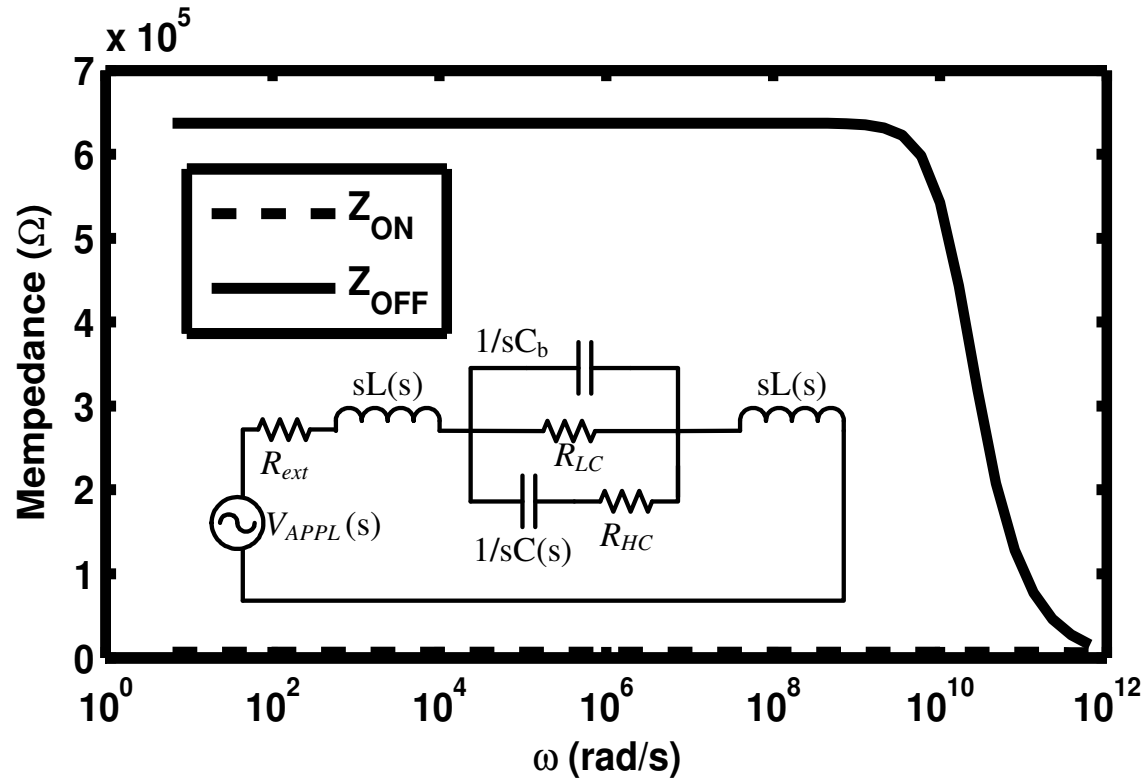


Figure 3.10. Variation of Z_{ON} and Z_{OFF} as a function of frequency. Z_{OFF} has a high frequency negative dispersion region. This phenomenon limits the READ/WRITE speed of RRAM employing memristors. Inset: RF equivalent circuit for memristors.

$$M(s) = R_{ext}(s) + 2sL(s) + \frac{1}{\left[C_b(s) + \frac{1}{sR_{HC}(s) + 1/C(s)} \right] s + \frac{1}{R_{LC}(s)}} \quad (19)$$

where, $M(s)=V_g(s)/I(s)$ is the impedance of the memristor or **mempedance** of the device.

During the ON state of the device, tunneling distance is zero, $C(s)$ approaches infinity ($s=j\omega>0$), and equation (19) reduces to the ON state impedance,

$$Z_{ON}(s) = R_{ext}(s) + 2sL(s) + \frac{1}{sC_b(s) + \frac{1}{R_{HC}(s)} + \frac{1}{R_{LC}(s)}} \quad (20)$$

On the other hand, during the OFF state, $l(t)$ is 0 nm, R_{HC} approaches 0 Ω , and the values of $C(s)$ approaches that of $C_b(s)$. Expression for mempedance during OFF state, Z_{OFF} , thus has a $2C_b$ term and no R_{HC} term.

Variation of Z_{ON} and Z_{OFF} as a function of frequency is plotted in Fig. 3.10, assuming $R_{ext}=15 \text{ } \Omega$, $L=1 \text{ nH}$, $C_b=4.8 \times 10^{-17} \text{ F}$, $R_{HC}=6.37 \text{ k}\Omega$, and $R_{LC}=637 \text{ k}\Omega$. As frequency increases from 1 Hz (6.28 rad/s) to THz, the variation of Z_{ON} is minimal, however, Z_{OFF} clearly experiences a negative dispersion at frequencies higher than 2 GHz. An explanation may be provided by re-writing Z_{ON} and Z_{OFF} in the following forms:

$$Z_{ON} = R_{ext} + \frac{R_{HC} \parallel R_{LC}}{1 + (R_{HC} \parallel R_{LC})^2 \omega^2 C_b^2} + j \left[2\omega L - \frac{\omega C_b}{(1/R_{HC} + 1/R_{LC})^2 + \omega^2 C_b^2} \right]$$

$$Z_{OFF} = R_{ext} + \frac{1}{1/R_{LC} + 4R_{LC}\omega^2 C_b^2} + j \left[2\omega L - \frac{2\omega C_b}{1/R_{LC}^2 + 4\omega^2 C_b^2} \right]$$

A very small C_b makes the imaginary components insignificant in the frequency range of interest. The denominator of the second term in Z_{OFF} is dominated by $1/R_{LC}$ at lower frequencies while the capacitive term dictates for frequencies greater than $=1/(4\pi R_{LC} C_b) = 2.6 \text{ GHz}$ when both the resistive and capacitive terms make equal contributions. The dominance of the capacitive term beyond 2.6 GHz results in the observed frequency dispersion. Low frequency Z_{ON} behavior is dominated by the resistance of the high conductivity filaments, R_{HC} , which being orders of magnitude lower than R_{LC} accounts for its small value. For frequencies greater than

$$f \geq \frac{1}{2\pi C_b R_{HC}} = 60 \text{ GHz}, \text{ where } \omega C_b \times R_{HC} \parallel R_{LC} \geq 1 \text{ the capacitive term dominates and}$$

frequency dispersion is observed. Detrimental effect of high frequency dispersion include increased bit error rate, high leakage current, reduction in the voltage excursion, and dynamical instability to reach the dc characteristics. Amsinck *et al.* reported that a minimum Z_{OFF}/Z_{ON} ratio of 43 must be maintained for a 512×512 array memory to operate [63]. Our calculation (Fig. 3.10) suggests that the ratio Z_{OFF}/Z_{ON} reduces from 100 at 300 MHz to 43 at 7.5 GHz making it unusable beyond this frequency. Depending on material combinations, memristors may reach this dispersion limit $Z_{OFF}/Z_{ON} < 43$, at frequencies lower than the theoretically predicted value owing to a high trap density and other growth and fabrication related defects. By suitably modifying the geometry or material combinations, the maximum allowable frequency can be pushed to a higher

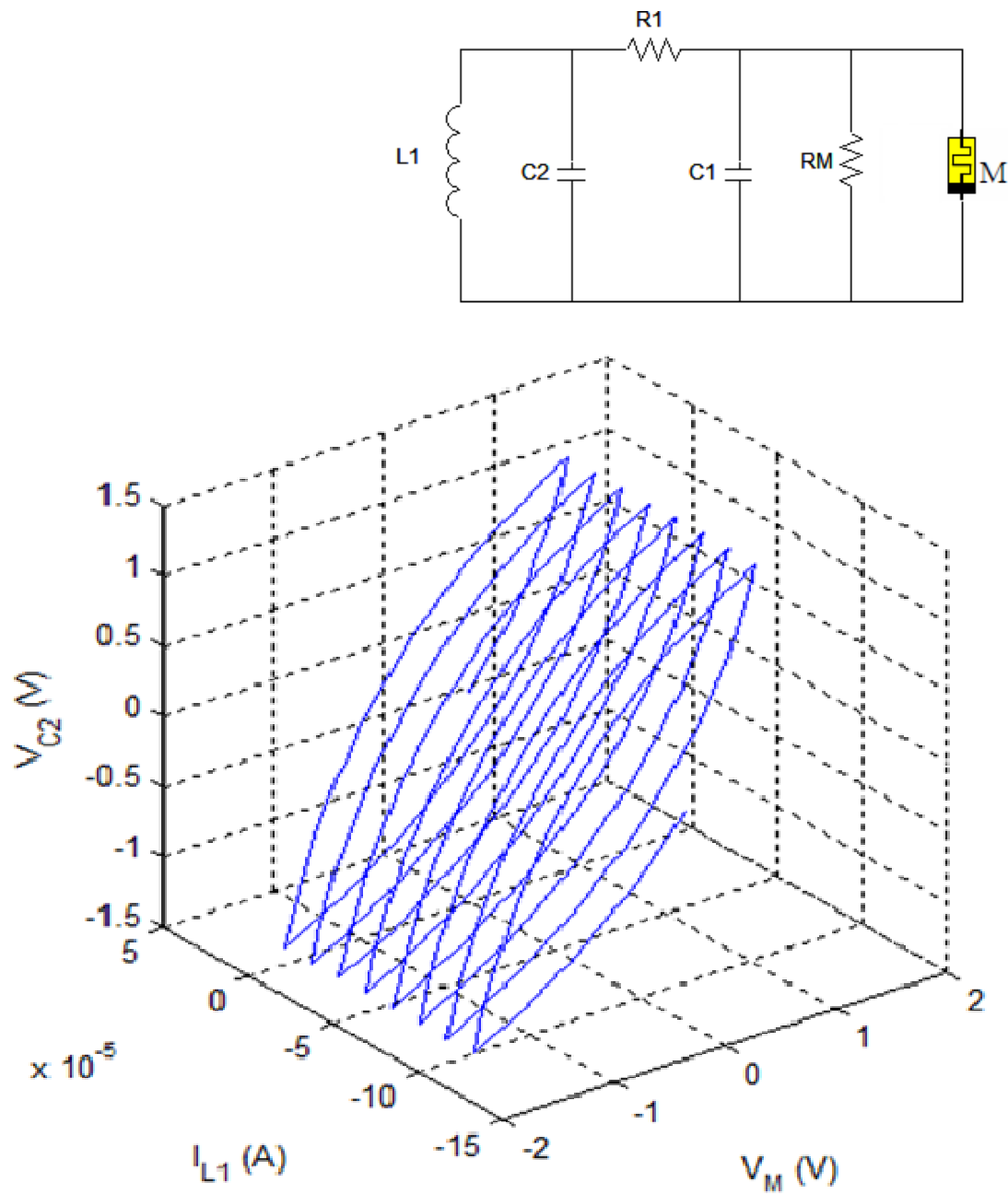


Figure 3.11. Simulation results of Chua's chaotic circuit employing memristor for 8 periods. The circuit demonstrates perfect chaos theory. Inset: Chua's chaotic circuit with memristor. Negative value of RM is realized using an opamp.

value. Increasing the device cross-sectional area from 50nm×50nm to 100nm×100 nm increases the maximum allowable frequency from 7.5 GHz to 12 GHz. On the other hand, a higher permittivity material such as $SrTiO_3$ decreases f_{max} to 3.25 MHz, which would decrease even further if doped with Nb [22].

3.6 Application Circuit

The proposed circuit is used to simulate the *chaotic* circuit postulated by Chua [64], as shown in the inset of Fig. 3.11, demonstrating the effectiveness of the proposed circuit model. Chaotic circuits employing memristors are perfect examples of chaos theory and can be used to modulate the intelligence signal in various defense communication systems. Altman [65] demonstrated the use of these circuits for trajectory recognition. These simplistic circuits can be used to study all the bifurcation sequences for non-linear circuits reported to date. The values of the components are set to $L_1=143$ H, $C_2=1$ mF, $R_1=1$ Ω , $C_1=0.111$ mF, and $R_M = -0.667$ Ω . The negative resistance is accomplished by using an operational amplifier in negative resistance converter mode with an input voltage source of $V_{APPL} = \sin(10^6 \pi)$. The simulated result is shown for eight periods in Fig. 3.11.

3.7 Conclusion

The dynamical characteristics of memristors are derived analytically for ON and OFF state transitions. DC, transient, and RF circuit representations are developed based on the

derived relationships and simulated in Cadence using HSPICE simulator. It is determined that a 50 nm TiO_2 based memristor would require 120 ps for a state transition which would impose a limit on the READ/ WRITE speed. Above a frequency of 7.5 GHz, the ratio of OFF and ON state mempedance collapses to 43 making it dysfunctional as RRAM in a 512×512 array. The limit on the maximum allowable frequency can be circumvented by having a larger cross sectional area device, or lower permittivity material.

Chapter 4 : Fabrication of ZnO Memristors and Experimental Measurement of Switching Performance

4.1 Introduction

According to the 2010 ITRS work group meeting, resistance random access memory (RRAM) has the potential to replace DRAM, SRAM, and NAND flash memory as the next generation non-volatile memory (NVM) [4]. Different technology platforms have been demonstrated to function as RRAM, such as transition metal oxides [66], perovskite oxides [67], and chalcogenide materials [68] to name a few. Watanabe *et al.* [67] demonstrated RRAMs using perovskite oxide SrTiO_3 doped with Cr with a $R_{\text{OFF}}/R_{\text{ON}}$ ratio of 10 ($R_{\text{ON}}=200\Omega$, $R_{\text{OFF}}=2\text{k}\Omega$). R_{OFF} and R_{ON} are defined as the resistances of the high resistance state (HRS) and low resistance state (LRS) of the device, respectively. The perovskite material required an electroforming voltage as high as 200 V and long duration pulses of 1 ms for WRITE or ERASE operation, making them slow and power hungry. Oblea *et al.* [68] reported RRAMs employing chalcogenide Ge_2Se_3 and Ag with reduction of both R_{OFF} and R_{ON} with successive DC sweeps. In contrast, binary metal oxides have drawn considerable interests in recent years due to their faster switching capabilities, higher storage density, simple composition, easy fabrication process, and high CMOS compatibility [69]. Strukov *et al.* demonstrated RRAM using $\text{Pt/TiO}_2/\text{Pt}$ [2]. Memristor based RRAMs are promising due to a faster write time compared to phase change random access memory (PCRAM), smaller cell structure compared to MRAM

and ultra-high density due to the non-requirement of an access device as for PCRAM [21].

We report for the first time a comprehensive and material dependent analysis of bipolar resistive switching (BRS) transients in memristors that is supported by experimental data obtained from ZnO memristors. The measured DC and transient characteristics of bipolar resistive switching (BRS) observed in ZnO memristors is unlike the frequently reported unipolar resistive switching (URS) observed in ZnO thin films. BRS is preferred over URS due to the requirement of a smaller RESET current that offers greater scalability without causing the material to breakdown due to excessive electric field [70]. Measured R_{OFF}/R_{ON} equaling 684 is obtained and that is the highest ever in any ZnO-based memristor. This letter also provides, the transient model of memristors based upon the underlying physics/chemistry of the filament formation processes, in contrast to the reported empirical fit to experimental data. This permits the extraction of switching delays in scaled down memristors and more importantly allows us to investigate different material systems.

4.2 Memristor Fabrication

Horizontal ZnO nanowires (NWs) were grown on p-Si substrates following a two-step process consisting of (i) single-crystalline ZnO epitaxial layer growth using metalorganic chemical vapor deposition (MOCVD), followed by (ii) controlled hydrothermal synthesis of single-crystalline horizontal ZnO NWs. It is to be noted that unlike the standard

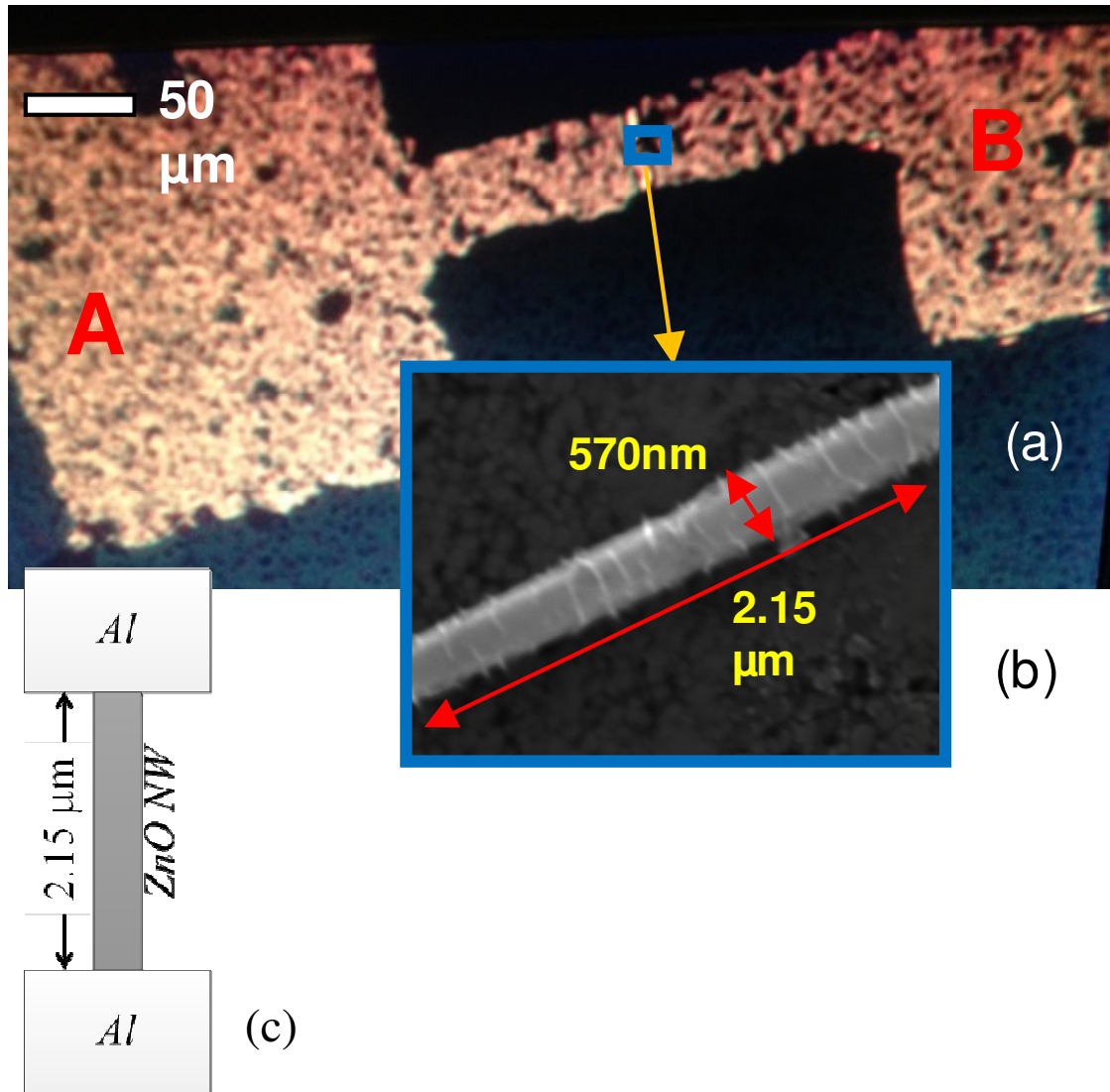


Figure 4.1. (a) Microscopic image of the device fabricated using EBL showing the electrodes. External bias was applied to Electrode A while Electrode B was grounded throughout the measurements. (b) SEM image of the ZnO horizontal nanowire. (c) Schematic of the device cross section

process of growing vertical nanorods (NRs) followed by pick-and-place technique to obtain horizontal nanostructures, the present technology is based upon the direct growth of horizontal nanostructures. Epitaxial growth of ZnO was carried out using MOCVD and follows the method outlined in [71]. Finally, the samples were suspended in a 15 mg $\text{Zn}(\text{NO}_3)_2$ and 35mg HMTA solution in a water bath maintained at 90°C for 18 hours to grow horizontal ZnO NWs.

SEM measurements suggest the NWs to be 2-5 μm long with the diameter varying from 400 nm to 600 nm as shown in Fig. 4.1(b). Electron beam lithography (EBL) was used to pattern contact electrodes on the NWs. Microscopic image of the fabricated device is shown in Fig. 4.1(a). Al contacts with 100 nm thickness were deposited using physical vapor deposition (PVD) technique followed by lift off and annealed at 300°C. Schematic cross-section of the memristor architecture is shown in Fig. 4.1(c).

4.3 DC I-V Characteristics

Fig. 4.2 shows Fig. 2 shows typical I-V characteristics of the fabricated ZnO NW memristor with the signature pinched hysteresis for 9 consecutive voltage sweeps showing uniform and stable switching characteristics with standard deviation of 100 and 215 Ω during LRS and HRS, respectively. At the onset of measurement an external voltage, V_{APPL} , increasing from 0V to 5V with a compliance current of 5 mA, was applied in a single sweep as shown in the bottom inset of Fig. 4.2. V_{APPL} was applied to electrode

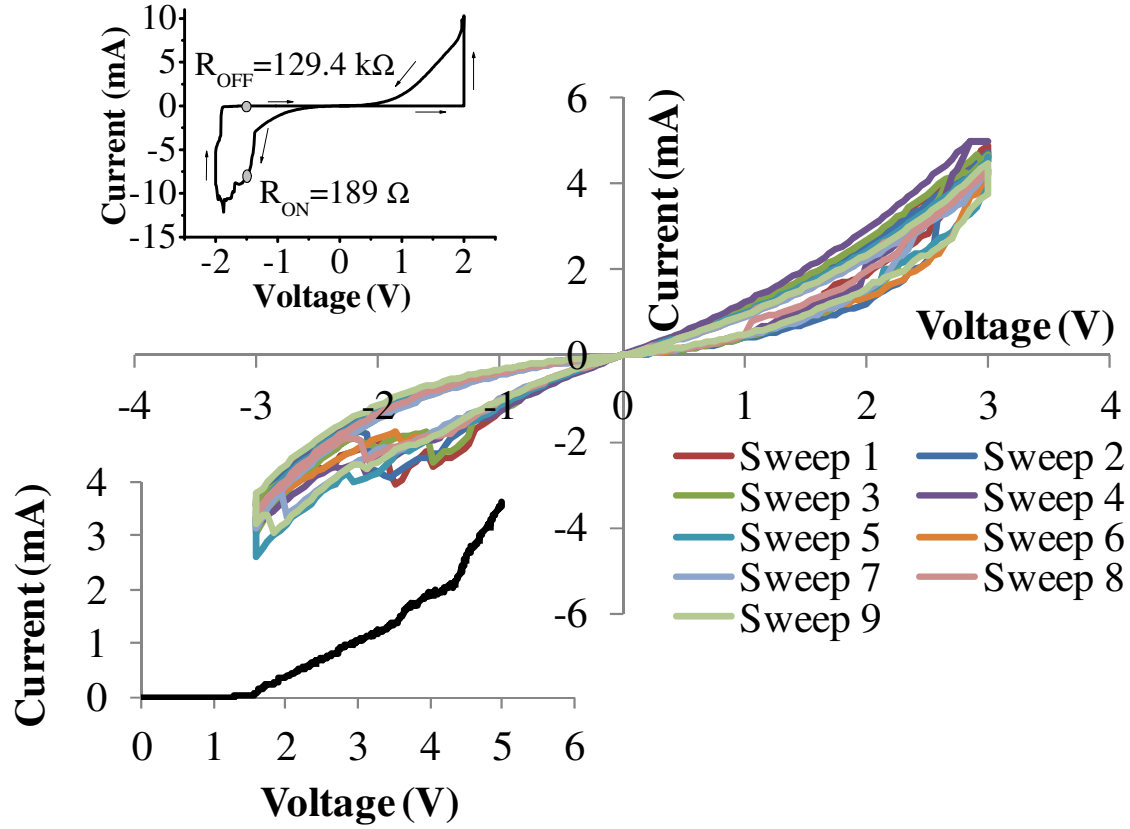


Figure 4.2. I-V characteristic of an Al/ZnO NW (2.15 μm)/Al memristor for 9 consecutive voltage sweeps. Inset (top): I-V characteristics with R_{OFF}/R_{ON} ratio of 684. Inset (bottom): Electroforming of Al/ZnO NW (2.15 μm)/Al memristor.

A with electrode B grounded initiating the electroforming process, thereby, creating low conductivity filaments inside the device. Initial experimental observations on memristors suggest a decrease in electroforming voltage with increasing cross-sectional area. This followed the application of V_{APPL} increasing from 0 to 3V and the switching mechanism is detailed in [16]. Resistances at HRS and LRS are measured to be 129 k Ω and 189 Ω , respectively at a read voltage of -1.5 V. The measured HRS to LRS resistance ratio of 684 is a significant improvement over the ratio of 3 reported by Chang *et al.* for a Pt/ZnO (100 nm thin film)/Pt memristors [72]. Assuming a filament diameter of 45 nm and inter-filament distance of 0.1 μm [24], a cross-sectional area of $2.55 \times 10^{-9} \text{ cm}^2$ can accommodate about 16 high conductivity filaments. Assuming a resistivity of $2.2 \times 10^{-4} \Omega\text{-cm}$ [73] for the high conductivity filaments, the calculated resistance of the LRS is 189 Ω , in exact agreement with the measured value. Assuming a resistivity of $2.2 \times 10^{-2} \Omega\text{-cm}$ [73], resistance of the low conductivity filaments, R_{LC} is calculated to be 350 k Ω and suggests the presence of at least two low conductivity filaments. A higher growth rate of the high conductivity filaments compared to their rupture rates results in remnant filaments inside the device [16]. During the subsequent voltage sweeps electrons tunnel from the tip of the remaining filaments resulting in a lower threshold voltage required to switch from HRS to LRS, which is reflected in the measured I-V characteristics of Fig. 4.2 [16].

4.4 Retention Characteristics

In order to determine retention characteristics of the fabricated memristors, R_{ON} and R_{OFF} were measured under 0.4V read voltage by sweeping the applied bias from 0V to 0.4V

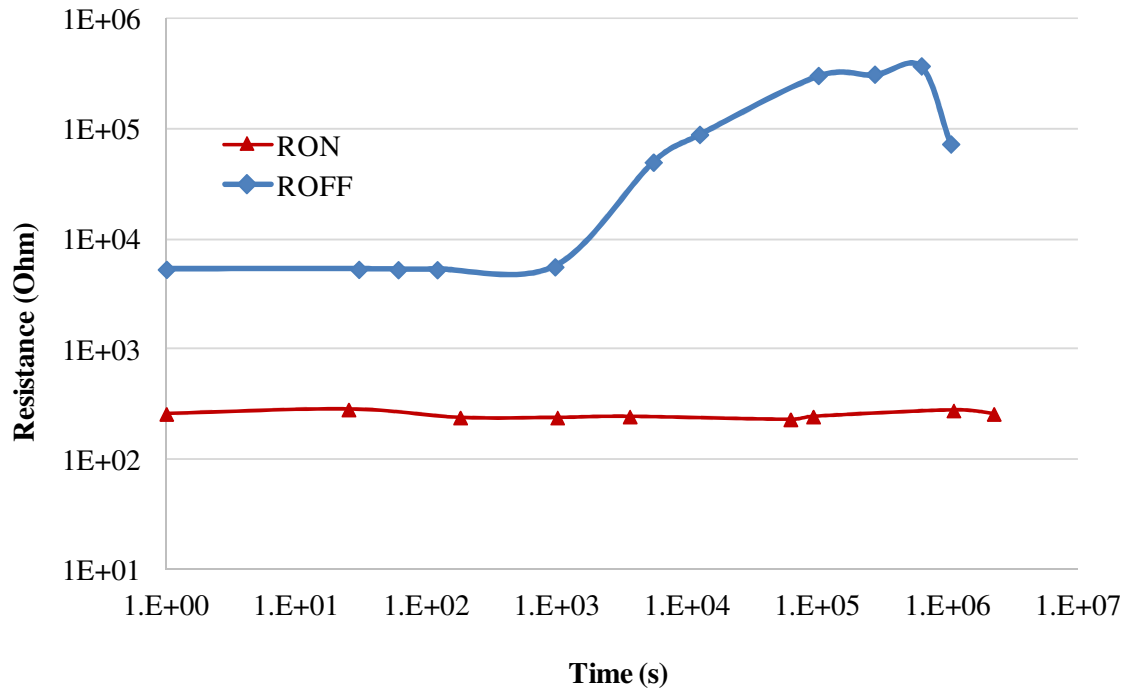


Figure 4.3. Measured retention characteristics of ZnO memristors under 0.4V bias

using HP4145B, as shown in Fig. 4.3. The value of R_{ON} fluctuated between 229 and 281 Ω for a duration up to 2.24×10^6 s at room temperature. R_{OFF} remained at high values with a minimum R_{OFF}/R_{ON} ratio of 23 over a duration of 10^6 sec. The comparatively large variation of the HRS characteristics is attributed to the unregulated temperature and humidity during the measurement extending longer than 10 days. Following these retention tests, the ZnO memristor exhibited reproducible switching characteristics without any performance degradation demonstrating its potential in nonvolatile memory applications. For comparison, Bessonov *et al.* reported state retention of 8×10^3 s for MoO_x/MoS_2 memristors with read voltage of only 10 mV [74]. Wu *et al.* reported retention characteristics up to 12 hours for $Pt/LaAlO_3/SrTiO_3$ memristors under read voltage of 0.2 V [75]. It is to be noted that the electric field assisted vacancy migration and thereupon HRS collapsing to LRS to result in low endurance is expected for high read voltages.

4.5 Effects of Scaling

Fig. 4.4 compares I-V characteristics of $0.5\mu m$ ZnO memristors with different diameters (d). $Ti(20nm)/Al(80nm)$ was deposited as the contact electrode where the Ti layer prevents oxidation of Al. The variation in diameter within a small range does not create any additional filaments and hence does not result in any observable difference in their I-V characteristics. In order to elucidate this point further, current density of different diameter memristors are shown in Fig. 4.5. A careful observation of the current density (J) values suggests that they are very similar for different diameter devices, particularly for the positive bias voltages. For $V_{APPL}=1.5V$, current densities during LRS were 6.4×10^6

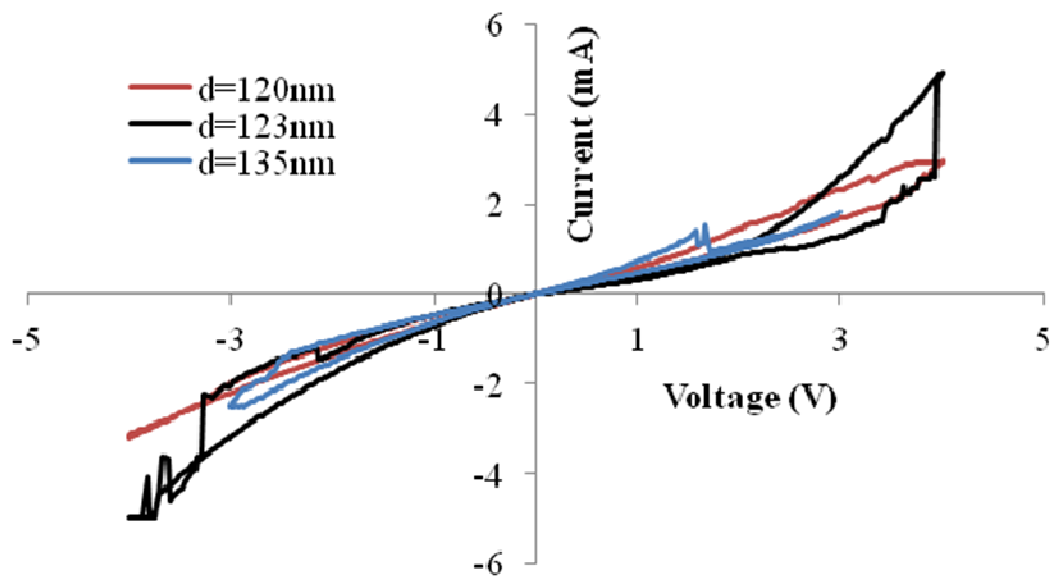


Figure 4.4. I-V characteristics of ZnO memristors with length 0.5 μm and different diameters

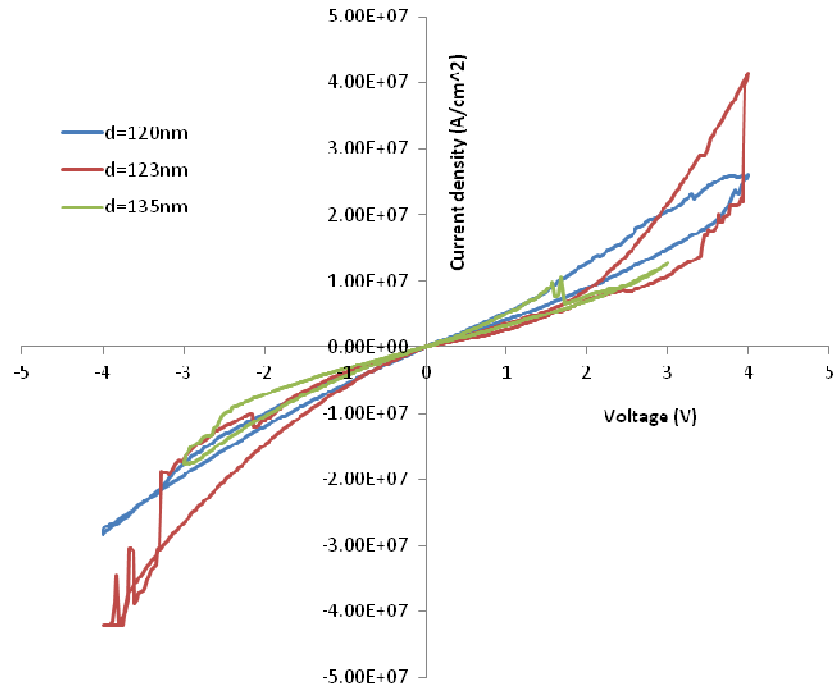


Figure 4.5. Current density of ZnO memristors with length 0.5 μm and different diameters

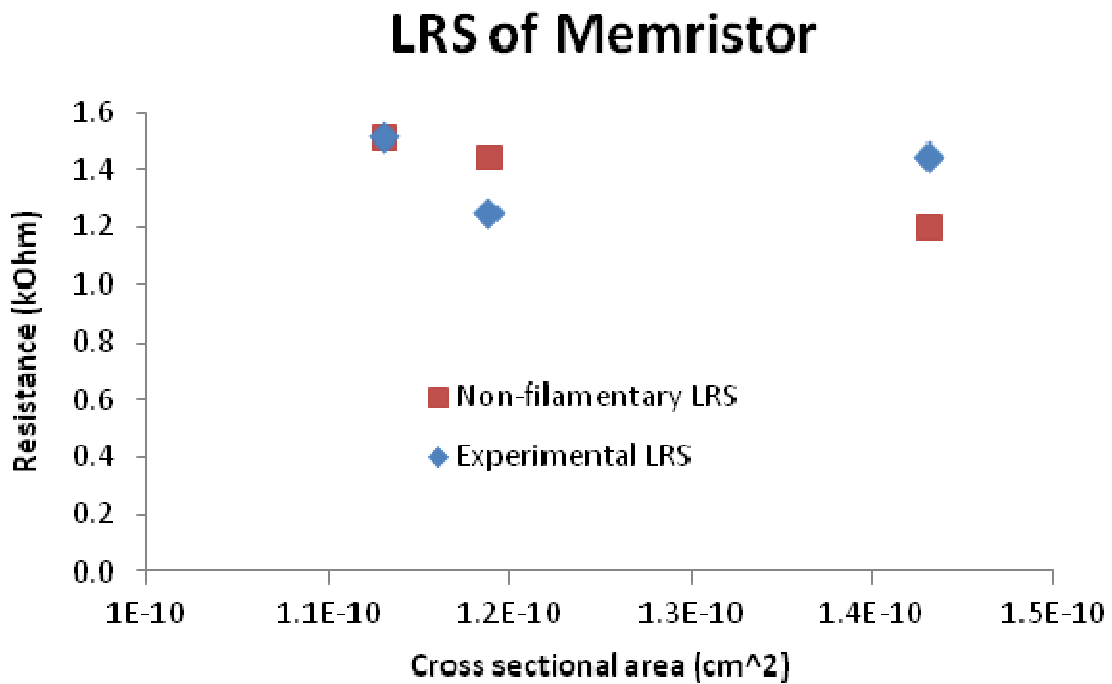


Figure 4.6. LRS of ZnO memristors with length 0.5 μm and different diameters as a function of device cross-sectional area

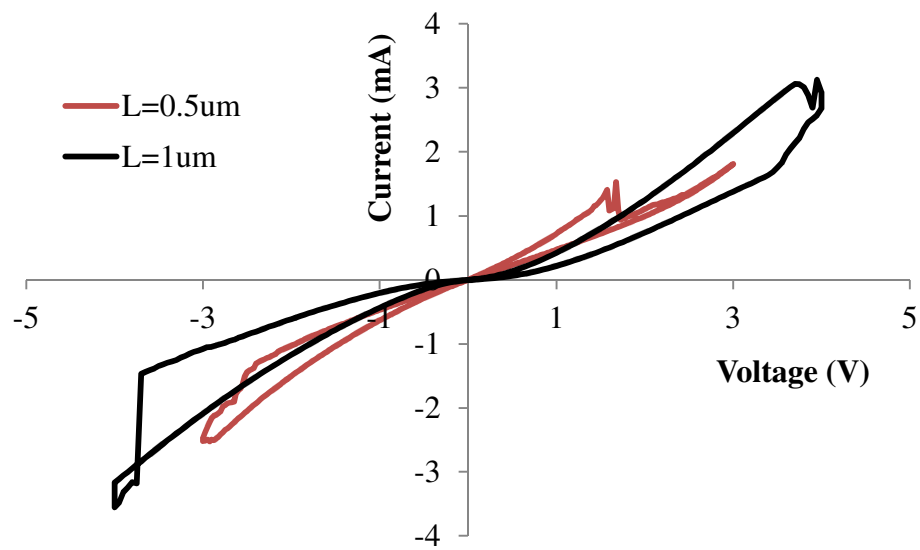


Figure 4.7. I-V characteristics of ZnO memristors of different lengths

A/cm², 4.66×10^6 A/cm², and 5.04×10^6 A/cm², respectively, for $d=120$ nm, 123nm, and 135 nm. During HRS the current densities were 8.42×10^6 A/cm², 5.5×10^6 A/cm², and 8.73×10^6 A/cm², for $d=120$ nm, 123nm, and 135 nm, respectively.

Fig. 4.6 compares measured LRS of memristors with different diameters to investigate whether conduction is due to filament formation or interface-type, with the expectation that non-filamentary conduction will follow a reciprocal cross-sectional area dependence. However, the experimental data do not show such trend and rather appears to have no dependency on device diameter or cross sectional area, suggesting filamentary conduction through the ZnO NWs.

Effects of device lengths (L) on memristor I-V characteristics are shown in Fig. 4.7 for 0.5 μ m and 1 μ m devices. Shorter length devices have lower threshold voltages, as expected, owing to the smaller distance between the electrodes that the filaments have to bridge to switch to LRS. For the same applied bias, both ON and OFF state current magnitudes are higher for shorter memristors that can be attributed to a reduction in resistance ($R \propto L$).

4.6 Measurement of Switching Transients

The measurement setup to extract current switching transients is shown in the inset of Fig. 4.8. Memristors used for transient measurements had a length and diameter of 2 μ m and 300 nm, respectively. A voltage pulse of amplitude 8V and pulse width of 500 μ s was

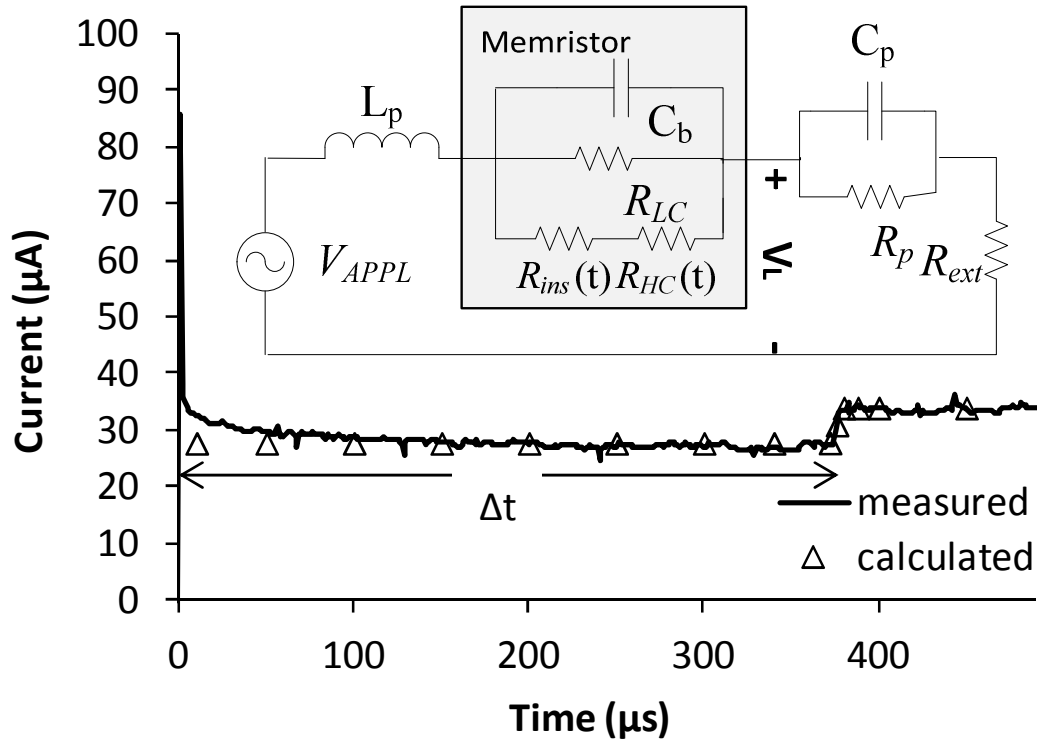


Figure 4.8. Measured and calculated transients during SET switching of ZnO memristors. After a delay time, $\Delta t = 372\mu s$, current through memristor increases with a rise time of $7\mu s$. Inset: transient equivalent circuit of memristor.

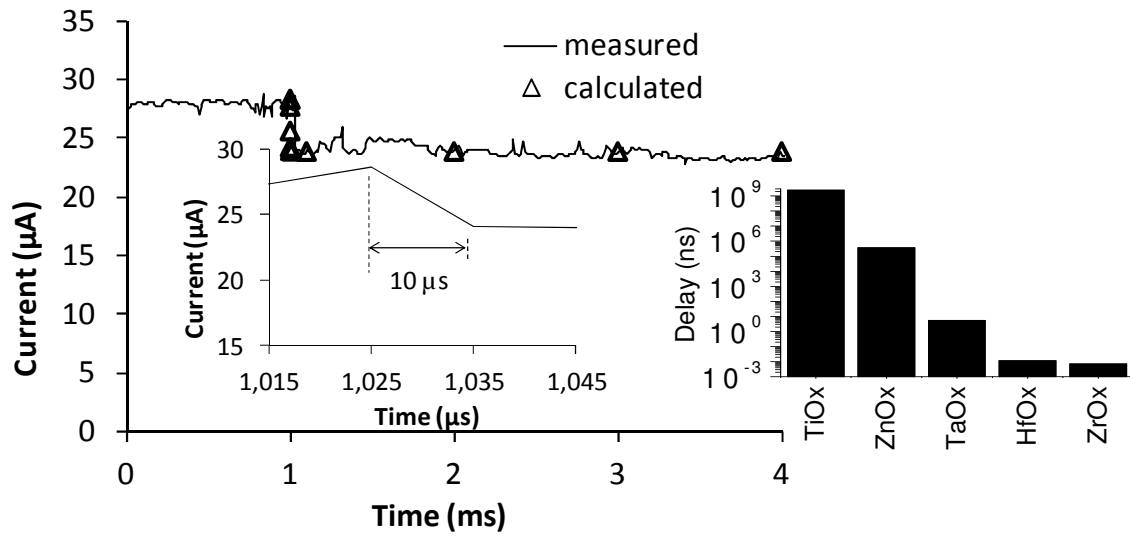


Figure 4.9. Measured and calculated transients during RESET switching of ZnO memristors. Inset 1: zoomed in view during RESET switching suggests smaller than 10 μ s fall time. Inset 2: comparison of switching delays of memristors employing different material system

applied at $t=0$, while the voltage across the load resistance equaling $8\text{ k}\Omega$ was monitored using an Agilent Infiniium 54810A high-speed oscilloscope resulting in $1\text{ }\mu\text{s}$ time resolution at a 8 GSa/s sampling rate. Note, the sampled voltage across the load resistance is a direct measure of the current transient and is shown in Fig. 4.8. R_{HC} and R_{ins} represent the resistance of the high conductivity filaments and the resistance of the insulating material in between the filament and anode, respectively. Both R_{HC} and R_{ins} are time dependent owing to the time dependent change of filament length. Bulk capacitance C_b equals $6.5\times 10^{-19}\text{ F}$ for a dielectric constant of 2.08 for the ZnO NWs. Parasitic resistance due to the cables and contact resistances are lumped in R_p and equals $7\text{ k}\Omega$. C_p and L_p represent the parasitic capacitance and inductance, respectively. Figs. 4.7 and 4.8 show the measured current transients of the memristor as a function of time during SET and RESET transients. Note a delay of approximately $372\text{ }\mu\text{s}$ for the device to switch from OFF to ON state while the actual transition happening only within the final $7\text{ }\mu\text{s}$. The time delay between application of the voltage pulse and the onset of switching transition, Δt , is attributed to attaining a critical tunneling distance ($\sim 10\text{ nm}$) required for the flow of any measurable filament assisted tunneling current. Δt that is correlated to the dynamics of filament formation depends upon both device geometry and the associated material parameters. The determination of Δt requires calculating the time dependent filament lengths and the associated memristance that was carried out using the method described by Mazady *et al.* [76]. The present approach has the advantage of predicting the delay associated with switching, Δt , for different material systems as shown in the inset of Fig. 4.9. The early demonstration of memristive system employing TiO_x shows a switching delay of 2.5 s . The calculation assumes a resistivity of $133\text{ M}\Omega\text{-cm}$ and

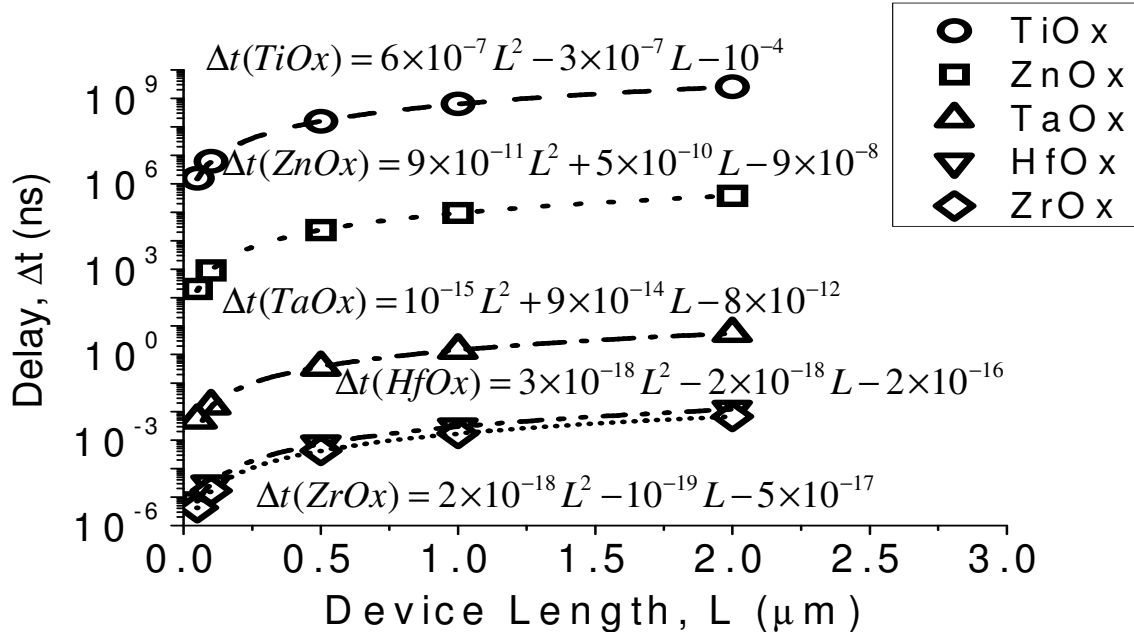


Figure 4.10. Effect of scaling on switching delays of memristors employing different material systems. Switching delays in different materials for different length of the device can be calculated using the equations shown, where L is the device length in nm.

mobility of $10^{-9} \text{ cm}^2/\text{V-s}$ with the device being $2 \text{ }\mu\text{m}$ in length and 300nm in diameter. A lower mobility of TiO_x as compared to that of ZnO ($6.7 \times 10^{-6} \text{ cm}^2/\text{V-s}$) is the primary factor responsible for the delay. For the same dimension, memristors employing TaO_x suggest switching delays of 5.5 ns , assuming resistivity of $39.9 \text{ }\Omega\text{-cm}$ and mobility of $0.47 \text{ cm}^2/\text{V-s}$. Similarly, an HfO_x memristor showed a delay of 11.8 ps , assuming resistivity of $133 \text{ M}\Omega\text{-cm}$ and mobility of $212 \text{ cm}^2/\text{V-s}$. Among the popular material choices for memristors, ZrO_x showed the smallest switching delay of 7.15 ps owing to a very high mobility of $370 \text{ cm}^2/\text{V-s}$ with a resistivity of $1.33 \times 10^{13} \text{ }\Omega\text{-cm}$ of the insulating material. For the measurement of RESET transients the load resistance was $54 \text{ k}\Omega$, the applied voltage had a pulse width of 5 ms and the time resolution of the oscilloscope was $10 \text{ }\mu\text{s}$. The model for RESET transition assumes an additional 1 ms delay which may be attributed to the presence of surplus oxygen vacancies in the vicinity of the filaments that require removal before the filaments start to rupture. The measured fall time of ZnO NW memristor is determined to be smaller than $10 \text{ }\mu\text{s}$, as shown in the inset of Fig. 4.9.

Fig. 4.10 shows the scaling dependence of switching delays for different materials. Memristors of different lengths, namely, 50 nm , 100 nm , 500 nm , $1 \text{ }\mu\text{m}$, and $2 \text{ }\mu\text{m}$, with the diameter fixed at 300 nm , are simulated using the circuit model as shown in the inset of Fig. 4.8, employing the time dependent filament length calculated from [76]. Shrinking the device length from $2 \text{ }\mu\text{m}$ to 50 nm results in 3-4 orders of reduction in the delay of a typical memristor. Required delay for switching, Δt , for different lengths of the device, L , and different materials can be estimated using the relationships shown in Fig. 4.10, obtained using a regression analysis of the data. It is important to note that scaling the

device alone may not be sufficient to achieve the desired switching performance for a given material system. For example, a 2 μm TaO_x memristor has a delay of 5.6 ns while scaling a ZnO memristor to 50 nm results in a longer delay of 200 ns. Power dissipation during SET and RESET switching is measured to be 261 and 155 μW , respectively, which are significantly better than the reported values for CuMoO_x based RRAMs [77]. Based upon measured data the estimated switching energy and slew rate are 83 nJ and 0.02 V/ μs , respectively, during SET switching. During RESET the switching energy and slew rate are 238 nJ and 6.21×10^{-3} V/ μs , respectively.

4.7 Conclusion

We report the first measured transient performance of ZnO NW memristors during BRS. The DC characteristics reported here shows uniform and stable BRS behavior with a $R_{\text{OFF}}/R_{\text{ON}}$ ratio as high as 684. Effects of device length and cross-sectional area on memristor I-V characteristics are shown experimentally that confirms filamentary conduction mechanism of ZnO memristors. The measured transient performance are in good agreement with the physics based model. Switching delays of memristors employing different material platforms are compared and effect of scaling is predicted. Crucial performance indices for RRAMs such as delay time, switching power, slew rates, and switching energy are reported.

Chapter 5 : Memristor Nano-PUF

5.1 Introduction

Physical unclonable functions (PUFs) [78] were introduced a decade ago and have emerged as a popular hardware security primitive. PUFs are circuits that extract a unique signature or code specific to the underlying hardware. Specifically, a PUF maps challenges to unique responses in physical structures such as integrated circuits (ICs) based on intrinsic, uncontrollable and reproducible characteristics. PUFs exploit some intrinsic attributes of the gates, such as process variability induced gate length variations, into tangible bits of information unique to that device. These bits of information can be used in different type of security protocols, such as unique identifiers, secret keys, public keys, authentications, IP protection, IC piracy, remote activation, and pseudo random bit generators [79-89].

PUFs represent a powerful alternative to traditional approaches that rely on permanent storage of secret keys/IDs in nonvolatile memory (NVM). First, a PUF's secret is not explicitly stored. Rather the signature is part of the device itself and may be re-generated only when necessary. Since PUFs can only generate output when powered, PUF is not as vulnerable to many of the physical attacks possible on NVM [90]. In addition, a system containing a PUF does not require non-NVM to store secret keys, resulting in simpler fabrication and making it lower cost [90]. Finally, since the secret key/ signature is generated based on uncontrollable and unpredictable variations of device parameters from manufacturing, PUFs are generally considered as unclonable.

Different PUF realizations have been reported in literature over the past decade. Silicon (CMOS) PUFs include ring oscillator based PUF (RO-PUF), Arbiter based PUF, SRAM-based PUF, Sense-amplifier based PUF, Butterfly PUF, Flash PUF, etc. [79-89, 91, 92]. Different types of PUFs exploit different physical entities, including leakage, delay, start-up characteristics, among others, to provide randomness in their outputs. SRAM-PUF exploits the start-up state of SRAM cells when the output is unpredictable because of intrinsic and uncontrollable variations of individual gates. The cross-coupled inverters in an SRAM cell race each other, generating a logic '0' by one inverter while logic '1' by the other. As which inverter will generate logic '1' and which one logic '0' is unknown (and dependent on process variations), the combination can be used as PUF. In the RO-based PUFs, frequencies of symmetric ROs are compared to produce '1'/'0's. Signals are passed through two symmetric paths in Arbiter PUF and due to process variation induced delay difference, the path which is fastest is random. Thus, the outcome of the race can be used to generate a random '1' or '0'.

CMOS PUFs have been traditionally used for hardware security and authentication. Unfortunately, models of CMOS devices are comparatively simpler and are easier to simulate, making them prone to certain machine learning and modeling attacks [93]. It is critically important that a PUF be difficult and time consuming to model by an attacker who does not physically possess the electronic device containing the PUF. This ensures that the attacker is unable to predict the PUF response for a given challenge. However, since PUFs do not add any functionality to the host device itself, it is rather important that the PUFs also be lightweight, cost efficient, and resource constrained [93]. As an

example PUFs should not occupy a significant portion of the die area and should consume very limited power without affecting the device performance.

PUFs suffer from lower reproducibility due to their sensitivity to noise, ambient, and aging [84, 94-98]. The noise margin depends on the difference in strengths between two SRAM cells, ROs, symmetric paths, etc. which solely depends on process variation. Larger non-deterministic variations between two symmetric units are better for a reliable and uniform PUF. The impact of noise may cause a different response for the same applied challenge in a PUF and make the application of PUF ineffective. The encoded bits of information employing the race condition between two symmetric units in PUF are known as the “key” which authenticates the user. Some cryptographic applications can tolerate certain amounts of errors while others must have error free keys. For stable and error free operation, PUFs may require post-processing techniques such as error correcting code (ECC) and different enrollment schemes [94, 99-105]. In ECC, a syndrome is generated from the enrolled PUF response and stored in memory or database to correct the key when it is re-generated in future. PUF collects the noisy response and corrects the responses with the help of this syndrome. Unfortunately, error correction using syndrome leaks some portion of the secret key or authentication bits. The ECC schemes are also costly and slow down the key generation from a PUF [100]. Besides being reliable, PUF outputs must be uniformly distributed and have sufficient entropy to be used directly in cryptographic applications [94, 99-105]. Fuzzy extractors are commonly used in PUFs to address these two concerns. It has been reported in [79] that the fuzzy extractor can be attacked using side channel information. For example,

Karakoyunlu *et al.* demonstrated hacking of PUF keys using Simple Power Analysis (SPA) technique [100]. In SPA technique power consumption of PUF is directly measured by inserting a small $\sim 50 \Omega$ resistor in series with the power or ground terminals. Semi-invasive and invasive attacks on SRAM-PUF have been reported in [104]. Cloning of SRAM-PUF has been reported using remanence decay of SRAM cells in [105]. Modeling attacks have been reported in [103], where the authors used various machine learning techniques to model challenge-response pairs for different strong PUFs. Enrollment algorithms and key extraction techniques are also proposed in the literature, most of which result in excessive and impractical overheads.

Memristor, leveraging nanotechnology fabrication process, poses itself as an interesting alternative to the existing PUF realizations in CMOS. The concept of memristor was first hypothesized by Chua in 1970 based upon symmetry arguments in the fundamental circuit elements (resistance, capacitance, and inductance) and circuit variables (voltage, current, charge, flux) matrix [1]. The symmetry argument demands for a relationship to exist between the magnetic flux and electric charge, dictated by memristor, similar to the relationship between voltages and currents that defines resistance. In that sense, memristor is deemed as the fourth fundamental circuit element. The governing mathematical relations of memristors suggest that the resistance of memristor depends upon the past history of current flow through the device, which is the electric charge. A renewed interest in memristors emerged with Strukov *et al.* reporting pinched hysteresis in the I-V characteristic, which is a signature of memristors, of a Pt/TiO₂/Pt two-terminal device in the absence of any applied magnetic field [2]. Memristors, being merely an

architecture consisting of an oxide layer sandwiched between two electrodes, can be scaled beyond the CMOS technology. As a consequence of such scalability, a larger number of memristors can be fabricated in the same die area required for a CMOS device. CMOS compatibility of memristors has been demonstrated by Borghetti *et al.* by fabricating TiO_2 memristor crossbar devices alongside Si MOSFETs on the same substrate [106].

Process variation dependent switching delays of memristors can be leveraged to randomize the outputs of PUFs making it very difficult, if not impossible, to be hacked by an attacker. It is to be noted that, in nanoscale device manufacturing, the same process variation induces more significant change in device attributes. The carrier transport dynamics in memristors is highly dependent on the length of the device and even a 10 nm process variation can introduce 130% mismatch in the switching delays for a 50 nm HfO_x memristor [107]. For comparison, with the same process variation, 2 μm HfO_x memristors show 11% mismatch in their switching delay characteristics. While race conditions between two gates have traditionally been exploited for the fabrication of PUFs, variability in device dimensions of a single memristor will suffice for fabricating memristor based PUFs. Moreover, the high non-linearity of memristor transport characteristics requires their circuit models to be complex. Complexity of the memristor model is further amplified by the fact that it is the fourth fundamental circuit element and cannot be represented by any combination of the other passive circuit elements such as, resistance, capacitance, and inductance.

The models of memristors that can be found in the literature are broadly classified into two categories: (i) behavioral and (ii) physics based models. Of the two established modeling techniques, behavioral models provide an overview of the expected characteristics but fail to provide an insight into the effects of various device parameters, variation of which will arise from the process variations. A circuit model based upon the underlying physics of the device, on the other hand, allows accurate estimation of the simulation time critical for time bounded authentication. Impact of the physical structures and bias conditions (example – scaling of device dimensions, temperature, material etc.) of memristor can be incorporated into the model for a true representation of the actual device. In this chapter, we provide two major contributions. First, we propose a physics based model to compute the memristance and demonstrate that the built-in complexity, due to the different physical processes and parameter variations, require an extensively long period of time for an attacker to simulate the function making it an excellent security primitive. Second, we provide the first experimental demonstration of a memristor nano-PUF, using memristors fabricated using ZnO-nanowires. Of our 6 memristor nano-PUFs, three 1-bit outputs were logic ‘1’ and three were logic ‘0.’ Albeit a small sample size, this corresponds to a uniform distribution. Furthermore, upon repeated experimentation, the same 1-bit output was generated by the PUFs; thus also demonstrating the reproducibility of the memristor nano-PUF.

5.2 Design of Memristor Arrays as PUFs

The governing equations of a memristive system, shown in Fig. 5.1, can be written as follows:

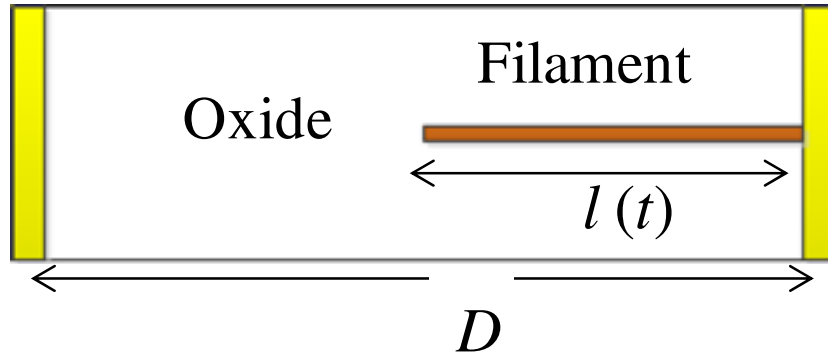


Figure 5.1. Schematic of a typical memristive system

$$v(t) = \left[R_{ON} \frac{l(t)}{D} + R_{OFF} \left(1 - \frac{l(t)}{D} \right) \right] i(t) \quad (1)$$

$$v_{drift} = \frac{dl(t)}{dt} = \mu_v \frac{R_{ON}}{D} i(t) \quad (2)$$

where $v(t)$ and $i(t)$ are the voltage across and current through the memristor, respectively, R_{ON} is the resistance of the device when conductive filaments connect both electrodes, R_{OFF} is the resistance of the device when there is no filament inside the device, $l(t)$ is the time dependent length of the filament, D is the total length of the memristor, and μ_v is the mobility of oxygen vacancies. It is to be noted that the present formulation incorporates the appropriate boundary conditions where the highly non-linear drift velocity of oxygen vacancies approaches zero near the electrodes. In contrast, previous formulations accounted for this non-linear drift velocity in an adhoc fashion by incorporating a nonphysical window function in the governing equations of memristors. Assuming, e as the electron charge, $n(x)$ as the concentration of oxygen vacancies, A as the cross sectional area of the device, and J_{diff} as the diffusion component of the total current, the non-linear drift velocity can be expressed as,

$$v_{drift} = \frac{dl}{dt} = \frac{i(t)}{Aen(x)} - \frac{J_{diff}}{en(x)} \quad (3)$$

The total current flowing through memristive system can be given as,

$$i(t) = \left[e\mu_v n(x)E(x) + J_{diff} \right] A \quad (4)$$

with $E(x)$ being the applied electric field.

Integration of Eqn. (3) and substitution in Eqn. (1) yields the appropriate expression for memristance:

$$M(t) = R_{OFF} + (R_{ON} - R_{OFF}) \left[\frac{q(t)}{Aen(x)D} - \frac{J_{diff}t}{en(x)D} \right] \quad (5)$$

As can be seen from Eqn. (5), memristance is affected by thickness of the oxide layer D , cross sectional area of the device A , for a cross bar architecture that equals the product of the width of the top and bottom metal bars, resistivity of the ON and OFF states, accumulated charge carriers, carrier diffusion constant, and time of measurement. Thus the effect of process variation on memristance characteristics is highly nonlinear and can be leveraged in memristor PUFs.

Rajendran *et al.* reported simulation of memristor PUFs using a behavioral model of memristors [93]. The model assumes a linear drift velocity profile of the oxygen vacancies which is a theoretical simplification, requiring the incorporation of a mathematical window function to explain experimental hysteresis observed in memristors. It is to be noted, that the window function tries to emulate the velocity of the oxygen vacancies that approaches zero at the boundaries and is correctly accounted for in the present analysis.

In [93], Rajendran *et al.* utilized the different process variations such as device dimensions, doping concentrations and mobility to demonstrate the extensively long period of time required for an attacker to produce the correct key.

The formulation for memristance used to simulate memristor PUF is an overly simplified representation of the linear drift velocity profile and neglects the effect of ON resistance compared to the OFF state resistance. Consequently, the model has lower degrees of freedom and the simulation results are not representative of an actual device.

Since PUF utilizes each degree of freedom arising from process variation mentioned above, introduction of additional degrees of complexity is generally sought. By fabricating memristors in a 3D architecture, such as crossbar arrays, randomness of the response to a specific challenge can be increased to a greater level by forming different orders of polyominoes. Polyominoes are defined as planar geometric figures that can be formed by joining multiple squares of identical dimensions edge to edge such that they create a polyform with each cell being a square. The concept of polyominoes in the context of memristor crossbar PUF can be understood by the following example. Let us assume X is the authenticator, Y is the person needing authentication to use his device, and Z is the attacker. The authenticator, X, may select a section of the nano-PUF to perform his simulations to authenticate Y. In order to prevent Z from being authenticated the following constraints must be satisfied:

- The number of possible combinations to select the polyomino should be as large as possible. If the number of possible combination is too small Z will be able to simulate all of those conditions apriori and will have the correct key.
- However, the size of the polyomino should not be so large that X cannot simulate and obtain the correct response in real time.

- At least one set of the outputs must be a common for both X and Y so that X can verify Y's outputs. This can be ensured by selecting polyominoes that has at least one cell lying at the edge of the crossbar.

As an example, the inset of Fig. 5.2 shows 6 different ways tetra-ominoes may be selected from a 8×8 memristor crossbar [93]. By increasing the array size of the crossbar architecture or by arbitrary selection of polyominoes shapes and sizes while authenticating a user, security of the PUF-based authentication system can be greatly enhanced. For instance, a smaller sub-section in the form of polyomino shapes may be selected randomly from the total N×N array for authentication. The number of possible polyomino shapes that can be constructed with M cells is given by $\frac{c\lambda^M}{M}$ and plotted in logarithmic scale in Fig. 5.2 as a function of M, where $c = 0.3169$ and $\lambda = 4.0626$ [93, 108]. The possible number of polyomino in a N×N array is given by $\frac{c\lambda^M}{M} \times N$. Total time required to simulate polyominoes of size M implemented using TiO₂ memristors is shown in Fig. 5.3. The quasi-DC circuit model of TiO₂ memristor reported by Mazady and Anwar was used for the simulation and implemented using a desktop computer with Intel Core i7-3770 processor, 4 cores with 2 threads per core, and

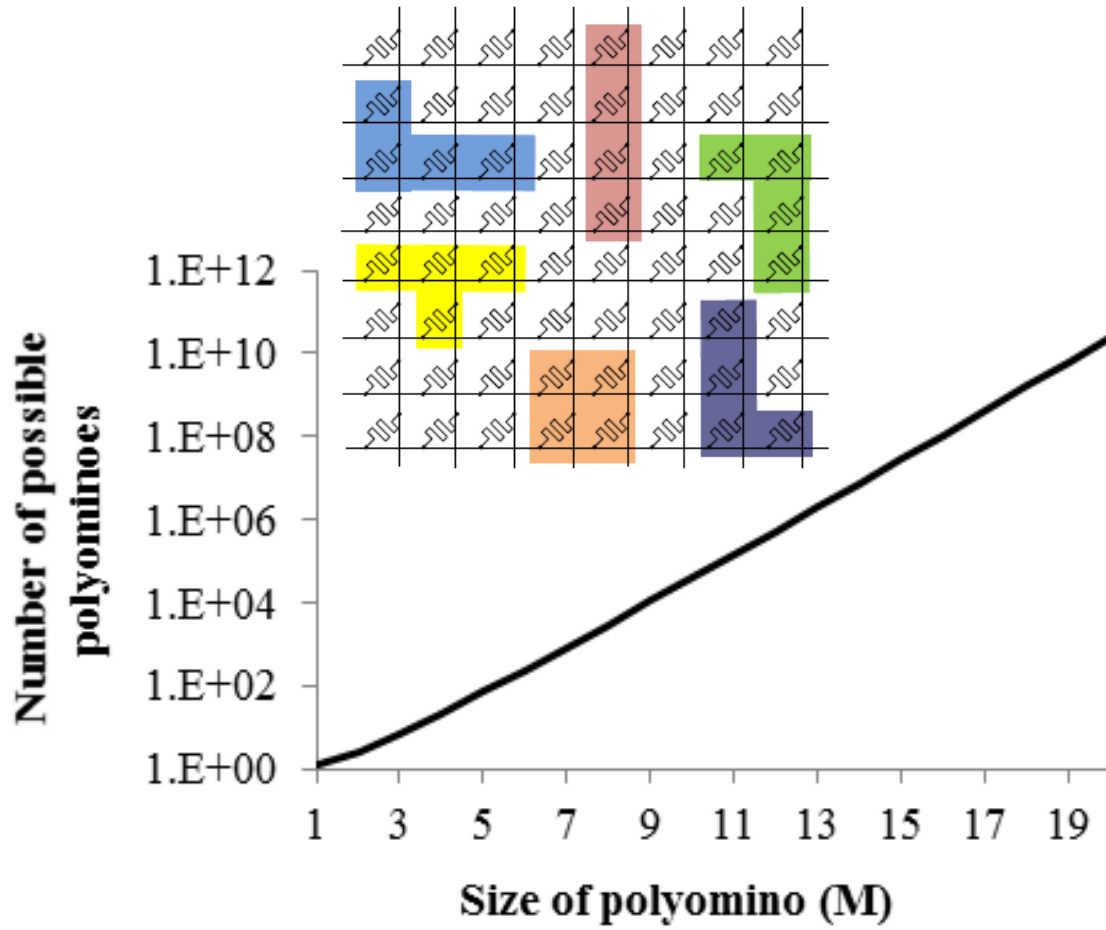


Figure 5.2. Total number of possible polyominoes in logarithmic scale as a function of polyomino size. Inset: six different ways tetra-ominoes may be selected from a 8×8 memristor nano-PUF [93].

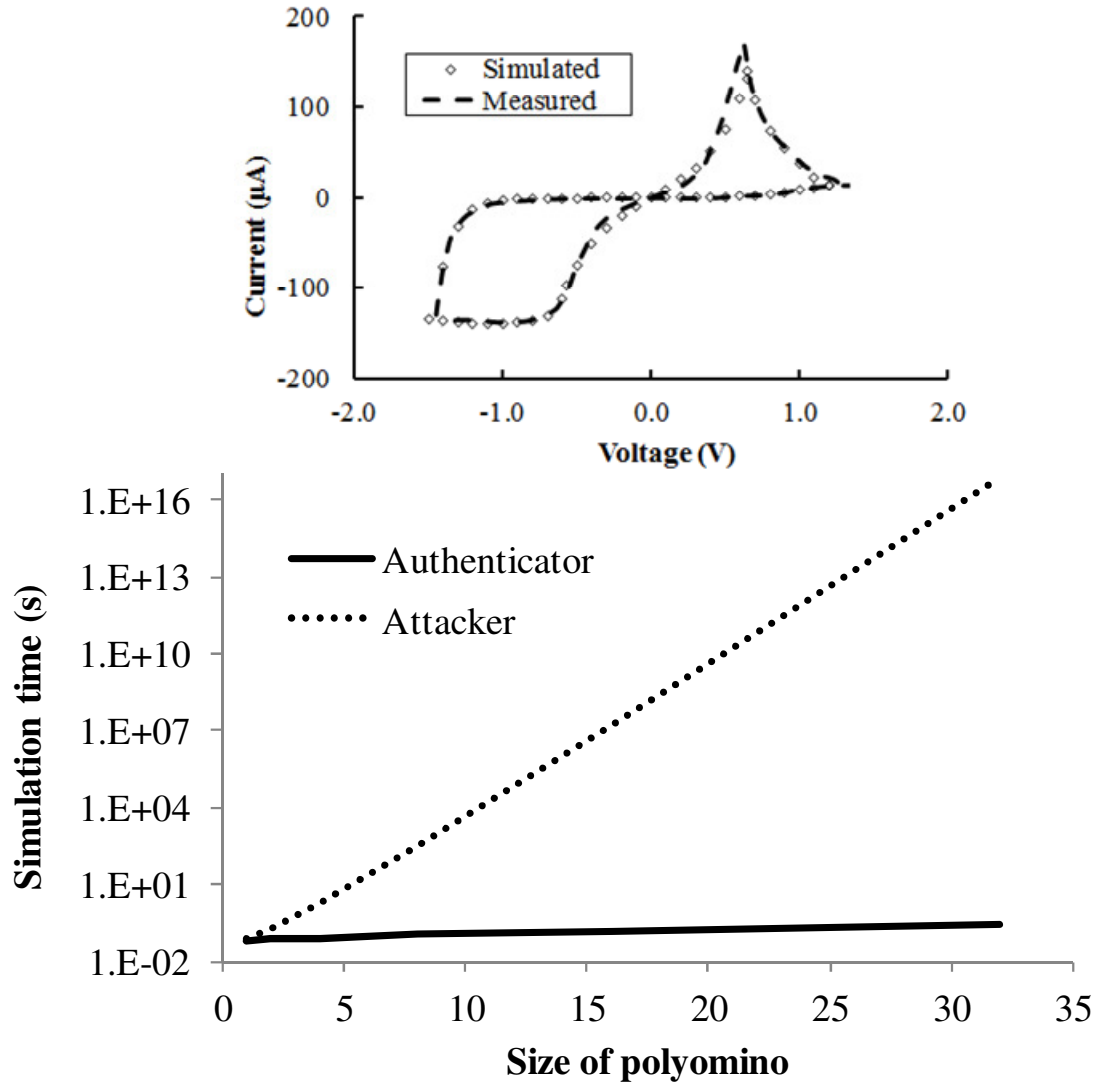


Figure 5.3. Simulation time comparison between an authenticator and an attacker in logarithmic scale as a function of polyomino size. Inset: the excellent agreement between the measured data and simulated data using the circuit model [16, 76].

8 GB RAM. It should be pointed out that the simulated circuit model, based upon the underlying electrochemistry and carrier transport physics of the devices, upon implemented using PSPICE, gives very good correlation with the experimental I-V data, as shown in the inset of Fig. 5.3 [16, 76]. The total simulation time, which is shown in logarithmic scale along Y-axis of Fig. 5.3, for an *authenticator* (or a person who has apriori knowledge of the design) for different size polyominoes is compared with the simulation time of an attacker. With only 32-ominoes, simulation time for an attacker, having the correct simulation model but unaware of the polyominoes selection, is 3×10^{17} times greater than the authenticator. For a time bound authentication protocol, such enormous delay of about 2.5×10^9 years, can be exploited to develop a public PUF, such that the appropriate circuit model is available to the general public but the polyominoes selection is not. The exponential increase of the simulation time for the attacker is attributed to the exponential increase of possible polyominoes as shown in Fig. 5.2. It is to be noted that the present physics based circuit model, providing higher degree of complexity, results in an increase in simulation time by seven order of magnitude for an attacker than that reported by Rajendran *et al.* [93].

5.3 Demonstration of a 1-bit Memristor PUF

The working principle of a single bit memristor PUF as proposed by Rose *et al.* is shown schematically in Fig. 5.4 and the implementation is shown in Fig. 5.5 [109]. $V_{WR} = 2.5$ V and $V_{RD} = 1$ V are the write and read voltages of the memristor and were supplied by a DC voltage source. Depending on the selection bits, the DM74157 multiplexers let one of

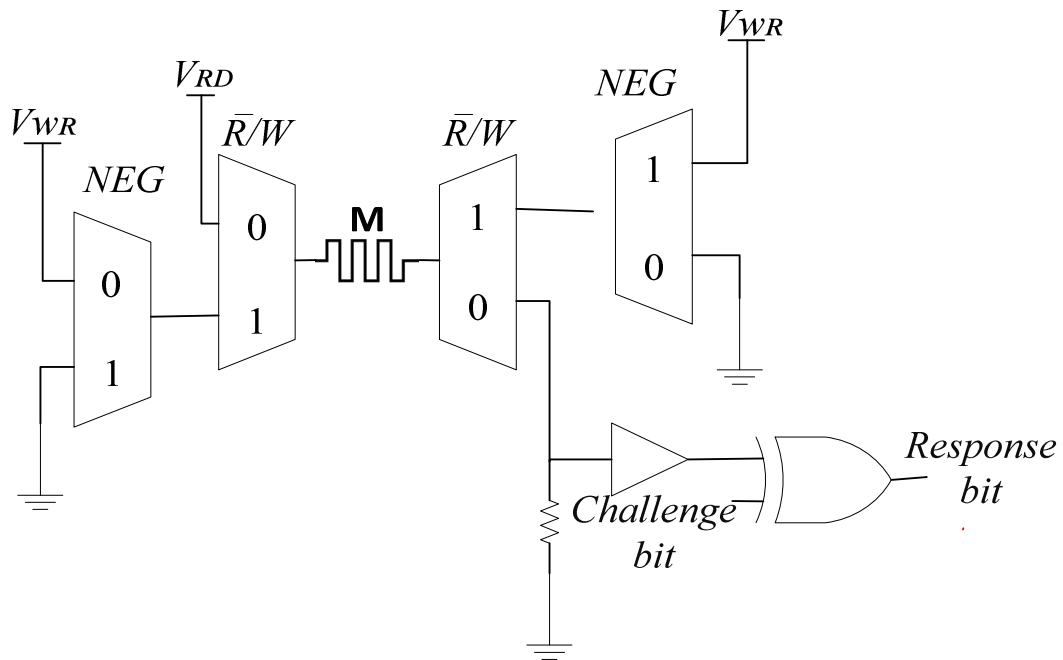


Figure 5.4. Schematic circuit diagram of a 1-bit PUF cell using memristor

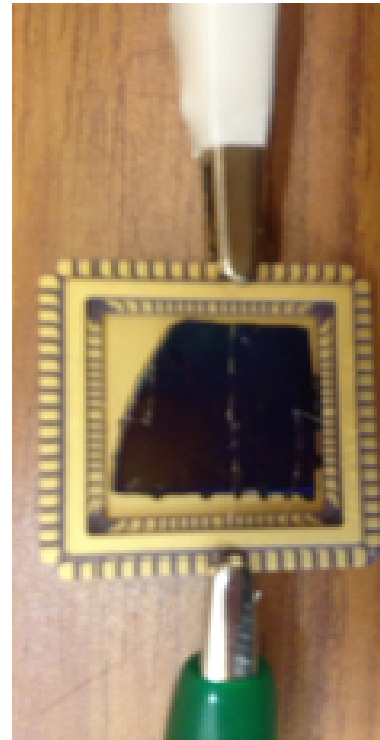
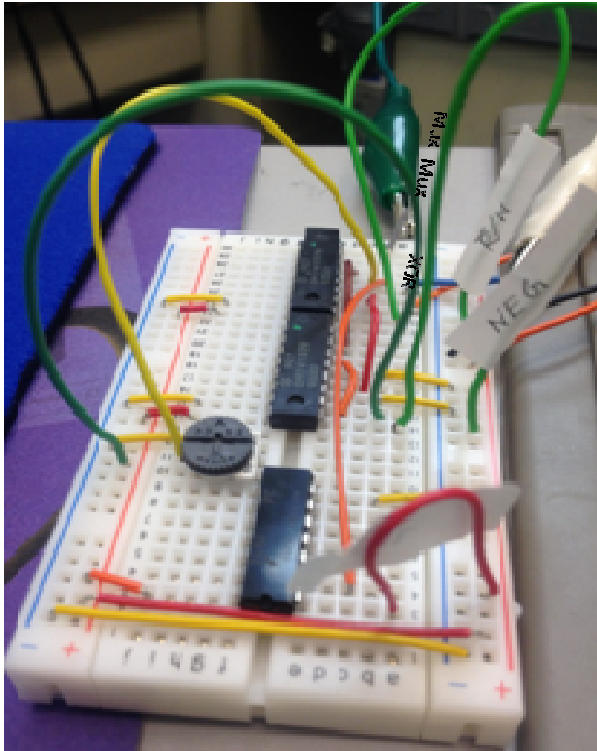


Figure 5.5. Implementation of a 1-bit PUF cell using memristor. (a) circuit implementation, (b) memristors wire bonded on a chip carrier.

Table 5.1. Truth table of a 1-bit PUF cell using memristor

NEG	R_bar/W	Comment
1	1	RESET
0	1	SET (Write time is critical)
X	0	Check Response

the inputs pass to the next node. The \bar{R}/W selection bit determines if the memristor is being read or written. During the write operation of the memristor, the *NEG* selection bit determines if the memristor is being SET ($NEG = 0$) or RESET ($NEG = 1$). The complete truth table for different operations is shown in Table 5.1. It is to be noted that the duration of the \bar{R}/W write selection bit during the SET operation is critical for successful PUF operation. The duration of the applied SET pulse was 375 μs to account for the switching delay and rise time of the 2 μm ZnO NW memristor. The switching delay mentioned above was measured using an Agilent Infiniium 54810A high-speed oscilloscope with a 8 Gsa/s sampling rate while biased with a 8V pulse for 500 μs duration, which is detailed in [107]. It is also worth noting that, for device length variation of 100 nm, arising from the process variation which is completely random, the time required for switching varies between 335 μs and 410 μs , as obtained from the physics based circuit model. As a result, a SET pulse of 375 μs may or may not bring the memristor to the low resistance state (LRS), depending on the actual length of the device. To obtain the response of the PUF, a challenge bit is applied at one inputs of the SN7486 XOR gate and output of a voltage divider is connected to the second input of the XOR gate. Depending upon the state of the memristor the response bit will either be a logic 1 or logic 0. A total of 4 memristors from the same process (described in Section III) were implemented in the PUF circuit, of which 3 memristors produced a logic 1 as the response bit while 1 memristor produced a logic 0 for a challenge bit of logic 1. Once the response bit was obtained each memristor was RESET again and the sequence in Table 5.1 (SET \rightarrow RESET \rightarrow check response) was followed to verify the repeatability of the PUF function. We found that the output was consistent at least in 2 trials for each PUF.

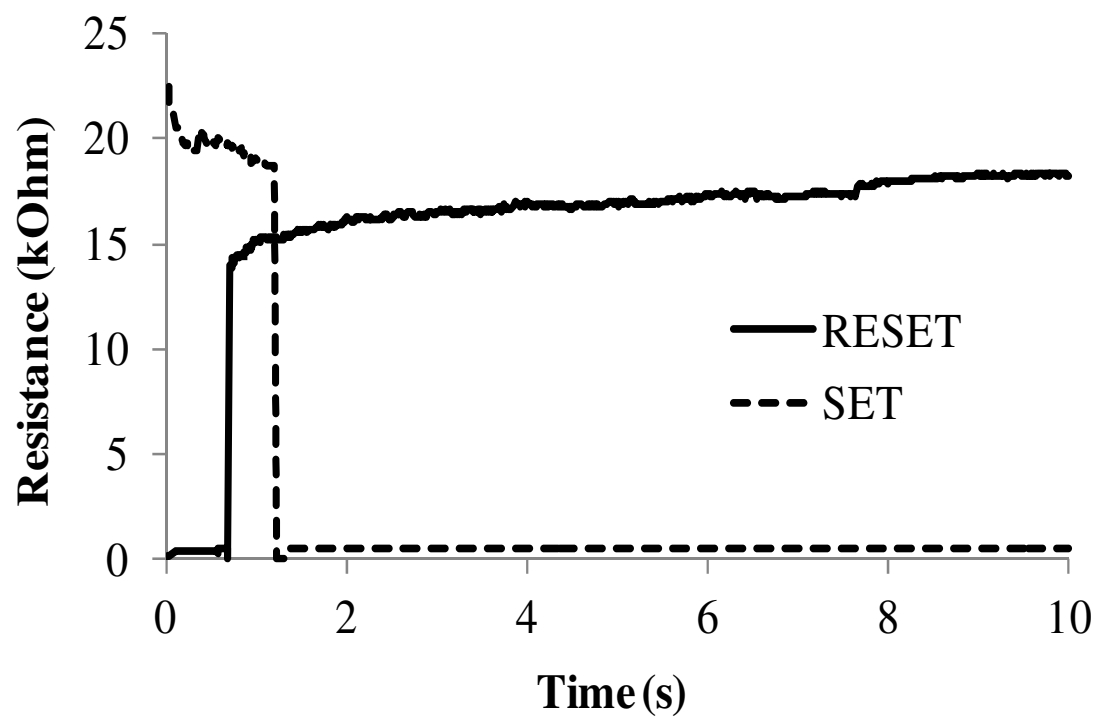


Figure 5.6. Measured SET and RESET switching of ZnO memristors

In order to further demonstrate the validity of the approach a second set of memristors, fabricated using a similar process as mentioned above but carried out at a different time frame to show the effect of process variability, was implemented in the PUF circuit. The typical SET and RESET characteristics of the memristors from the second process are shown in Fig. 5.6. For the SET switching, a 3V bias was applied across the memristor with a current compliance of 5mA to ensure that the device does not break down due to excessive current following through it during ON state. For the RESET switching, a -3V bias was applied across the device with 20 mA compliance current that allows a higher value of current to flow through the device, resulting in excessive heating and consequently rupture of the filaments, switching the device to OFF state. Implementation of the memristors in the PUF circuit produced logic 0 for both devices with a challenge bit of logic 0. This simple demonstration gives a proof-of-concept and shows a 50% uncertainty of the response bit for total 6 memristors.

It is to be noted that, the WRITE and READ voltages, V_{WR} and V_{RD} , required for the operation of the PUF can be scaled by scaling the device length. It is well known that, the role of the WRITE voltage in memristive systems is to drift the oxygen vacancies from anode to the cathode and thereby creating conductive filaments. This ionic drift process is dictated rather by the applied electric field than the WRITE voltage. As a result, the required WRITE voltage decreases linearly as the device scales, described by $E = V_{WR}/D$, where E is the electric field across the memristor. On the other hand, the READ voltage should be small enough so that it does not change the state of the device, and will scale

with the device length. As an example, scaling the ZnO NW memristor from 2 μm to 100 nm will result in a V_{WR} and V_{RD} of 0.125 V and 50 mV, respectively.

Memristors of different lengths varying from 50 nm to 2 μm , with the diameter fixed at 300 nm, were investigated by the authors for their switching speeds in [107]. Analytically derived carrier transport physics, which was also validated by experimental data of a ZnO NW memristor, were utilized to obtain the switching speeds. Shrinking the device lengths from 2 μm to 50 nm results in 3-4 orders of reduction in the delay in a typical memristor. This suggests that replacing the 2 μm memristor in the PUF circuit with a 50 nm memristor will result in approximately 98% reduction of switching delay and enhancement in PUF response. Mazady and Anwar studied switching delays of the popular material choices for memristors, namely ZnO, TiO₂, Ta₂O₅, HfO₂, and ZrO₂, and reported the fastest switching behavior of a ZrO₂ memristor. Switching delay of ZrO₂ is only 7.15 ps owing to a very high mobility of 370 cm²/V-s with a resistivity of 1.33 $\times 10^{13}$ $\Omega\text{-cm}$ of the insulating material. This suggests that replacing the ZnO memristor in the PUF circuit with a ZrO₂ memristor will result in 8 orders of magnitude reduction in the delay characteristics.

5.4 Conclusion

A physics based circuit model of memristors was implemented. The model represents a substantial improvement over the ones used in prior work as it incorporates the impact of physical structures and bias conditions of memristor for a more accurate representation of

the actual device. We used the same model to estimate the simulation time required for randomly selected polyominoes from a 3D array of memristors. The first hardware demonstration of a single bit PUF was also shown and the PUF uniqueness and reliability were quite promising. Furthermore, the model is versatile enough to be used for memristors fabricated using different material platforms.

Chapter 6 : Memristor based Digital Logic

6.1 Introduction

Boolean logics can be implemented using semiconductor devices, electromagnetic relays, optics, fluidic logic, and pneumatic logic, among others. Existing semiconductor logic elements utilizes diodes or transistors acting as electronic switches. The earliest microprocessors implemented using integrated circuit used resistor-transistor logic (RTL) and diode-transistor logic (DTL). The comparatively large static power dissipation in the resistive element of RTL and increased propagation delay through the diodes in DTL led to the emergence of transistor-transistor logic (TTL) families. With the advancement of semiconductor fabrication technology, complementary metal oxide semiconductor (CMOS) has eclipsed the previously mentioned logic families by offering reduced chip area, lower power consumption, and smaller propagation delay.

Scaling down of power consumption and device dimensions are being vigorously pursued for the realization of low power electronics. At present complementary metal oxide semiconductor (CMOS) with their small footprint, low power consumption, and small propagation delay is the technology of choice. Scaling of device dimensions with the current technology node being 22 nm, has not been followed by power supply voltage scaling due to restrictions on metal oxide semiconductor field effect transistor (MOSFET) threshold voltage (V_T). A decrease in V_T results in an exponential increase in leakage current detrimentally affecting voltage scaling and increasing the static power

consumption of CMOS logic family. As an example, with the leakage current of a 2-input CMOS NAND gate (74HC00) listed as 1 μA , the static power dissipation P_S equals 3 μW for a supply voltage $V_{DD}=3\text{V}$. Dynamic power consumption, on the other hand, depends upon the dynamic behavior related to switching frequency, rise and fall times of individual MOSFETs while switching, and their parasitic capacitances. As an example, for the same 2-input CMOS NAND gate, the dynamic power could be as high as 53.1 μW [$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + C_L \times V_{CC}^2 \times f_o$], where $C_{PD}=22\text{pF}$ is the dynamic power dissipation capacitance, $f_i=100\text{ kHz}$ is the input signal frequency, $N=2$ is the number of bits switching, $C_L=15\text{ pF}$ is the load capacitance including jig and probe capacitances, and $f_o=100\text{ kHz}$ is the output signal frequency. For a switching transition time of 19 ns, the switching energy equals 1 pJ, which could have been lowered if we were able to scale voltage without increasing leakage current. The switching transition time is defined as the sum of rise and fall times of the output signal, where rise time is the time required for the signal to reach from 10% to 90% of the ‘logic 1’ voltage and fall time is the time required for the signal to reach from 90% to 10% of the same voltage amplitude.

For technology nodes smaller than 65 nm, 90% of the total leakage current through any MOSFET is dictated by the tunneling current through gate oxide which is more pronounced for thinner oxides [110]. High-k dielectrics with the dielectric constants k ranging from 7.5 to 300 have been explored in recent years to reduce tunneling current. Ultra high-k materials, such as BST (Ba,Sr)TiO₃ with $k=300$ may achieve the thinnest equivalent oxide thickness (EOT) but suffers from fringing-induced barrier lowering (FIBL) [111, 112], such that fringing electric fields from source and drain junctions to the

channel lowers the potential barrier between source and channel. As a result of FIBL, threshold voltage V_T of the MOSFET decreases and leakage current increases. High- k materials in the moderate range of dielectric constant, such as Si_3N_4 ($k=7.5$) and Al_2O_3 ($k=10$), contain random interface trap (RIT) states that gives rise to Coulomb scattering degrading carrier mobility. Midrange dielectric constant materials, such as ZrO_2 ($k=22$) and HfO_2 ($k=25$) happen to be the materials of choice for gate oxide. However, incompatibility with poly-silicon gates has limited the use of ZrO_2 in MOSFETs while issues such as boron penetration, low crystallization temperature, charge trapping, and low channel mobility still need to be resolved for HfO_2 gate oxide.

Improved electrostatic control of multi-gate devices makes them an optimized choice for sub-32nm technology, with FinFETs being of particular interest due to their compatibility with the traditional planar CMOS process [113], reduced short channel effects (SCE), and reduced junction leakage due to band-to-band tunneling (BTBT) [114]. However, TCAD simulations of bulk FinFET technology suggest leakage current as high as 10 nA/ μm for 65 nm technology node resulting in static power dissipation $P_S = 12$ nW/ μm for $V_{DD}=1.2$ V that increases to 2 $\mu\text{A}/\mu\text{m}$ ($P_S = 1.6$ $\mu\text{W}/\mu\text{m}$ for $V_{DD}=0.8$ V) for 22 nm node [115]. With silicon on insulator (SOI) FinFETs the leakage current is reduced to 0.4 $\mu\text{A}/\mu\text{m}$ ($P_S = 0.32$ $\mu\text{W}/\mu\text{m}$ for $V_{DD}=0.8$ V) for 22 nm node by isolating the device layer from the silicon substrate and similar results may be obtained for bulk FinFETs by increasing body doping from 10^{16} cm^{-3} to 10^{18} cm^{-3} [115]. Additional reduction in leakage current may be obtained by optimizing the isolation oxide height (T_{ins}) between the gate and substrate for bulk FinFETs. As an example, decreasing T_{ins} from 150 nm to 50 nm decreases the

leakage current from 580 nA/ μm ($P_S = 0.52 \mu\text{W}/\mu\text{m}$ for $V_{DD}=0.9 \text{ V}$) to 250 nA/ μm ($P_S = 0.22 \mu\text{W}/\mu\text{m}$ for $V_{DD}=0.8 \text{ V}$) for 32 nm technology node, however, further decrease of T_{ins} increases the leakage current [115]. Research has also been carried out with different fin widths and shapes that suggest decreasing the fin width reduces leakage current by suppressing SCEs [114] with a triangular fin reducing the leakage current and, as a result, the static power dissipation by 70% compared to a rectangular fin [116]. However controlled etching of fins to meet specific shape and dimension requirements is rather challenging [117]. The best performance of FinFETs that has been published in recent years reported leakage current of 0.1 $\mu\text{A}/\mu\text{m}$ [113, 118, 119] for regular FinFETs and 1 nA/ μm for low power (LP) FinFETs [120], causing static/ leakage power of 80 nW/ μm and 0.8 nW/ μm , respectively. Assuming a power dissipation capacitance $C_{PD} = 2.4 \times 10^{-15} \text{ F}/\mu\text{m}$ following the discussion of [118, 121], the dynamic power dissipation for the FinFET with $V_{DD} = 0.8 \text{ V}$ at 100 kHz switching frequency and load capacitance of 15 pF/ μm is 308 $\mu\text{W}/\mu\text{m}$.

The global market for circuit elements with memory (memristor) is expected to rise from essentially zero in 2012 to over \$100 million in 2018, and to exceed \$675 million in 2023 as per the January 2014 BCC Research Report [122], Such components, allowing low power computation, will replace the present digital logics as predicted by Di Ventra *et al.* [123]. Integration of memristors with the current CMOS technology has also been demonstrated by interconnecting two 21 \times 21 memristor crossbars with several conventional silicon FETs [106]. The fabricated architecture was implemented to route 4 digital voltage inputs using 4 memristors and 2 FETs to perform Boolean sum-of-product

operation with 20% yield. Designing logics using memristors allows the use of the same physical unit as multiple functional units, such as – memory, logic, and interconnect [106]. This approach has the potential to redefine the traditional computer architecture to advanced architectures overcoming the “von Neumann bottleneck” of throughput [124]. The traditional von Neumann architecture requires sequential processing of fetch, decode, and execution of instructions resulting in reduced data transfer rate. Performing the logical operations within the memory element permits the central processing unit (CPU) to simultaneously access both the program memory and data memory utilizing the full potential of the CPU.

Memristors, since their experimental demonstration in 2008, provides an alternative platform for low power and scalable logic. Unlike shorting the power supply and ground buses during switching of CMOS logics, memristor offers a finite resistance during the ON state preventing any short circuit current. The dynamic power consumption of a 100 nm ZrO_x memristor is only 67.5 nW, assuming a SET voltage of 0.15V, input signal frequency of 100 kHz, and load capacitance of 15 pF. For a total transition time of 14.3 ps, the switching energy of memristor logic is merely 9.65×10^{-19} J. Among the futuristic technologies carbon nanotube (CNT) FET based inverter logic was reported to have the minimum switching energy of 6.08×10^{-17} J through HSPICE simulations which is two orders of magnitude higher than memristor based logic gates .

Material Implication (IMP) logic, $x \rightarrow y$ (‘x implies y’ or ‘if x then y’), is one of the fundamental building blocks, together with the FALSE logic, of all Boolean logic

operations [8]. The concept of IMP logic was pioneered by Whitehead and Russel in their classic 1910 *Principia Mathematica* [125]. The importance of IMP logic can be understood by the fact that, IMP and FALSE logics together form a computationally complete logic basis and can compute any compound Boolean operation. The term “*Material*” has traditionally been used to distinguish between a “Material Implication” and “Logical Implication”, although from an electrical engineering perspective they have identical truth tables and imply similar functionality. Logicians use material implication, also known as “material consequence”, “implication”, “implies”, or “conditional”, as a binary connective to create new sentences in the form of “if....then” structure. The truth value of the conditional new sentence entirely depends on the truth values of the component propositions. In other words, material implication resembles the conditional in ordinary language that says if the antecedent is true and the consequent is false, then and only then the entire conditional is false. As an example, “if you own a dog, then you own an animal” is a material implication in the sense that the conditional is false only if someone claims that he owns a dog but does not own an animal. The material implication logic can be realized using only a resistor and two memristors. Similar to Shannon’s formulation [126], the physical states of the memristors, namely - high resistance state (HRS) or low resistance state (LRS), are implemented as the logic inputs for the IMP gate. In that sense, memristor based IMP logic is also a ‘stateful’ logic with the memristors remembering their states and performing the logic operations at the same time. The fact that the same device serves both as logic and memory in the IMP logic architecture, the demonstration of IMP logic using memristors also means demonstration of a non-von Neumann architectures. Use of memristors as logic gates has mostly been

reported through phenomenological models or simulations [124]. A simulation model of memristor based IMP logic was reported by Kvatinsky *et al.* which suggested that the widely used linear ionic drift model is not practical for IMP logic gates [127]. The same group also proposed a possible architecture for 8-bit full adder using only IMP and FASLSE logics [124]. Klimo *et al.* proposed voltage based fuzzy logic computations using memristors which is an extension of classical Boolean logic [128]. A hybrid of CMOS-memristor logic, also known as memristor ratioed logic (MRL), can be constructed by performing OR and AND logic operations using memristors while signal sensing and restorations using CMOS inverters [129]. Chang *et al.* proposed a computer architecture implementing memristor based latch and flip-flops in the arrangement of a 3D-IC [130]. Rajendran *et al.* designed programmable threshold gates using memristors, where memristors were used as weights at the inputs of the threshold gates [131]. Another alternative to obtain stateful logic operation involves use of magnetic tunnel junctions (MTJ) where spins of magnetic materials are employed as the physical state, as reported by Wang *et al.* [132]. Two separate current biases switched the magnetization of the active layer and operations of six logic gates were demonstrated. Kimura *et al.* combined a ferroelectric memory element in a configurable logic gate by implementing complementary ferro-electric capacitors [133]. It is worth noting that the fabrication of the devices involving Ta/NiFe/MnIr/CoFe/Al layers with thickness of 7 Å demands a very advanced and expensive fabrication facility. Moreover, a Wheatstone bridge was required for the read circuitry adding to the power requirement of the device. However, compared to MTJs, memristors promise faster switching at 120 ps with power consumption in the range of pJs [8].

Other demonstrations of nanoelectronic circuit based logic operations [106, 134-137] required incorporation of transistors to be computationally complete as the nanoelectronic crossbar architecture was incapable to perform NOT operation by itself. Such architectures cannot use the full potential of the dense crossbar configuration as only a small subset of the junctions can actually be used to fetch the data to the transistors. Design of an alternative logic family is hence required beyond the realm of usual Boolean logics (i.e. AND, OR, NOT, and so on). IMP logic, not requiring a NOT operation and thus a transistor, is a very important proposition toward developing such alternative logic architectures. The only demonstration of IMP logic using memristor till date has been reported by Borghetti *et al.* using TiO₂ thin film crossbars [8]. It is important to note that Borghetti *et al.* used current amplifiers in order to distinguish between logic outputs which results in an increased power requirement for the logic. In addition, fabrication of the crossbar architecture reported by Borghetti *et al.* required a two step metallization process that complicates the fabrication process and results in sneak paths [138].

We report experimental demonstration of IMP logic using ZnO nanowire (NW) memristors. For devices with identical geometries, ZnO results in faster switching compared to TiO₂ memristors [107]. For example, a 2 μm ZnO NW memristor shows 4 orders of faster switching than TiO₂ memristor. Additionally, the NW architecture allows higher packing density of the logic or memory elements compared to thin film memristors.

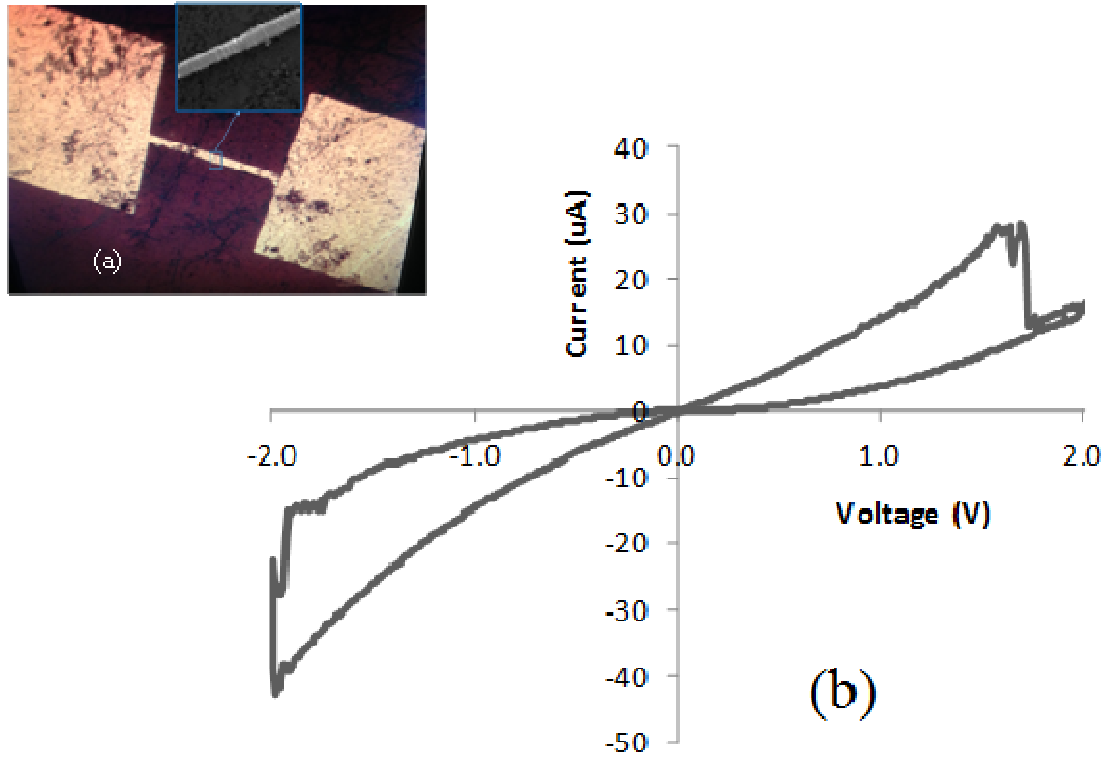


Figure 6.1. DC I-V characteristics of an Al/ZnO NW/Al memristive device. Inset: Optical microscopic image of the device fabricated using EBL showing the electrodes.

6.2 Fabrication and Characterization of Memristors

ZnO NW memristors were fabricated using a three-step process. In the first step, ZnO epitaxial layer was grown using metalorganic chemical vapor deposition (MOCVD) that serves as the nucleation layer for the subsequent growth. Following the growth of the epitaxial layer, a novel process developed to grow horizontal nanowires using controlled hydrothermal synthesis was performed as reported by Rivera *et al.* [139]. It is to be noted that unlike the standard practice of growing vertical NRs followed by pick-and-place technique to obtain horizontal nanostructures, the present technology allows the direct growth of horizontal nanowires. SEM measurements suggest the NWs to be 2-5 μm long with the diameter varying from 400 nm to 600 nm as shown in the inset of Fig. 6.1 (a). Microscopic image of the fabricated device is shown in Fig. 6.1 where electron beam lithography (EBL) was used to pattern the contact electrodes. Al contacts were deposited using physical vapor deposition (PVD) technique followed by lift off and annealed at 300°C.

Fig. 6.1 shows the fabricated ZnO NW memristive device that has a length of 2 μm . The measured DC I-V characteristic is shown in Fig. 6.1(b). A positive bias greater than 2V applied for 10 μs toggles the device from high resistance state (HRS) to low resistance state (LRS). HRS and LRS of the device are defined as logic '0' and logic '1' inputs to the device, respectively. A negative voltage, with magnitude larger than -2V, resets the device to HRS. For a smaller or zero bias voltage, the device does not switch and remains in the same resistance state, confirming the fundamental property of ReRAM.

6.3 Demonstration of IMP Logic

In order to implement the IMP logic stable resistance levels of LRS and HRS is required, that collapse only minimally in subsequent voltage sweeps [16]. LRS of 1.1 – 1.3 k Ω and HRS of 6.25 – 7.15 k Ω at 1V applied bias is chosen for stable and repeatable switching. Successful demonstration of the IMP logic using memristors of HRS/LRS ratio of only ~5 is a significant improvement over the requirement of HRS/LRS ratio of 100 reported by Borghetti *et al.* [8]. The capability of the logic gates to function with memristors of smaller HRS/LRS ratio means that they have less stringent requirements on the memristor performance, resulting in lower bit error rates, improved endurance, and better retention characteristics.

A schematic of the IMP logic employing memristive systems is shown in Fig. 6.2. In this configuration two memristors (M1 and M2) are connected to a common node and to a load resistor $R_L=1$ k Ω . The input logic voltages (x and y) correspond to the initial states of M1 and M2 (HRS = logic ‘0’ and LRS = logic ‘1’). The memristors can be SET to logic ‘1’ by applying a positive bias voltage V_{SET} for 10 μ s. It is important to note that positive bias is ubiquitously used for digital logic operation than the previously demonstrated IMP operation with negative bias [8]. The magnitude of V_{SET} is selected as 3V, higher than the threshold voltage required for switching, to ensure switching in the subsequent voltage pulses. The devices require a negative voltage of –5V to RESET (logic ‘0’). Prior to each logic operation of the truth table, a read voltage of 1V is applied across the device and the resistance is measured. An intermediate voltage $V_{INT} = 1.3$ V is

x	y	z
0	0	1
0	1	1
1	0	0
1	1	1

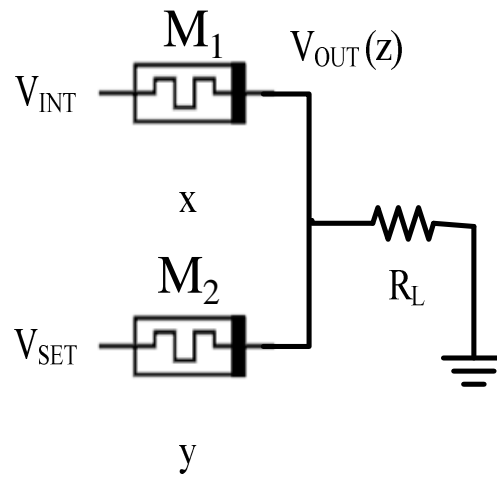


Figure 6.2. Truth table and schematic diagram of the IMP logic employing two memristors.

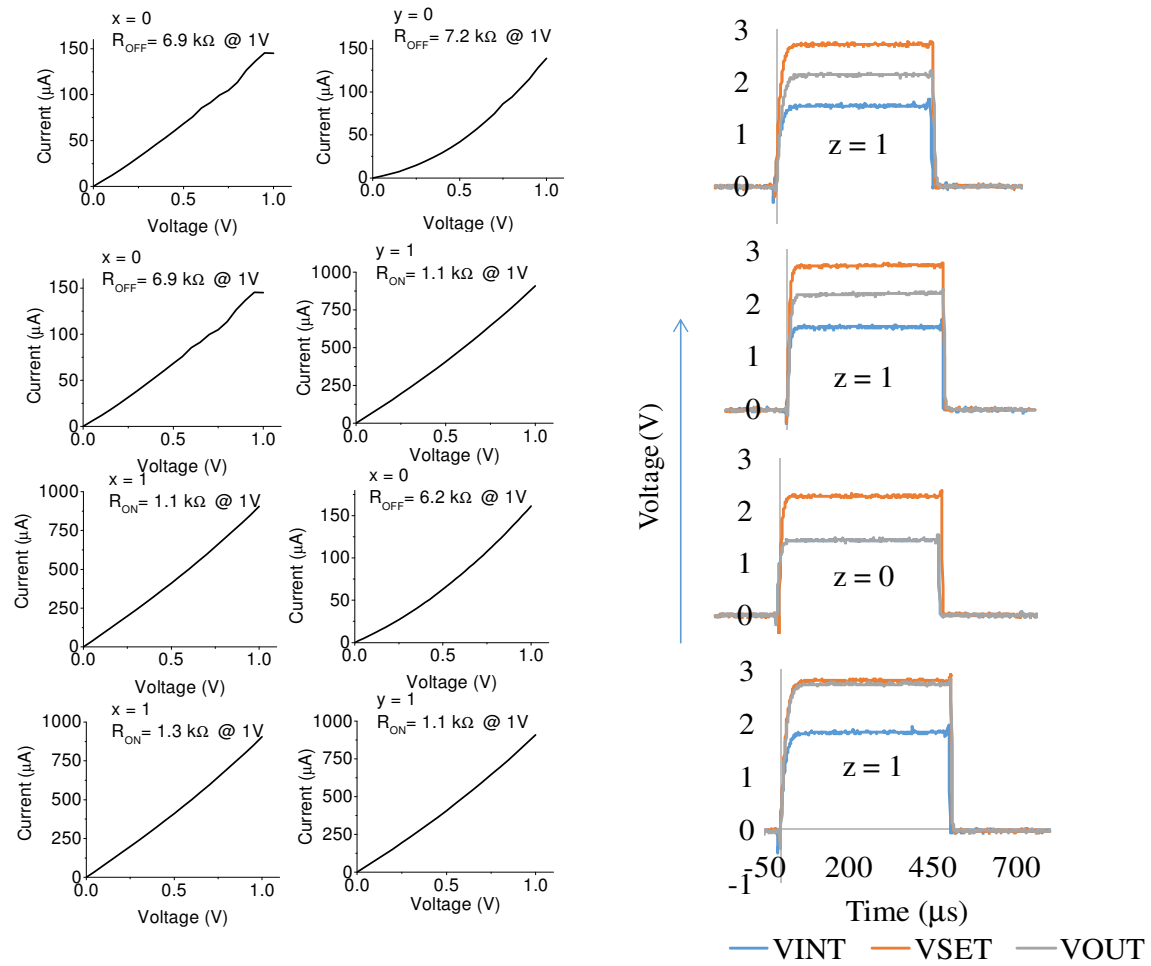


Figure 6.3. Experimental demonstration of IMP logic operation using memristors.

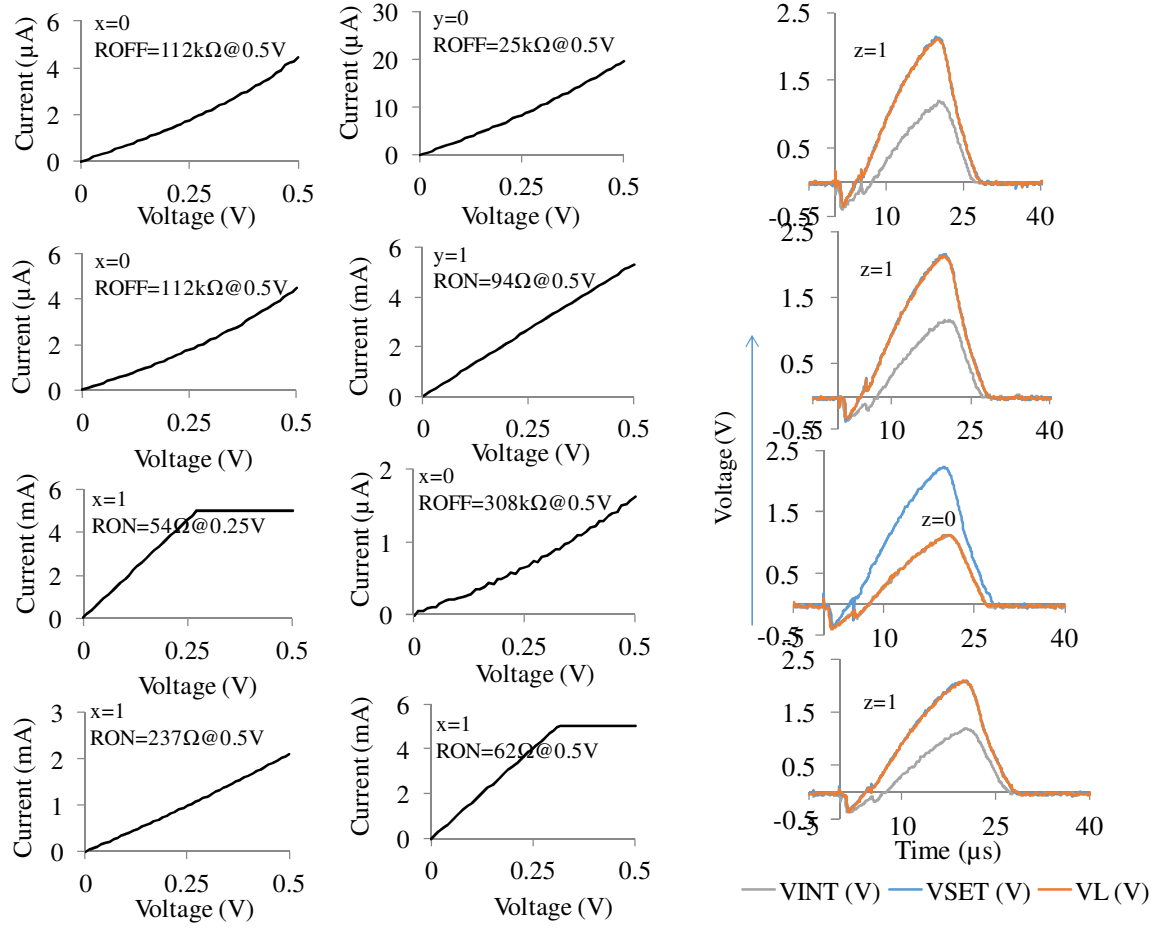


Figure 6.4. Experimental demonstration of memristor based IMP logic at 100 kHz frequency.

defined such that $V_{SET} - V_{INT}$ is smaller than the threshold voltage required for switching. V_{INT} is considered as the higher limit of logic '0' throughout this experiment.

The IMP operation is performed by applying a V_{INT} pulse to M1 and a V_{SET} pulse to M2 simultaneously. The circuit is configured as a synchronous logic that triggers at the rising edge of a clock pulse. For initial conditions $x = 0$ and $y = 0$, both memristors M1 and M2 are in HRS and V_{OUT} is in logic '0' ($z = 0$). With the triggering of the clock pulse, V_{INT} and V_{SET} are applied to M1 and M2, respectively. Pulse V_{INT} is not enough for M1 to switch, however, V_{SET} switches M2 to LRS and z becomes a logic '1' as shown in Fig. 6.3. For initial conditions $x = 0$ and $y = 1$, LRS of M2 results in a high V_{OUT} . With the application of the next clock pulse, V_{INT} does not switch the resistance of M1, and V_{SET} does not switch M2 as it already was in LRS. As a results, V_{OUT} remains high and $z = 1$. For initial conditions $x = 1$ and $y = 0$, LRS of M1 brings V_{OUT} close to V_{INT} . In the succeeding clock trigger, voltage across M2 is $\sim V_{SET} - V_{INT}$, which is not enough to switch M2 to LRS due to such selection of V_{INT} magnitude, and as a result $z = 0$. For initial conditions $x = 1$ and $y = 1$, both the memristors are in LRS and with the application of V_{INT} and V_{SET} , voltage magnitudes $V_{INT} - V_{OUT}$ and $V_{SET} - V_{OUT}$ are not sufficient to switch either M1 or M2.

In order to demonstrate the reproducibility and reliability of the logic switching measurements, a second set of memristors, fabricated using a similar process as mentioned above but carried out at a different time frame to account for the effect of process variability, was implemented. The Boolean logics of the truth table shown in Fig.

6.2 were demonstrated using the new set of memristors and the results are shown in Fig. 6.4. The LRS and HRS resistances were not regulated within a tight range as the experiment mentioned earlier to emulate a more practical scenario and R_{ON} varied in the range 54 – 237 Ω while R_{OFF} varied in the range 25 – 308 k Ω . During the READ operation of the mentioned R_{ON} and R_{OFF} resistances, the supply voltage was swept from 0 to 0.5 V and a current compliance of 5 mA was imposed by the semiconductor parameter analyzer so that the devices do not breakdown due to excessive current flowing through them. The logic gate was demonstrated to be functional at a clock frequency of 100 kHz. The lone experimental demonstration of IMP logic by Borghetti *et al.* [8] did not report the frequency of operation, and to the best of our knowledge this is the fastest IMP logic that has ever been reported.

It is to be noted that, the bias voltage required for the memristor to switch can also be scaled by scaling the device length. It is well known that, the role of the bias voltage in memristive systems is to drift the oxygen vacancies from anode to the cathode and thereby creating conductive filaments. This ionic drift process is dictated rather by the applied electric field than the bias voltage. As a result, the required bias voltage decreases linearly as the device scales, described by $E=V/d$, where E is the electric field, V is the applied bias, and d is the length of the memristors. As an example, scaling the ZnO NW memristor from 2 μm to 100 nm will result in a V_{SET} of 0.15 V, V_{INT} of 65 mV, V_{RESET} of -0.25 V, and V_{READ} of 50 mV. Such voltage scaling leads to reduced power consumption as shown in Fig. 6.5. The total power consumption of 50 nm memristor based IMP logic is only 56.2 μW . The reported voltage scaling is a significant improvement over the IMP

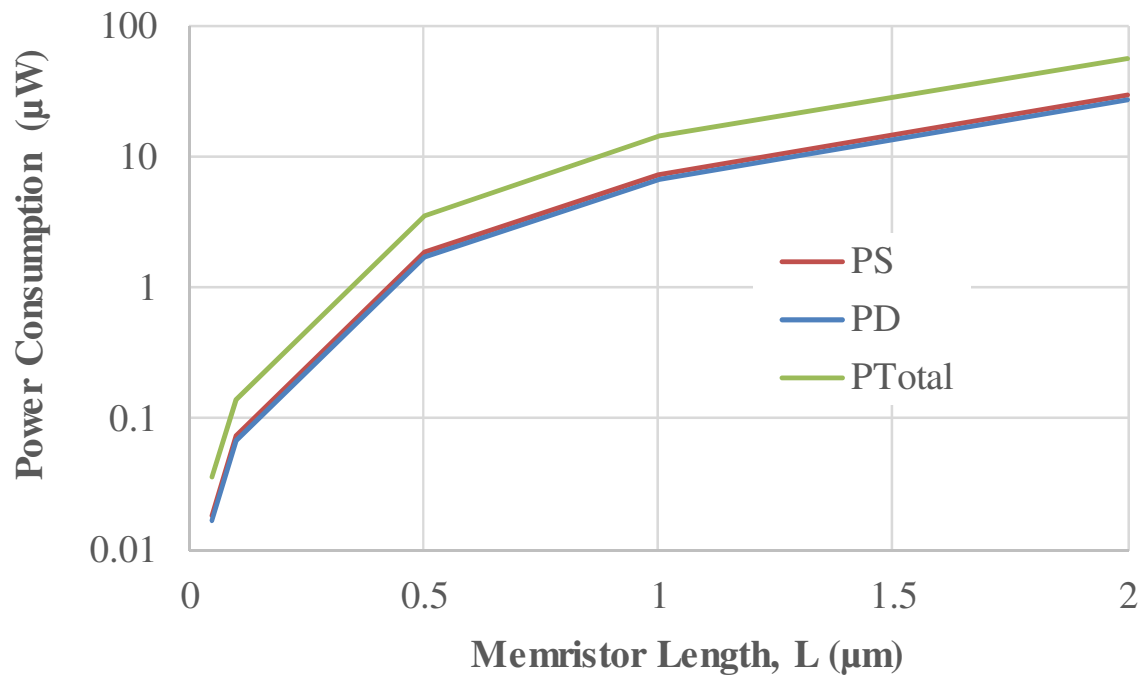


Figure 6.5. Power dissipation of memristor based implication logic as a function of device length.

logic gates demonstrated by Borghetti *et al.* [8] that required V_{SET} and V_{RESET} of -5V and 9V, respectively, for 50 nm TiO_2 memristors.

Memristors of different lengths varying from 50 nm to 2 μm , with the diameter fixed at 300 nm, were investigated by Mazady and Anwar for their switching speed [107]. Analytically derived carrier transport physics, which was also validated by experimental data of a ZnO NW memristor, were utilized to obtain the switching speeds. Shrinking the device lengths from 2 μm to 50 nm results in 3-4 orders of reduction in the delay of a typical memristor. This suggests that replacing the 2 μm memristors in the logic gates with 50 nm memristors will result in approximately 98% reduction in the gate delay. Mazady and Anwar studied switching delays of the popular material choices for memristors, namely ZnO, TiO_2 , Ta_2O_5 , HfO_2 , and ZrO_2 , and reported the fastest switching behavior of a ZrO_2 memristor. Switching delay of ZrO_2 is only 6.8 ps owing to a very high mobility of 370 $\text{cm}^2/\text{V}\cdot\text{s}$ with a resistivity of $1.33 \times 10^{13} \Omega\cdot\text{cm}$ of the insulating material.

6.4 Conclusion

ZnO NW memristors were fabricated using MOCVD followed by hydrothermal synthesis and EBL. Two memristors were implemented to construct an IMP logic, where they serve as both the memory and logic elements. The IMP logic was successfully demonstrated with a $R_{\text{OFF}}/R_{\text{ON}}$ ratio as low as 5, resulting in smaller bit error rate of the logic function. Logic pulses of positive amplitudes were demonstrated showing the

viability to be used with the existing binary logic systems. The capability to perform logic operations within the memory element shows the potential of designing a computer architecture different from the familiar paradigms of Von Neumann systems. Power consumption by memristors based logic gates is significantly lower than CMOS based gates that can be reduced further by scaling the memristors [121].

Chapter 7 : Experimental Realization of Chaotic Circuit using Physical Passive Memristive System

7.1 Introduction

In recent years, complexity of dynamical systems and nonlinear circuits has aroused a great deal of interest in the scientific community [14, 140, 141]. Circuits showing perfect chaotic behavior have potential applications in cryptography, military communications [142], and trajectory recognition [65]. Analysis of chaos in the earth-moon fuzzy boundary, which is popularly known as the unsolvable “three body problem” in contrast to the “two body problem” solved by Sir Isaac Newton, will result in 25% less fuel for lunar exploration missions [143] and improves for explorations of the other celestial bodies, such as the *Genesis Discovery Mission* by NASA [144]. A system showing chaotic behavior should have the following characteristics:

- The system should be aperiodic in time and superposition of any number of periodic motions is incapable to describe the aperiodic behavior.
- The system should be deterministic and the same initial conditions should lead to the same final state. However, very small change in the initial conditions should result in very significant change in the final state.
- A short term prediction of the response of the system may be made, but it must be difficult or impossible to make any long term predictions.
- The phase-space trajectory should be complex but ordered.

It should be noted that, a deterministic chaotic system must not have random temporal dynamics that is irreproducible.

Experimental evidence of deterministic chaos has been reported for dissipative non-linear systems [145-149]. Demonstration of the first chaotic attractor was reported by Edward Lorenz in 1963, when he was trying to improve weather forecasting [150]. The systems of equations that define convection of atmosphere were given as the following, and are now popularly known as Lorenz equations:

$$x' = -10(x - y)$$

$$y' = 28x - y - xz$$

$$z' = xy - \frac{8}{3}z$$

where x , y , and z are the state variables of the system. Scrutiny of Lorenz equations suggests that they are: (i) non-linear, (ii) contains at least 3 state variables, and (iii) although the system is chaotic, it can be defined by only a set of 3 equations, demonstrating *deterministic* chaos rather than stochastic chaos. Numerical solution of Lorenz equations did not have any stable solution suggesting that it may be possible to forecast the atmospheric conditions in the near future, however, forecasting weather in the distant future is impossible, as infinitesimal uncertainty in the initial conditions results in very large change in the atmospheric conditions. Several other systems, namely, lasers [151], dynamo [152], fluid flow [153], brushless DC motors [154], chemical reactions [155], and forward osmosis [156], have also been demonstrated to have

characteristics described by the aforementioned Lorenz equations. Swinney *et al.* demonstrated chaotic behavior in four different types of systems, namely, nonlinear oscillator, Belousov-Zhabotinskii reaction, Rayleigh-Benard convection, and Couette-Taylor system [145]. The nonlinear circuit consisted of a resistor, an inductor, and a varactor diode that conducts in forward bias and has nonlinear capacitive characteristics in reverse bias. The series circuit has three degrees of freedom. The Belousov-Zhabotinskii reaction is an oscillating chemical system that involves cerium-catalyzed bromination and oxidation of malonic acid by a sulfuric acid solution of bromate which can be modeled by a set of coupled nonlinear ordinary differential equations. In Rayleigh-Benard convection system, parallel plates containing a fluid is heated from the bottom. Rayleigh number $R_a = (g\alpha d^3/\kappa\nu)\Delta T$ is used as a control variable for this system, where g is the gravitational acceleration, α is the thermal expansion coefficient, d is the thermal distance between the parallel plates, κ is the thermal diffusivity, and ν is the viscosity. In contrast, Couette-Taylor system employs fluid contained between concentric cylinders that rotate with angular velocities of Ω_i and Ω_o , respectively. Reynolds number for this system are given as, $R_i = (b - a)a\Omega_i/\nu$ and $R_o = (b - a)b\Omega_o/\nu$, respectively, where a and b are the radii of the inner and outer cylinders.

One of the most intensively investigated circuit in relation to identifying the nature of chaos is Chua's piecewise linear circuit that was introduced in 1986 [157]. Before that nonlinear dynamics of circuits were often ignored. For example, Dutch electrical engineer and physicist van der Pol reported his experiments on neon bulb oscillators in a 1971 Nature journal where he described the observed nonlinearity as "often an irregular

noise is heard” and ignored it as “a subsidiary phenomenon” [158]. However, the origin of such noises are now well studied and understood. Chaotic circuit in its simplistic form is an aperiodic oscillator that unlike an ordinary electronic oscillator do not have repeating waveforms. The circuit proposed by Chua, exhibiting complex dynamics of bifurcation and chaos and yet requiring very simple setup, has been extensively studied [14, 159-163], and has been regarded as “a paradigm for chaos” [164]. The original Chua’s circuit consisted of an inductor, a linear resistor, two capacitors, and a voltage controlled nonlinear resistor known as “Chua’s diode”. The fourth order non-autonomous circuit exhibited a large variety of bifurcations, namely period adding, quasi-periodicity, intermittency, equal periodic bifurcations, double scroll attractors, hysteresis and coexistence of multiple attractors [159]. In order to demonstrate chaotic behavior, a circuit must contain [165]:

- i. At least one element with nonlinear characteristics
- ii. At least one locally active resistor
- iii. A minimum of three energy storage elements

Since the discovery of memristor, high non-linearity in its carrier dynamics has led researchers to study its effects through mathematical analysis and numerical simulations by replacing Chua’s diode with a memristor in Chua’s circuit [64]. Memristor is regarded as the fourth fundamental circuit element that gives the relationship between magnetic flux (φ) and electric charge (q). The current-voltage relationship of memristor is given as $V_M = M(q)I_M$, where V_M and I_M are the voltage across and current through the memristor and $M(q)$ is the memristance. Unlike resistances, memristance $M(q)$ is dependent on

amount of charge (q) that has passed through the device thereby making resistance of a memristor different at each point of its I-V characteristics. This phenomenon gives rise to the observed non-linearity in memristor based circuits and a pinched hysteresis loop is observed in memristor I-V characteristics. The same voltage across the memristor can thus produce two different currents through it depending on the state of the device, namely, HRS or LRS. One important aspect of this hysteresis loop is that, it is dependent on the frequency of operation, with high frequencies diminishing the hysteresis effect and making it similar to a linear resistor. Although the first experimental claim of a physical memristor was made only recently in 2008, naturally occurring phenomena typical of memristor characteristics have been observed for two centuries in biological ion channels [166], discharge lamps, tungsten filaments, hissing arcs, thermistors [167], complex oxides [35], and spintronics [168], among others.

Memristor, being a non-linear element with built-in memory, allows realization of chaotic circuits of compact forms [169]. Itoh and Chua showed that replacing the Chua's diode with a memristor of piece-wise linear $\varphi - q$ relationship can generate a gallery of chaotic attractors including the Chua's oscillator. Ahamed *et al.* reported chaotic beats using three-segment piecewise linear driven Chua's circuit for a suitable choice of parameters where the memristor emulator acts as a chaotic time varying oscillator [170]. An external driving sinusoidal bias shifted the self-oscillation frequency of the memristor emulator to a lower value. The superposition of the sinusoidal excitation and the memristor self-oscillation gave rise to amplitude modulation, envelope of which exhibited chaotic behavior. Barboza and Chua proposed a chaotic circuit employing only

4 functional elements, with one being an emulator of memristor which itself consisted of a number of passive and active components, such as operational amplifiers [171]. An improvement to this circuit configuration was proposed by Muthuswamy and Chua that employed only 3 functional elements -- a capacitor, an inductor, and a memristor emulator – that was argued to be the most compact form of chaotic circuit [172]. The negative differential resistance region of the memristor was employed to generate the chaos and the memristor was said to be a “locally-active” element. It is to be noted that, in this configuration the memristor emulator required +15V and -15V power supplies to bias the opamps employed to emulate memristor. Driscoll *et al.* have recently showed that a chaotic circuit can be constructed by utilizing only a memristor and a series resistor [142]. The memristor behavior was emulated using a microcontroller such that it has the characteristics of a double potential well. More specifically, the memristor emulator had the following characteristic equation,

$$\frac{d}{dt} \begin{bmatrix} x \\ \dot{x} \end{bmatrix} = \begin{bmatrix} \dot{x} \\ -\frac{1}{m} \frac{\partial U}{\partial x} - \gamma \dot{x} + \frac{F(V_M)}{m} \end{bmatrix}$$

where m is the effective mass in the potential well, $U(x)$ is the multi-well potential with $U(\pm\infty) = \infty$, γ is the damping coefficient and F is the driving force associated with the bias applied to the memristor. This equation describes the carrier dynamics in a multi-well potential that resembles electron hopping from one fragmented filament to the next inside memristor. However, the demonstration of proof-of-principles was only made possible by emulating the memristive systems using a number of active circuit components, such as opamps [172] and microcontrollers [142], marring the benefits of a

compact circuit. Zhong *et al.* reported chaotic behavior of Chua's circuit with memristor emulator having cubic nonlinearity [173]. Replacing the piece-wise linear characteristics in Chua's circuit with a continuous nonlinear polynomial allowed practical implementation of the circuit where the cubic nonlinearity was provided by a memristor emulator. Several works have been reported in an effort to mimic memristor characteristics with discrete components, such as using mutators [1], micro-controllers [11], multiplexers and operational amplifiers [174], cellular nonlinear networks [175], among others. However, in all these cases ideal characteristics of memristor was implemented that has linear dopant drift profile and symmetric I-V characteristics. It was conjectured that the non-linear resistor in Chua's circuit is required to have odd-symmetric nonlinear I-V characteristics to generate chaos. However, Buscarino *et al.* have showed that theoretically it is possible to develop chaotic circuits using memristors with non-symmetrical I-V characteristics that neither have piece-wise linear charge-flux relationship nor do have cubic nonlinearity [169]. The governing equations of memristor based on the front-like dopant movement were considered and an anti-parallel combination of 2 memristors generated chaos. The window function proposed by Biolek *et al.* was considered in all the simulations [17].

It is to be noted that the desired nonlinear characteristic with cubic or higher order polynomials is readily achievable with a passive memristive system as has been reported by Mazady and Anwar [76]. Moreover, memristor has different coefficients of the polynomial equations at different regions of operations adding to the complexity of the non-linear circuit. The polynomial equations were derived from the dynamical behavior

of memristors that takes into account the underlying physics and electrochemistry [16]. Tunneling barrier width (or filament length) was used as the state variable that decreases to 0 nm during the ON state of the device. The formulation explains the coupled electronic and ionic conduction observed in such devices.

The cubic and higher order non-linearity in memristor I-V characteristics, that can be exploited to construct chaotic circuit, is expressed by the following polynomials [76]:

$$I_1 = -11.8V_{APPL}^4 + 35.4V_{APPL}^3 - 23.6V_{APPL}^2 + 7.8V_{APPL} - 0.4$$

$$I_2 = -4.8V_{APPL}^4 - 18.7V_{APPL}^3 + 27.6V_{APPL}^2 - 18.1V_{APPL} + 4.6$$

$$I_3 = 500V_{APPL}^3 + 0.5V_{APPL}^2 + 11.6V_{APPL} - 0.05$$

$$I_4 = 69V_{APPL}^2 + 172V_{APPL} - 34.5$$

$$I_5 = -2.1V_{APPL}^4 - 8V_{APPL}^3 - 11.5V_{APPL}^2 - 7.3V_{APPL} - 1.7$$

Currents I_1 , I_2 , I_4 , and I_5 were obtained by fitting the filament assisted tunneling currents in regions oa , ab , cd , and do of the I-V characteristics as shown in Fig. 7.1. It can easily be observed that the polynomial equations that describe the I-V characteristics of memristors have different coefficients at different regions of operations, namely during high resistance state (HRS), low resistance state (LRS), and during switching events. It is important to note that such nonlinearity was artificially incorporated in a memristor emulator using 1 opamp, 2 multiplexers, and 5 resistors by Zhong *et al.* [173].

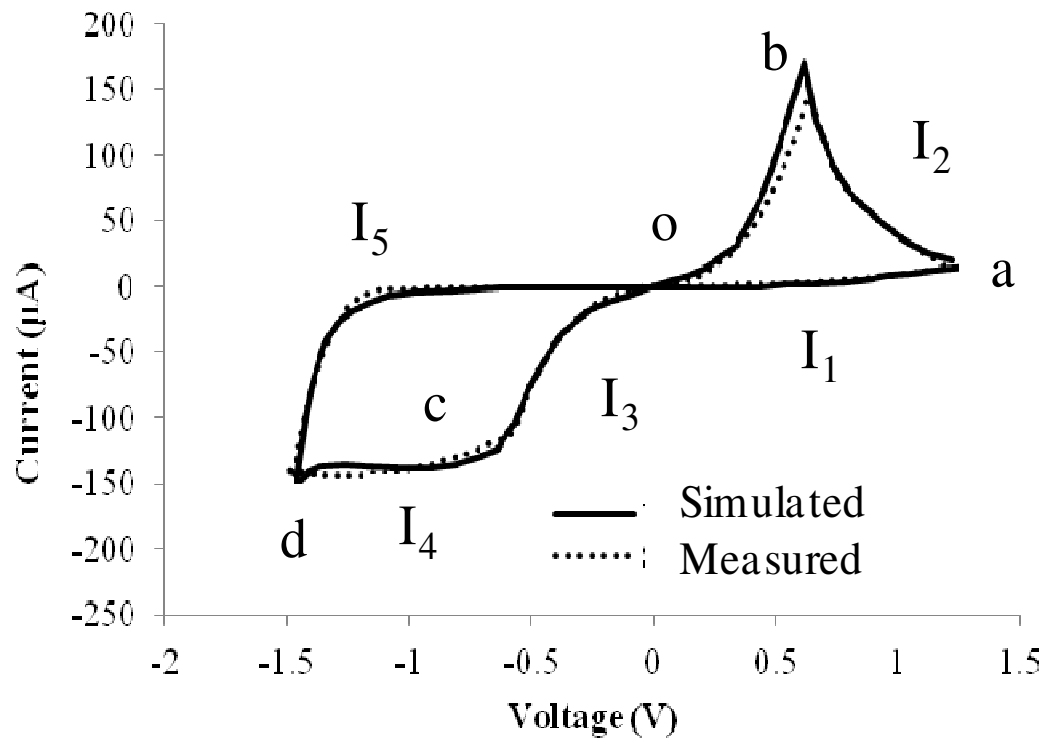


Figure 7.1. Simulated and measured I-V characteristics of a Pt/TiO₂/Pt memristor [76].

Exploiting such inherent nonlinearity of passive memristors, development of a chaotic circuit is reported for the first time in this article. It is important to note that the demonstration of chaos using a passive physical memristor is radically different than all the previous reports where memristor emulators were fabricated using opamps or microcontrollers. Replacing memristor emulators with a single passive component, results in the most compact form of chaotic system that has ever been reported and the non-requirement for additional biasing circuitry reduces power consumption. Two different configurations of the chaotic circuit is demonstrated, one being the 3-element chaotic circuit proposed by Muthuswamy and Chua and the other being the 2-element chaotic circuit proposed by Driscoll *et al.* [142].

7.2 Implementation of 3-element Chaotic Circuit

The circuit shown in the inset of Fig. 7.2 was implemented to demonstrate chaotic behavior using 3-element chaotic circuit with one element being a passive physical memristive system. The current through the series circuit can be written as,

$$i = C \frac{dV_C}{dt}$$

Assuming $x(t) \triangleq V_C(t)$ and $y(t) \triangleq i_L(t)$, the above equation can be re-written as,

$$x(t) = \frac{y}{C}$$

We can also write,

$$\frac{di_L}{dt} = \frac{1}{L} \{-V_C + R_M(-i_L)\}$$

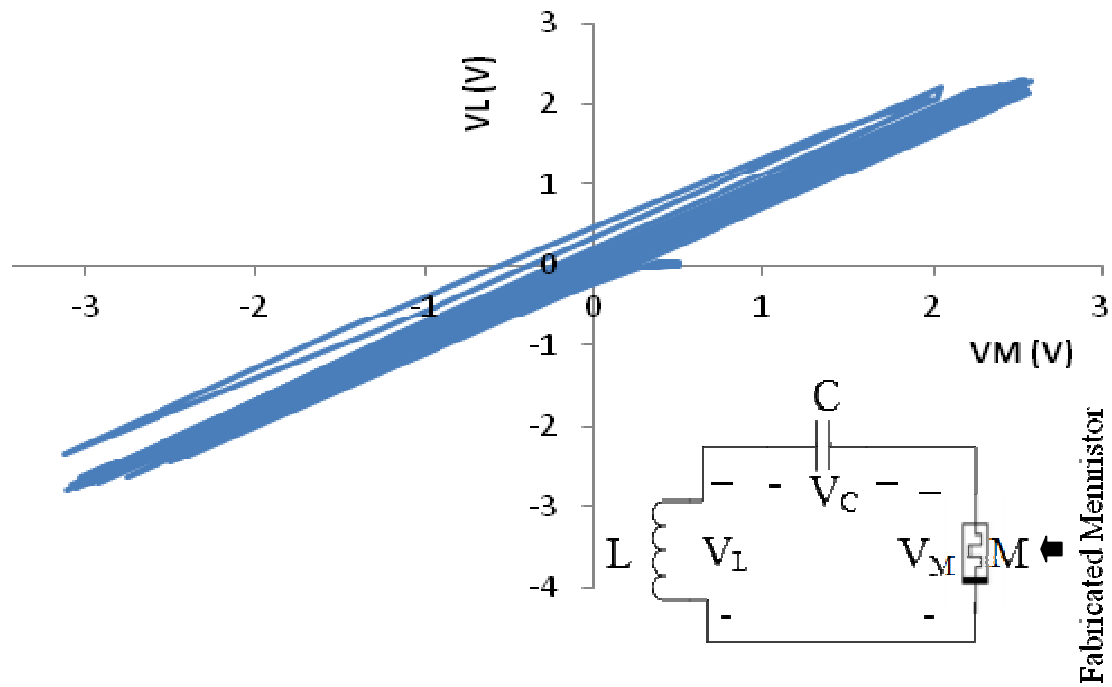


Figure 7.2. Demonstration of chaotic behavior using ZnO nanowire memristors. Inset: the compact chaotic circuit was implemented using all passive components.

That can be expressed as,

$$\dot{y} = -\frac{1}{L}\{x + R_M y\}$$

The third state variable arises by defining an internal state of memristor z such that,

$$R_M = \beta(z^2 - 1)$$

$$\text{and, } \dot{z} = -y - \alpha z + yz$$

where α and β are constants and different values result in diverse chaotic properties.

A sinusoidal voltage source with amplitude 3 V (peak) and frequency 1 kHz was applied across the memristive system M . The threshold voltage required for the memristive system to switch was determined to be ± 2 V and the amplitude of 3 V for the sinusoidal excitation was chosen to ensure continuous switching. A 1 μ F capacitor and a 227 mH inductor were connected in series with the memristor to construct the chaotic circuit. The voltages across the memristive system V_M and the inductor V_L were measured using an Agilent Infiniium 54810A high-speed oscilloscope with 8 GSa/s sampling rate. V_L as a function of V_M is shown in Fig. 7.2 for 100 consecutive cycles. It is to be noted that the memristive system serves two purposes in the circuit: (i) it gives rise to the third state variable required for an autonomous continuous-time system to be chaotic according to the Poincare-Bendixson theorem [172, 176] and (ii) it provides the essential non-linearity for chaotic behavior.

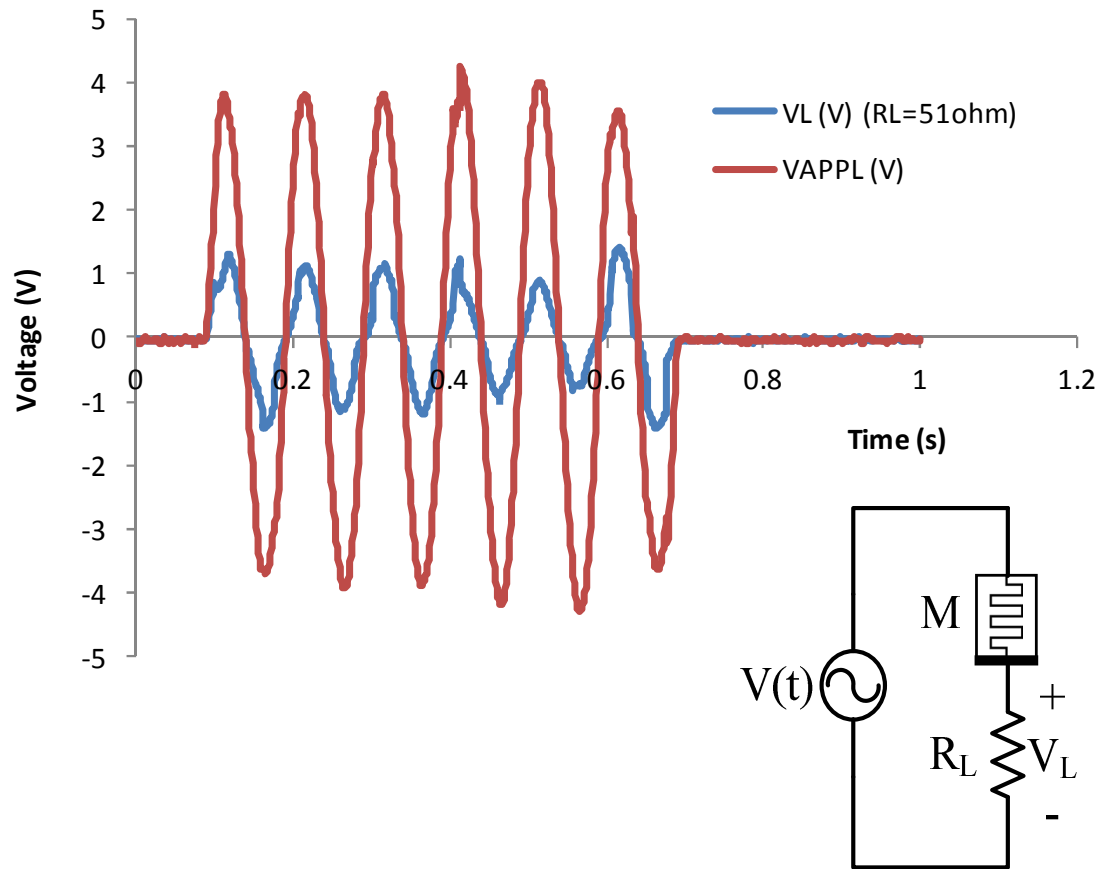


Figure 7.3. Time domain measurement of memristor chaotic behavior. Inset: Schematic of the 2-element chaotic circuit.

7.3 Implementation of 2-element Chaotic Circuit

The inset of Fig. 7.3 shows the setup for a 2-element memristive chaotic system as was proposed by Driscoll *et al.* [142]. The response of memristor, for a sinusoidal excitation $V(t)$ of amplitude 5V(peak) and frequency 10 Hz applied using an Agilent 33120A function generator, was measured for 6 consecutive cycles. A 50 Ω resistor was connected in series with the memristor to measure the current through the memristor. The voltage across the load resistance of 50 Ω , V_L , is representative of the current through the memristor. The memristor showed chaotic response for 6 cycles as can be seen in Fig. 7.3. In order to analyze the time dependence of a dynamic system power spectral density extracted from fast Fourier transform of the time series dynamical variable is often utilized. The power spectral density allows distinguishing between periodic, quasi-periodic, and chaotic regimes. Fig. 7.4 shows the calculated power spectral density of the sinusoidal excitation and the memristor switching characteristics. The power spectrum of the external sinusoidal excitation showed a single fundamental frequency of $\omega_c = 62.77$ rad/s which is expected from the applied 10 Hz sinusoid. On the other hand, the power spectral density of the memristor shows two peaks at $\omega_{m1} = 6.28$ rad/s and $\omega_{m2} = 125.5$ rad/s in addition to a broadband noise. The ω_{m2} frequency is approximately twice the frequency of the external sinusoidal excitation and is attributed to the switching of the memristor between resistive states, HRS and LRS. The memristor switches state during both positive (HRS to LRS switching) and negative half (LRS to HRS switching) of the sinusoid making the switching frequency twice of the sinusoidal excitation. The broadband noise suggests non-periodic chaotic behavior that may arise from stochastic as well as from deterministic processes.

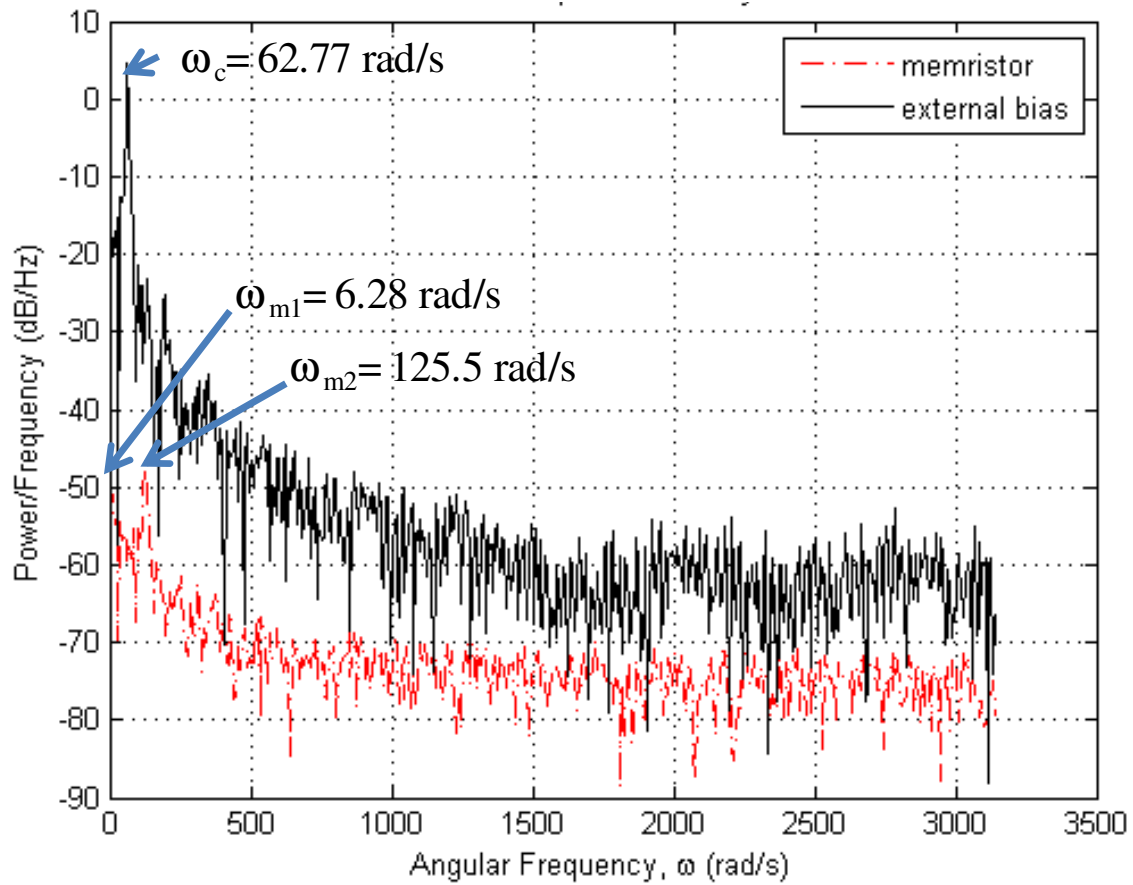


Figure 7.4. Power spectral density of the sinusoidal excitation and the memristor.

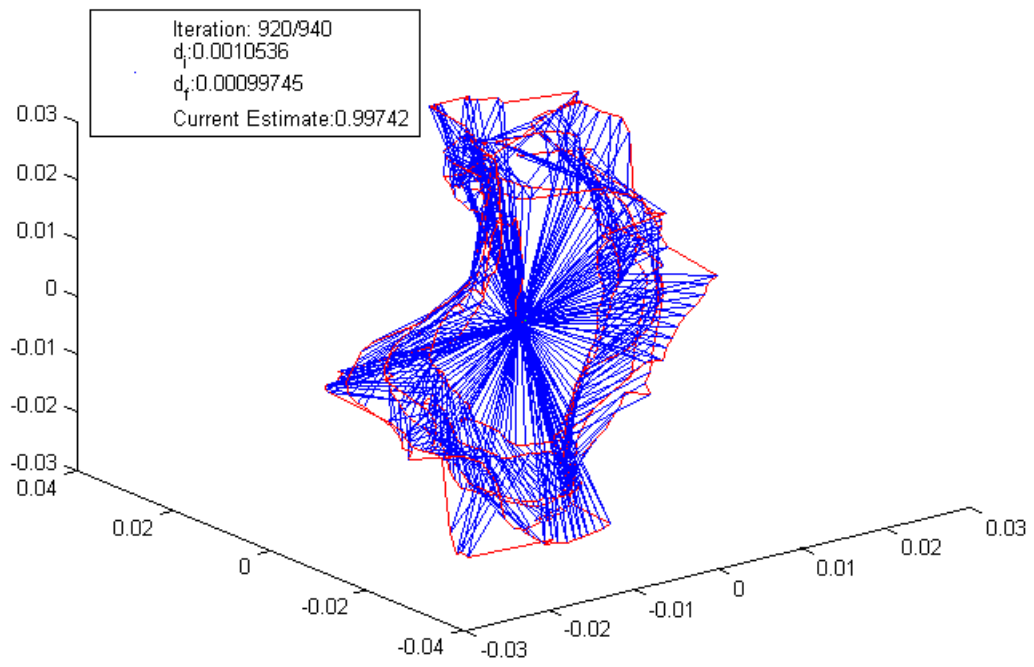


Figure 7.5. Demonstration of chaotic behavior using phase-space trajectories of ZnO nanowire memristors

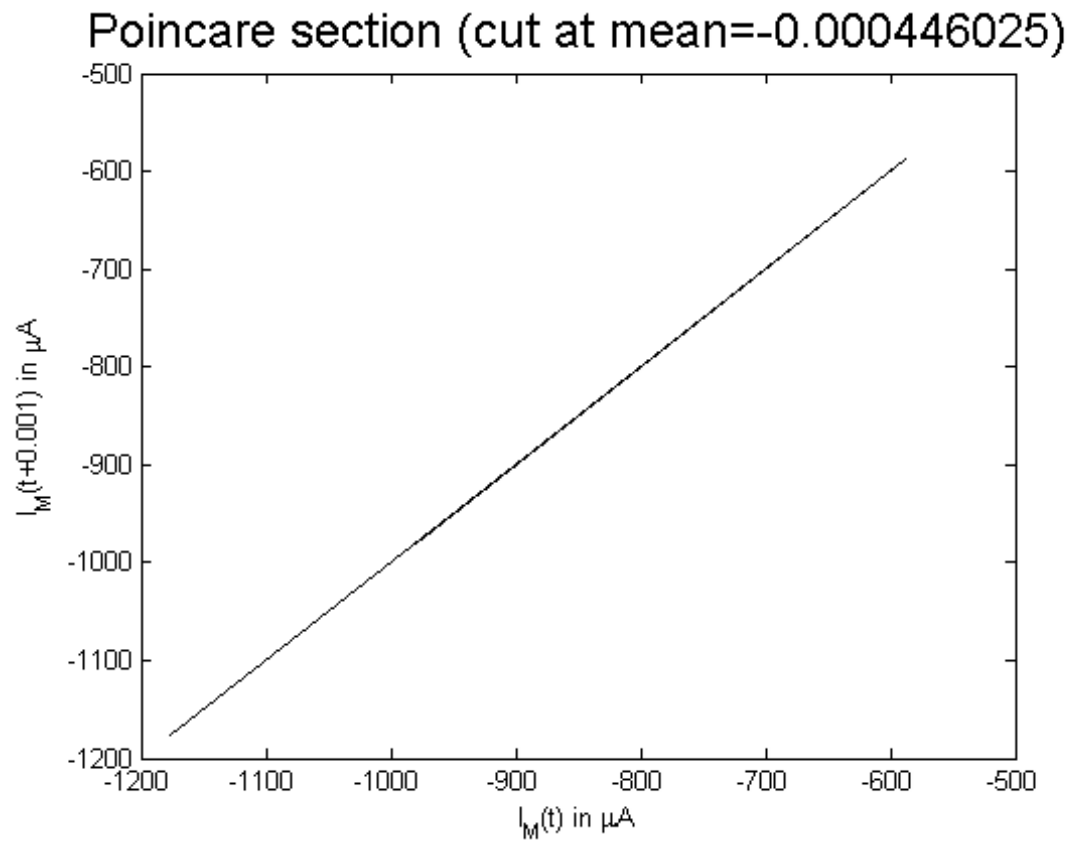


Figure 7.6. A Poincaré section constructed from the intersection of the phase-space trajectories of current through memristor with the plane passing through the mean value of current.

In order to determine if the chaotic behavior is due to a deterministic nonlinear system, trajectories in a multidimensional phase space are analyzed. Each point in the phase-space plot characterizes the entire system at a single instant in time and Lyapunov exponents of the chaotic system is extracted to quantify chaos. The phase-space plot of the memristor based chaotic system is shown in Fig. 7.5 that is calculated from the measured time-series data using the method outlined by Wolf *et al.* [177]. As can be observed, the phase-space trajectory has no single steady orbit and is rather spread over the entire available phase space. Lyapunov exponents provide a quantitative measure of the exponentially fast divergence or convergence of adjacent orbits in the phase space for a dynamical system and is expressed as [142]: $|\delta I_M(t)| \approx e^{\lambda t} |\delta I_M(t_0)|$, where $I_M(t)$ is the time dependent current through the memristor, $I_M(t_0)$ is the initial current through the memristor, and λ is the Lyapunov exponent. The system under test is determined to be chaotic if there exists one or more positive Lyapunov exponents. The maximum calculated Lyapunov exponent for the memristor based chaotic circuit shown in Fig. 7.3 was $\lambda=61.57 \text{ s}^{-1}$ during the 100th evolution of the phase-space trajectory, with a positive value of λ suggesting chaotic behavior of memristor that is classified as “strange” attractor.

One easier alternative to determine a chaotic system is to analyze its Poincaré sections and maps than direct analysis of phase portrait. The concept of Poincaré section was introduced by French mathematician Henri Poincaré, who was dubbed the “last universalist” – a person who is at ease in all branches of mathematics – by E.T. Bell. A Poincaré section is constructed from the intersection points of positively directed orbits

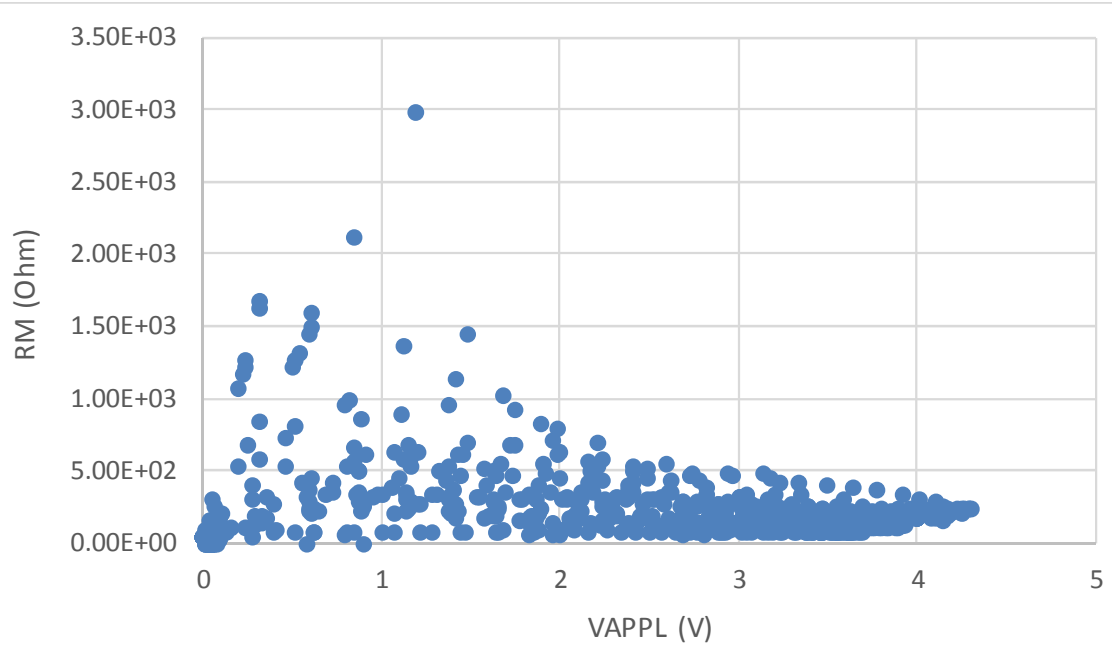


Figure 7.7. Experimentally measured memristance as a function of applied bias. Small changes in V_{APPL} results in significant change in memristance suggesting chaotic behavior.

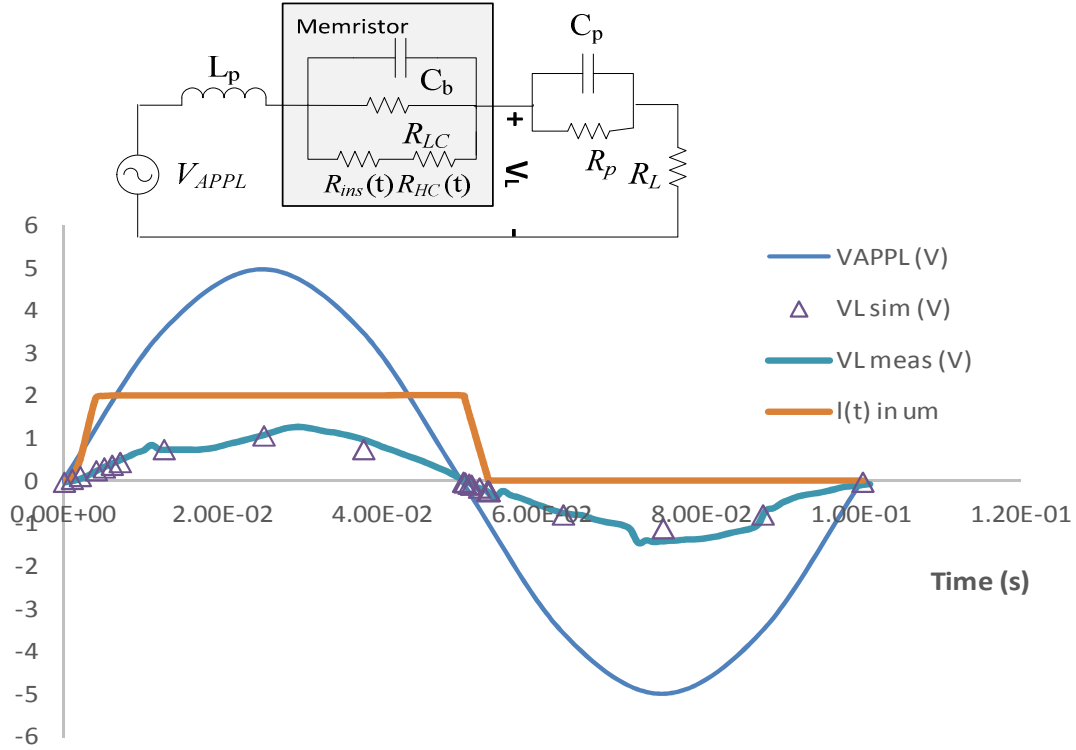


Figure 7.8. Measured and simulated load voltage, V_L as a function of time. Formation and rupture of filament as a function of time is also shown. Inset: memristor circuit model used for simulation [107].

with a $(m-1)$ -dimensional hypersurface, where m is the number of dimensions of the phase portrait. For the three-dimensional phase-space trajectory shown in Fig. 7.5, Poincaré cut is a two-dimensional plane. The intersection of the continuous-time orbits with the Poincaré cut plane constructs discrete-time data points. For a non-chaotic periodic system, Poincaré cut produces a point, or is zero dimensional. Fig. 7.6 shows a Poincaré section constructed for the three-dimensional phase-space trajectories shown in Fig. 7.5. The linear characteristic of Poincaré section suggests that the orbits for this chaotic attractor lies essentially along a sheet and hence the system is deterministic, i.e. each value of $I_M(t)$ gives a single valued $I_M(t+1)$.

Fig. 7.7 shows a scatter plot of memristance as a function of applied bias. The memristance value changes widely for a small change in applied bias suggesting chaotic behavior of the memristor. It is to be noted that the percentage change in memristance from the current experiment is calculated 43,000% which is 240 times higher than the reported variations by Driscoll *et al.* It can also be noticed that the variation is greater for smaller bias voltages while it is smaller for applied voltages higher than 2V as the probability of the memristor to switch to LRS is higher above 2V.

In order to determine the origin of the chaos the memristor based chaotic circuit was simulated using the model outlined by Mazady and Anwar [76, 107]. It is well known that the formation and rupture of conductive filaments give rise to the observed switching characteristics of memristors. R_{HC} and R_{ins} represent the resistance of the high conductivity filaments and the resistance of the insulating material in between the

filament and anode, respectively. Both R_{HC} and R_{ins} are time dependent owing to the time dependent change of filament length. Bulk capacitance C_b equals 6.5×10^{-19} F for a dielectric constant of 2.08 for the ZnO NWs. Parasitic resistance due to the cables and contact resistances are lumped in R_p and equals 7 k Ω . C_p and L_p represent the parasitic capacitance and inductance, respectively. The time dependent length of the filaments calculated using [76] is shown in Fig. 7.8. At the onset of the positive half of the sinusoidal applied bias the high conductivity filaments starts to grow from the cathode towards the anode. At $t=6\text{ms}$ and for $V_{APPL}=1.84\text{V}$, the formation of the filaments complete as they reach the anode electrode and the memristor switches on LRS. For the rest of the positive half of the applied bias the filament remains intact and the device remains in LRS. At the negative half of V_{APPL} the conductive filaments start to rupture and the filament length becomes zero at $t=53\text{ms}$ switching the device to HRS. The current through memristor is calculated using the circuit model shown in the inset of Fig. 7.8. The voltage across the load resistance V_L , which is representative of the current through memristor, is shown in Fig. 7.8 as a function of time. Comparison of the simulated V_L with the measured values shows excellent agreement. The nonlinearity and the associated chaos in memristor based circuit are thus understood to arise from the nonlinear dynamics of filament formation and rupture inside memristors. The model considers a very simplistic case of cylindrical filament formation which is more convoluted in experimental devices. For example, the location of filaments in the device in subsequent sweeps, mobility variations at the center of the filaments and at the surface, filaments branching out to dendrites, conical shapes of filaments with larger diameter at the cathode and smaller diameter at the anode, filaments winding to give rise to

inductance, hopping conduction between filament fragments, among others, play significant role in nonlinear carrier dynamics of memristors.

7.4 Conclusion

Experimental demonstration of chaotic circuit employing inherent nonlinearity of a fabricated memristor has been shown. The fabricated memristor replaces a number of components, such as opamps and microcontrollers, and reduces power consumption than the earlier reports. The two-element chaotic circuit employing only a memristor and a series resistor is the most compact form of chaotic circuit that has ever been reported. Chaotic attractor was constructed from measured time-series data to verify the nature of chaos that suggests Lyapunov exponent of 61.57 s^{-1} . The origin of chaos in memristors is believed to be the high nonlinearity and randomness in filament formation and rupture inside memristors.

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PUBLICATIONS

Refereed Journal Publications

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- [3] **Anas Mazady**, Abdiel Rivera, and Mehdi Anwar, "Optical Parameters of $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ Nanowires in THz Regime", *Solid State Electronics*, vol. 101, pp. 8-12, Nov 2014. DOI: 10.1016/j.sse.2014.06.019.
- [4] Abdiel Rivera, **Anas Mazady**, and Mehdi Anwar, "Co-axial Core-Shell ZnMgO/ZnO Nanowires", *Solid State Electronics*, Sep 16, 2014. DOI: 10.1016/j.sse.2014.08.010.
- [5] Hung Chi Chou, **Anas Mazady**, John Zeller, Tariq Manzur, and Mehdi Anwar, "Room Temperature Quantum Cascade Laser: $\text{ZnO}/\text{Zn}_{1-x}\text{Mg}_x\text{O}$ versus $\text{GaN}/\text{Al}_x\text{Ga}_{1-x}\text{N}$ ", *J. Electron. Mater.*, vol. 42, no. 5, pp 882-888, May 2013.
- [6] **Anas Mazady** and Mehdi Anwar, "Bipolar Resistive Switching Transients in ZnO Nanowire Memristors", *IEEE Trans. Nanotechnology* (under review).
- [7] **Anas Mazady**, Md. Tauhidur Rahman, Domenic Forte, and Mehdi Anwar, "Memristor Nano-PUF - A Security Primitive: Theory and Experiment", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* (under review).
- [8] Abdiel Rivera, **Anas Mazady**, and Mehdi Anwar, "MOCVD Assisted Growth and Characterization of $\text{Zn}_{1-x}\text{Mg}_x\text{O}$ NWs on p-Si", *Appl. Phys. Lett.* (under review).
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- [10] **Anas Mazady** and Mehdi Anwar, "Transient Circuit Model of Memristors", *International Journal of High Speed Electronics and Systems* (under review).
- [11] Abdiel Rivera, **Anas Mazady** and Mehdi Anwar, " ZnMgO/ZnO Core-Shell Structures for Gas Sensing", *International Journal of High Speed Electronics and Systems* (under review).
- [12] Abdiel Rivera, **Anas Mazady** and Mehdi Anwar, "Optimized Growth of ZnO Nanowires using MOCVD", *International Journal of High Speed Electronics and Systems* (under review).
- [13] Abdiel Rivera, **Anas Mazady** and Mehdi Anwar, "Energy Harvesting Leveraging Piezoelectric Property of ZnO Nanorods," *International Journal of High Speed Electronics and Systems* (under review).

- [14] **Anas Mazady**, Abdiel Rivera, and Mehdi Anwar, "Zn_{1-x}Mg_xO-based Deep-Ultraviolet Solar Blind Detector", *ACS Nano* (*in preparation*).
- [15] **Anas Mazady**, Hung Chi Chou, John Zeller, Mohammad Tehranipoor, and Mehdi Anwar, "Counterfeit IC Detection Using THz Spectroscopy", *IEEE Trans. Components, Packaging, and Manufacturing Technology* (*in preparation*).
- [16] **Anas Mazady** and Mehdi Anwar, "Implication Logic Implementation Using ZnO Nanowire Memristors," (*in preparation*).
- [17] **Anas Mazady** and Mehdi Anwar, "Experimental Realization of Chaotic Circuits Using Physical Passive Memristive Systems," (*in preparation*).

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- [1] **Anas Mazady**, Abdiel Rivera, and Mehdi Anwar, "Effects of Annealing on Structural and Optical Properties of ZnO Nanowires", *Proc. MRS 2014*, vol. 1675.
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Book Chapter

- [1] Hung Chi Chou, John Zeller, **Anas Mazady**, and Mehdi Anwar, "Wide-Bandgap Semiconductor Quantum Cascade Lasers Operating at Terahertz Frequencies", *The Wonder of Nanotechnology: Quantum Optoelectronic Devices and Applications*, SPIE Press 2013.

Conference Presentations

- [1] **Anas Mazady**, Abdiel Rivera, Mohammad Tehranipoor, and Mehdi Anwar, "Multi-level Authentication Platform Using Electronic Nano-Signatures", *Int. Conf. on Lasers, Optics, and Photonics*, Philadelphia, Sep 8-10, 2014.
- [2] Abdiel Rivera, **Anas Mazady**, and Mehdi Anwar, "Comparison of ZnMgO/ZnO Core-Shell Structures with ZnO Nanorods for UV Detection", *Int. Conf. on Lasers, Optics, and Photonics*, Philadelphia, Sep 8-10, 2014.
- [3] **Anas Mazady**, Abdiel Rivera, and Mehdi Anwar, "Effects of Annealing on Structural and Optical Properties of ZnO Nanowires", *Materials Research Society (MRS) Spring Meeting & Exhibit*, San Francisco, CA, April 21-25, 2014.
- [4] **Anas Mazady**, Abdiel Rivera, and Mehdi Anwar, "Optimization of Annealing Conditions for ZnO-based Thin Films Grown Using MOCVD", *Materials Research Society (MRS) Spring Meeting & Exhibit*, San Francisco, CA, April 21-25, 2014.
- [5] Abdiel Rivera, **Anas Mazady**, and Mehdi Anwar, "Low Temperature Growth of Horizontal ZnO Nanorods", *Materials Research Society (MRS) Spring Meeting & Exhibit*, San Francisco, CA, April 21-25, 2014.
- [6] **Anas Mazady**, Abdiel Rivera, and Mehdi Anwar, "DC Circuit Model of TiO₂-based Memristors", *Connecticut Microelectronics and Optoelectronics Consortium (CMOC) Symposium*, Storrs, CT, April 9, 2014.
- [7] **Anas Mazady**, Abdiel Rivera, and Mehdi Anwar, "THz Properties of Zn_{1-x}Mg_xO Nanowires", *Connecticut Microelectronics and Optoelectronics Consortium (CMOC) Symposium*, Storrs, CT, April 9, 2014.
- [8] **Anas Mazady**, Abdiel Rivera, and Mehdi Anwar, "Transient Circuit Model of Memristors", *Connecticut Microelectronics and Optoelectronics Consortium (CMOC) Symposium*, Storrs, CT, April 9, 2014.
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