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# Indium Gallium Arsenide Three-State and Non-Volatile Memory Quantum Dot Devices

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# **Abstract**

## **Indium Gallium Arsenide Three-State and Non-Volatile Memory Quantum Dot Devices**

Pik Yiu Chan, Ph.D.

University of Connecticut, 2014

With the silicon technology reaching the end of the Roadmap soon, III-V devices have been researched as possible replacements for silicon. Indium gallium arsenide (InGaAs) is particularly appealing due to its well-established processing protocols in high-speed and high-frequency applications.

This dissertation investigates various metal-oxide-semiconductor (MOS) devices using InGaAs as the substrate material. II-VI gate dielectric stacks consisting of ZnSe, ZnS and ZnMgS were used in this research as an alternative to conventional oxide-based gate insulators for InGaAs devices. II-VI gate dielectric materials have been chosen due to their high  $\kappa$  values, wider band gaps and similar lattice constants to InGaAs for a lattice-matched semiconductor-insulator interface.

Multi-state field-effect transistors were also fabricated incorporating germanium-oxide-cladded germanium quantum dots (QDs) at the gate regions. These QDs have the

ability to store charges and providing an additional output state (in addition to the ON and the OFF states). Such QDs can also be used as charge storage centers in non-volatile memory devices, which were also investigated. Integration of quantum well channels in the substrate is another method to provide multi-bit operations, which is discussed in the dissertation.

Fabrication process flows, experimental results and modeling simulations of the different fabricated devices are also presented. A look at multi-value logic applications and the future of InGaAs devices are included.

Indium Gallium Arsenide Three-State and  
Non-Volatile Memory Quantum Dot Devices

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2014

APPROVAL PAGE

Doctor of Philosophy Dissertation

Indium Gallium Arsenide Three-State and Non-Volatile Memory

Quantum Dot Devices

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# 1. Introduction

## 1.1. *Transistor Scaling and Implications*

The semiconductor industry follows Moore's Law, which predicts the size of metal-oxide-semiconductor (MOS) devices to shrink by 50% every 18-24 months [1]. The law also predicts the increases in switching speed and logic density, and the reductions in power dissipation and production costs. As the transistor size reduces, every design parameter of the transistor will need to shrink to facilitate the performance changes, for example, gate dielectric thickness ( $t_{ox}$ ) and supply voltage ( $V_{DD}$ ).

To optimize transistor performance, scaling needs to maximize the on-state current ( $I_{on}$ ), but at the same time minimize the off-state current ( $I_{off}$ ) [2]. The switching frequency is directly proportional to  $I_{on}$  but inversely proportional to  $V_{DD}$ . We can also look at scaling from the power dissipation point of view. Power dissipation is the sum of the dynamic power consumption (directly proportional to  $I_{on}$ ) and the static power consumption (due to off-state leakage current).

If the industry is to follow Moore's Law in the sub-22nm silicon technology, the silicon dioxide gate thickness,  $t_{ox}$ , will be less than 20Å [3], and this could cause severe leakage current and increase off-state power consumption. There are various mechanisms that cause current leakage in a transistor. The first component of leakage

current is gate oxide tunneling in the device [4-8]. If the gate insulator becomes too thin, leakage current would increase due to Fowler-Nordheim tunneling and direct tunneling.

Another component that leads to current leakage is subthreshold conduction, which is pronounced in the weak inversion regime at low gate voltages [4-9]. The subthreshold current decreases with increasing threshold voltage ( $V_{TH}$ ) [5], but a result of device scaling is the decrease in  $V_{TH}$ . This increases the device off-state current, thus increasing the static power of the device.

There are other mechanisms that cause current leakage, such as band-to-band tunneling [10-11], gate-induced drain leakage [12] and punch-through [8], but gate tunneling and subthreshold conduction have become more important due to device scaling. The total  $I_{off}$  is given by the sum of all the above leakage currents. The higher the  $I_{off}$ , the higher the static power dissipation.

Dynamic power consumption, on the other hand, is a function of the square of the supply voltage  $V_{DD}$  [2]. An obvious solution to reducing the dynamic power dissipation would then be to reduce  $V_{DD}$  [11, 13]. However, one problem with this solution is that  $V_{TH}$  of the device would also be reduced, and as mentioned before, subthreshold current would increase as a result [14], causing static power consumption to increase.

Device scaling leads to higher clock frequency, but since dynamic power dissipation also increases with the switching speed [2], this leads to more heat generation

[14]. Heat is also generated in memory devices as they are being written and erased, causing electrons to flow in the circuits, building up capacitance in the devices and the interconnects [15]. High operating temperature can affect threshold voltage and subthreshold conduction, and heat removal has to accompany device scaling to ensure proper device operation [16-17]. As transistor size reduces, the packing density of transistors on the wafer increases. Power dissipation for logic chips has reached 100 W/cm<sup>2</sup> [11, 18-19], and this may become the limiting factor of device scaling.

## ***1.2. Dissertation Outline***

Because of the imminent end of the silicon technology on the Roadmap, researchers have been looking for alternatives to continue device scaling. This dissertation research explores the use of indium gallium arsenide (InGaAs) material with lattice-matched gate dielectric consists of II-VI materials as an alternative.

Chapter 2 explores options for replacing silicon and presents the competitiveness of InGaAs in this race. II-VI gate dielectric is introduced as a possible candidate for InGaAs FETs, and possibilities for multi-state capability are discussed.

Chapter 3 explains the theory behind three-state behavior in quantum-dot-gate field-effect transistors (QDG-FET).

Chapter 4 discusses the options and theory behind non-volatile memory devices that use quantum dots as the floating gate.

Chapter 5 focuses on the spatial wavefunction switching behavior in multi-quantum-well substrate, and how this phenomenon can be used for multi-bit logic applications.

Chapter 6 presents the device fabrication of the research, which includes the fabrication of InGaAs non-volatile memory devices and QDG-FETs. Detailed process flow is included.

Chapter 7 discusses the gate materials that were used in this research: the II-VI gate dielectric stack and the  $\text{GeO}_x$ -cladded Ge quantum dots.

Chapter 8 presents the experimental results for the fabricated devices including two types of metal-oxide-semiconductor (MOS) capacitors and InGaAs QDG-FET showing three-state output behaviors.

Chapter 9 focuses on the modeling simulations to compare with the experimental results. The model theory is presented, along with simulation results for the various fabricated devices. This chapter also discusses the application of InGaAs FETs in multi-bit logic applications.

Chapter 10 discusses the viability of InGaAs FETs in the future CMOS development, and how it can be incorporated fully into the current technology.

Chapter 11 concludes the dissertation with a summary and presents ideas for future work and improvement for the project.

## 2. Indium Gallium Arsenide and II-VI Materials

### 2.1. *What are our Options?*

Any further reduction in silicon dioxide gate thickness will only degrade the performance of the transistors, and there has to be an alternative to increasing the switching frequency without increasing the power density on the wafer.

A replacement for silicon dioxide has to be able to withstand scaling without causing too much gate leakage. Researchers have turned to high- $\kappa$  dielectric materials to look for suitable candidates. High- $\kappa$  materials have higher dielectric constants, allowing for a thicker dielectric layer than silicon dioxide for the same current density. The equivalent oxide thickness (EOT) for a high- $\kappa$  material is given by Equation (2-1):

$$EOT = T_{\kappa} \frac{\epsilon_{ox}}{\epsilon_{\kappa}} \quad (2-1)$$

where  $T_{\kappa}$  is the thickness of the high- $\kappa$  dielectric, and  $\epsilon_{ox}$  and  $\epsilon_{\kappa}$  are the dielectric constants for silicon dioxide and the high- $\kappa$  dielectric respectively.

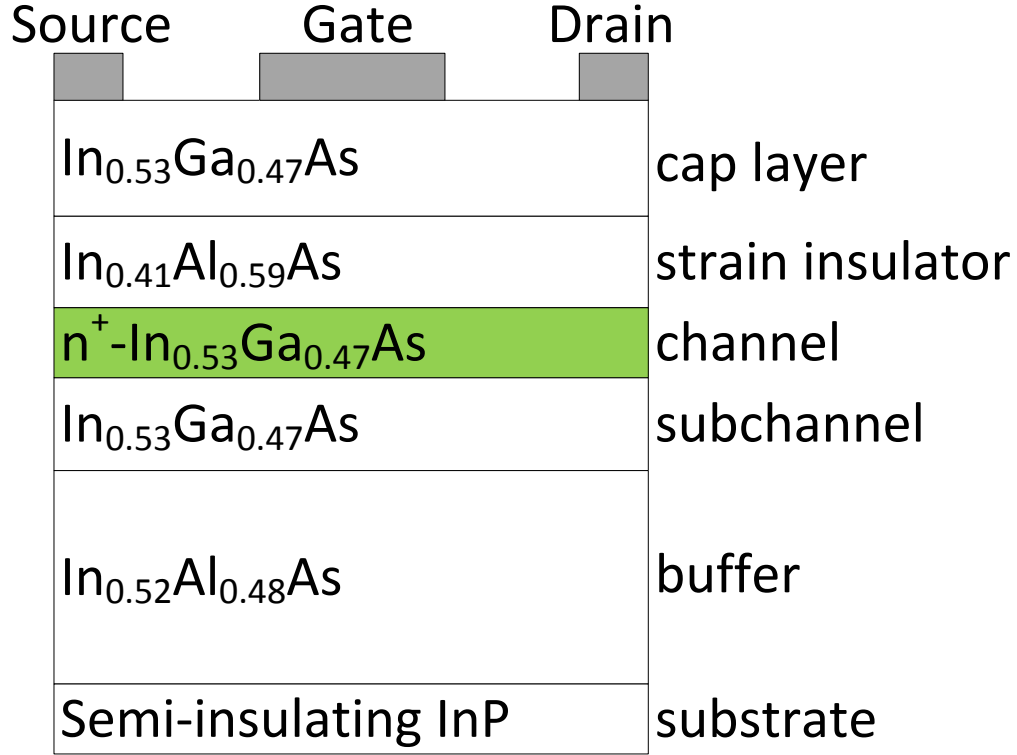
To increase the switching speed without causing too much power dissipation, an alternative is to use a semiconductor material with much higher charge carrier velocities than that for silicon. An obvious choice is III-V compound semiconductors [14, 18-19].

They have been used in high-speed, high-frequency, and high-power transistor devices for a long time. In fact, InGaAs high-electron-mobility transistors (HEMTs) are one of the fastest transistors on the market.

## **2.2.        *Why InGaAs?***

InGaAs, due to its light effective electron mass [20], has an electron mobility that is more than ten times than that for silicon for comparable carrier sheet density [18]. The III-V HEMT industry is also very mature, which makes using InGaAs as the channel material even more appealing.

Figure 2.2-1 shows a basic structure of an InGaAs HEMT [21]. What makes a HEMT appealing is that the electron channel is undoped, which prevents electrons from slowing down due to dopant impurity scattering in the channel. III-V HEMTs usually have very good electrical performance such as high  $I_{on}$ , but the lack of gate dielectric causes HEMTs to have large vertical Schottky gate leakage [22]. To develop III-V technology to replace silicon on the Roadmap, good gate dielectrics for InGaAs and other III-V materials are required.



**Figure 2.2-1: Basic structure of an InGaAs HEMT [21].**

### 2.3. *High- $\kappa$ Gate Dielectric Options*

One of the reasons why silicon is such a superior semiconductor material is because of its native oxide, silicon dioxide. First of all, silicon oxide is very easy to grow thermally. Secondly, the interface between silicon and silicon dioxide is almost perfect. III-V semiconductors, on the other hand, are not so lucky. When InGaAs is exposed to oxygen, a variety of native oxide species and elemental group V species will appear at the surface [23-25]. Such species may include As<sub>2</sub>O<sub>3</sub>, As<sub>2</sub>O<sub>5</sub>, Ga<sub>2</sub>O<sub>3</sub>, Ga<sub>2</sub>O, In<sub>2</sub>O<sub>3</sub>, In<sub>2</sub>O, GaAsO<sub>4</sub>, InAsO<sub>4</sub>, As-As dimers, and As and Ga anti-sites. At the interface of InGaAs



and the oxide layer, interface states usually form inside the forbidden band gap, causing the Fermi level to be pinned at the surface state energy and affecting the modulation of the Fermi level [26-28]. However, several researchers have reported that  $\text{Ga}_2\text{O}_3$  deposited *in situ* on GaAs substrates have shown unpinning of the Fermi level [18, 29].

Oxide-based insulators deposited by atomic layer deposition (ALD) as the gate material are also popular choices [30-33]. It is found that the ALD method seems to remove the surface oxide, and the surface oxide does not return during the ALD oxide deposition [18]. In fact,  $\text{Al}_2\text{O}_3$  deposited by the ALD method has shown good  $I_{on}$  but the  $I_{off}$  remains high [34]. The interface traps are still present at the InGaAs- $\text{Al}_2\text{O}_3$  interface. Interface states that are present below the conduction band affect the subthreshold swing, affecting  $I_{on}$  of the device [18], while those present inside the conduction band trap electrons, causing a shift in the threshold voltage. Sometimes the worsened  $I_{off}$  is due to device processing. Most InGaAs and III-V MOSFETs use ion implantation to form the source and drain regions, and post-implantation high-temperature activation and annealing are required. However, the volatile group V elements would be affected by this high temperature, causing more bulk defects and junction leakage [34].

In addition to affecting Fermi level modulation, interface-state induced Coulombic scattering and interface roughness can also reduce channel mobility, which is a big selling point of III-V materials [18, 35-36]. To avoid this degradation, researchers are exploring InGaAs MOSFETs that have a buried active channel, instead of the conventional surface channel [13, 18, 37-43]. These buried-channel devices are usually

called quantum-well field-effect transistors (QW-FETs), and they have a wider-bandgap III-V barrier layer between the buried channel and the gate dielectric stack. The barrier diminishes the effects from the oxide interface states, confines the charge carriers and lessens the leakage current [13, 18].

As good as this sounds, there are some drawbacks to using a buried channel. Because of the barrier layer, the active channel is further away from the gate, reducing the gate electrostatic control over the channel [25, 44]. Also, to reduce short-channel effect, the barrier composite has to be made very thin, which may not be able to avoid the effects from the interface states [18].

Comparisons have been made between surface-channel and buried-channel MOSFETs. Carrier mobility in surface-channel devices is degraded, but buried channel devices have worse  $I_{off}$  [35-36]. In surface-channel devices,  $\text{Al}_2\text{O}_3$  is usually used as the gate oxide [45-46].

In this research, we are using high- $\kappa$  II-VI materials that are lattice-matched to the InGaAs material to serve as the gate insulator for MOS devices [47-54]. The II-VI gate dielectric stacks used have a  $\kappa$  value greater than 8. With  $\kappa$  for silicon dioxide being 3.9, according to Equation (2-1), the thickness of our II-VI gate dielectric stack can be made twice as thick as  $\text{SiO}_2$  to have the same drain current density. The drain current,  $I_{DS}$ , of a transistor is given by Equation (2-2):

$$I_{DS} = \frac{W}{L} \mu_n C_{ins} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) \cdot V_{DS} \quad (2-2)$$

where  $W$  and  $L$  are the channel width and length of the transistor,  $\mu_n$  is the electron mobility,  $C_{ins}$  is the insulator capacitance,  $V_{GS}$  is the gate-to-source voltage, and  $V_{DS}$  is the drain-to-source voltage.

The insulator capacitance,  $C_{ins}$ , is given by Equation (2-3):

$$C_{ins} = \frac{\epsilon_o \kappa A}{t} \quad (2-3)$$

where  $\epsilon_o$  is the free-space permittivity,  $\kappa$  is the dielectric constant of the insulator,  $A$  is the area, and  $t$  is the thickness of the dielectric.

Looking at Equations (2-2) and (2-3), we can see that using a II-VI gate stack that is twice as thick than silicon dioxide can still give the same  $C_{ins}$ , and it will not affect the drain current and thus the speed of the transistors. A thicker II-VI gate dielectric can reduce the leakage current and the off-power of the transistor device.

Since the II-VI gate dielectric stack is lattice-matched to the InGaAs channel, the interface state density between the dielectric and the channel will be reduced, and the channel carrier mobility will not be degraded as much. Also, the reduction in interface

traps will also reduce trapped interface charges, and so there will be less fluctuation in the device threshold voltage.

The  $\kappa$  value of the II-VI gate dielectric stack used is comparable to the range of value for  $\text{Al}_2\text{O}_3$ , which is between 8 and 9 [31, 36].

#### **2.4. *Incorporation of Quantum Dots in the Business***

As it was mentioned before, reduction in transistor size leads to an increase in the packing density of transistors on the wafer. More transistors means the storage or bits per unit area will increase. In addition to reducing the size of the transistor, a novel way to increase the logic density on a wafer is by developing field-effect transistors (FETs) that can procure several output states. One way to accomplishing this is to use quantum dots (QDs) at the gate region to manipulate the device threshold voltage. When electrons tunnel from the inversion channel into the QDs, their presence in the QDs will vary the output characteristic in such a way that an additional output state is generated. With three distinct states per transistor, it is possible to increase the number of bits per unit area while keeping the same number of transistors per unit area without increasing the power dissipated, thus maintaining the amount of generated heat in the system.

If there is a control gate dielectric present, the electrons will be trapped in the QDs, and the device can act as a nonvolatile memory device. Our group has demonstrated the use of silicon and germanium quantum dots (QDs) in different applications [47, 55-57]. These QDs, unlike those presented elsewhere [58], are cladded by their native oxides. These oxide claddings insulate the QDs from each other in a closely-packed setting. These QDs site-specifically self-assemble themselves over the  $p$ -type gate region in an FET. Our research has shown that these individually cladded QDs can be vessels for storing charges [49, 55-57].

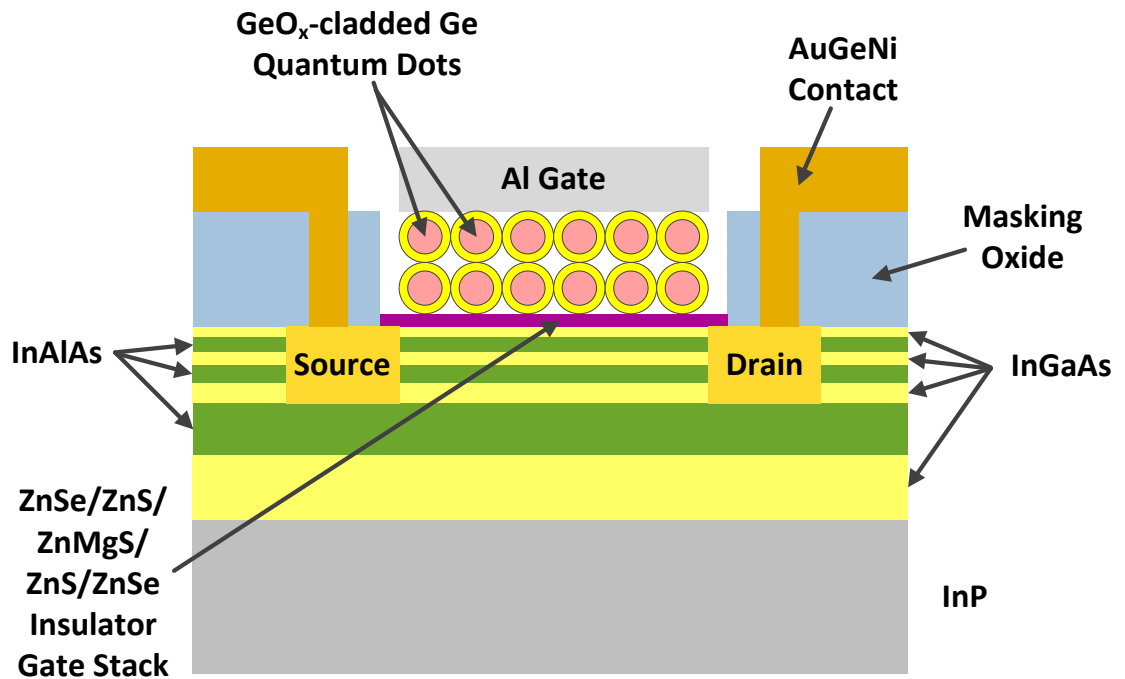
## **2.5. *Quantum Well Channels in Multiple-State Operation***

Another interesting way of creating multiple states in one transistor is to incorporate quantum well channels in the device substrate. As electrons migrate into the lower, and then the upper, transport channels under the gate region, the output current will change accordingly, and it is possible to assign logic states depending on which of these transport channels are “active”, or have electron carriers present. This phenomenon is called the spatial wavefunction switching (SWS) effect, and was developed by Jain, et al. [59-60].

### 3. Theory of Three-State Behavior in InGaAs

#### Quantum-Dot-Gate (QDG) FETs

Figure 3-1 shows a cross-sectional structure of an InGaAs QDG-FET.

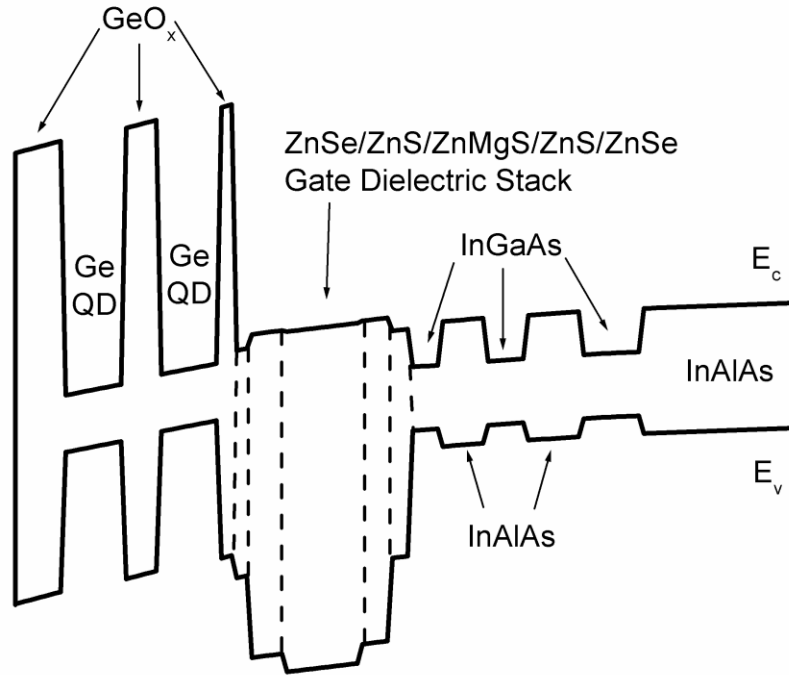


**Figure 3-1: Cross-sectional structure of an InGaAs QDG-FET.**

The “bulk” InGaAs substrate consists of three InGaAs quantum well channels sandwiched between the wider-bandgap InAlAs barriers. This heterostructure epitaxy is deposited on an InP substrate. The gate dielectric stack used in this FET is a combination

of ZnSe, ZnS and ZnMgS, and germanium oxide-cladded germanium quantum dots self-assemble in the gate region.

Figure 3-2 shows the band diagram of this InGaAs QDG-FET.



**Figure 3-2: Band diagram of an InGaAs QDG-FET.**

When the gate voltage,  $V_{GS}$ , increases, electrons from the inversion channel tunnel through the gate dielectric stack into the lower QD layer situating right above the tunnel gate insulator. As  $V_{GS}$  becomes more positive, the electrons in the lower QD layer tunnel into the next QD layer that is closer to the gate electrode. The tunneling rate for electrons from the channel to the quantum dots,  $R_{te}$ , is given by Equation (3-1) [59]:

$$R_{te}|_c^d = \frac{4\pi}{\hbar} \sum_{c,d} |\langle \psi_d | H_t | \psi_c \rangle|^2 (f_c - f_d) \delta(E_d - E_c) \quad (3-1)$$

In the equation, the subscripts  $c$  and  $d$  represent the inversion channel and the quantum dot respectively.  $\psi$ ,  $f$ , and  $E$  represent the wavefunction, Fermi distribution and energy level respectively.  $H_t$  is the Hamiltonian.

The threshold voltage,  $V_{TH}$ , of the QDG-FET will also adjust as electrons tunnel into the quantum dot layers. The change in the threshold voltage,  $\Delta V_{TH}$ , is calculated according to Equation (3-2):

$$\Delta V_{TH} = -\frac{\Delta Q}{C_{ox,eff}} \quad (3-2)$$

The effective oxide capacitance,  $C_{ox,eff}$ , changes depending on whether the electrons are in the inversion channel, the lower QD layer or the upper QD layer. In Equation (3-2), the change in charge in the gate region,  $\Delta Q$ , depends on the electron charge ( $q$ ), the charge in each QD ( $n_{qd}$ ), the number of QDs in the layers ( $N_{qd}$ ), the distance the QD layer is from the gate ( $t_{qd}$ ), and the distance of the gate insulator from the gate ( $t_g$ ). The relationship is shown in Equation (3-3), with the subscripts 1 and 2 indicate the lower and upper QD layers respectively:

$$\Delta Q = q \left( \sum \frac{t_{qd1} n_{qd1} N_{qd1}}{t_g} + \sum \frac{t_{qd2} n_{qd2} N_{qd2}}{t_g} \right) \quad (3-3)$$



As the gate voltage increases, more electrons are found at the inversion channel under the gate material, and this increases the tunneling rate of the electrons into the QDs. This in turn increases the electron charges in the QDs, given by the product of  $n_{QD}$  and  $N_{QD}$  in Equation (3-3), which subsequently increases  $\Delta V_{TH}$  in Equation (3-2).

Behaving the same way as a regular FET, the drain current,  $I_{DS}$ , of a QDG-FET increases as a function of the drain voltage,  $V_{DS}$ , according to Equation (3-4):

$$I_{DS} = \left(\frac{W}{L}\right) \mu_n C_{ox,eff} \left\{ [V_{GS} - (V_{TH} + \Delta V_{TH})] V_{DS} - \frac{V_{DS}^2}{2} \right\} \quad (3-4)$$

where  $W$  and  $L$  are the channel width and length of the device, and  $\mu_n$  is the electron mobility.

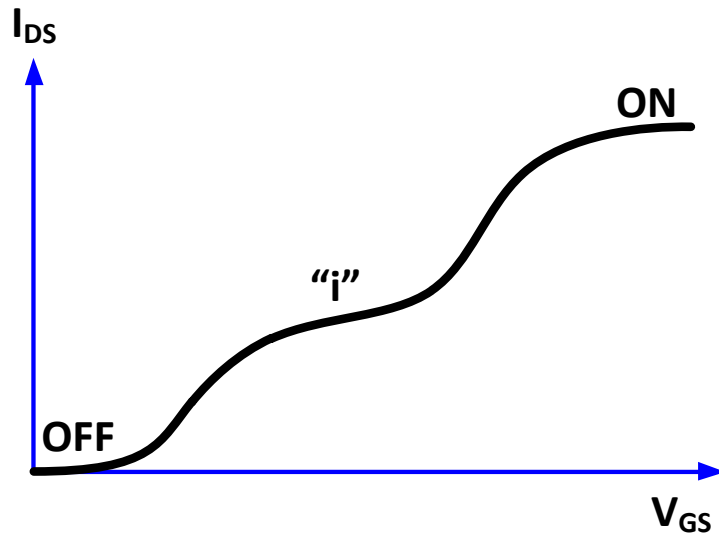
As previously described, as  $V_{GS}$  increases, electrons migrate from the channel to the quantum dot layers, and this also increases  $V_{TH}$ . This continues to happen as long as the electrons continue to tunnel from the inversion channel into the QD layers, and the increase in  $V_{GS}$  approximately cancels out the change in  $V_{TH}$ , and the term  $V_{GS} - (V_{TH} + \Delta V_{TH})$  in Equation (3-4) remains nearly constant. Because of this, within this range of  $V_{GS}$  Equation (3-4) can be reduced to Equation (3-5):

$$I_{DS} = \left(\frac{W}{L}\right) \mu_n C_{ox,eff} \left[ (kV_{DS}) - \frac{V_{DS}^2}{2} \right] \quad (3-5)$$

where

$$k = [V_{GS} - (V_{TH} + \Delta V_{TH})] \quad (3-5a)$$

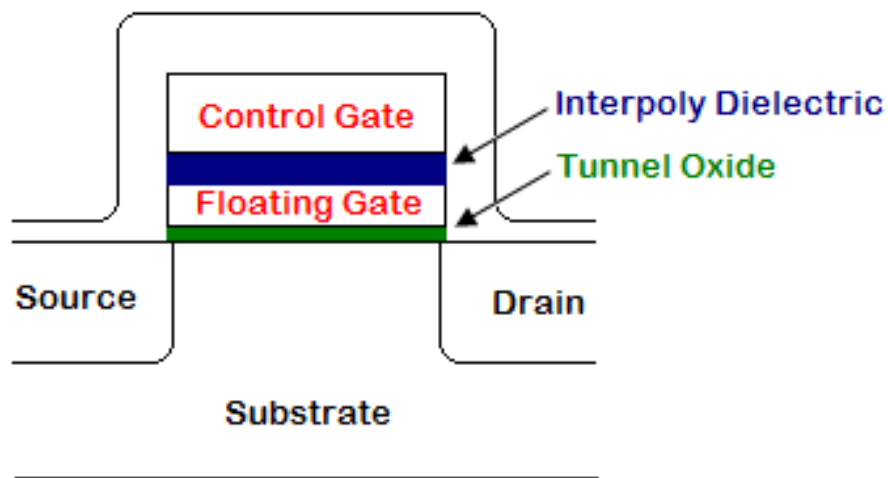
From Equation (3-5), it is obvious that  $I_{DS}$  is independent of  $V_{GS}$  within this range of  $V_{GS}$ , and it is almost constant at a fixed  $V_{DS}$ . When expressing the transfer characteristic of  $I_{DS}$  as a function of  $V_{GS}$ , we can observe the ON and the OFF states of the device, in addition to an intermediate “i” state in between due to  $I_{DS}$  independence on  $V_{GS}$  as given in Equation (3-5). A graphical depiction of this three-state phenomenon is shown in Figure 3-3.



**Figure 3-3: Graphical representation of the three states in a QDG-FET.**

## 4. Non-volatile Memory Devices

A conventional non-volatile memory (NVM) transistor has a floating gate sandwiched between the tunnel oxide and the control gate, and charges are stored in the continuous floating gate material, as shown in Figure 4-1:

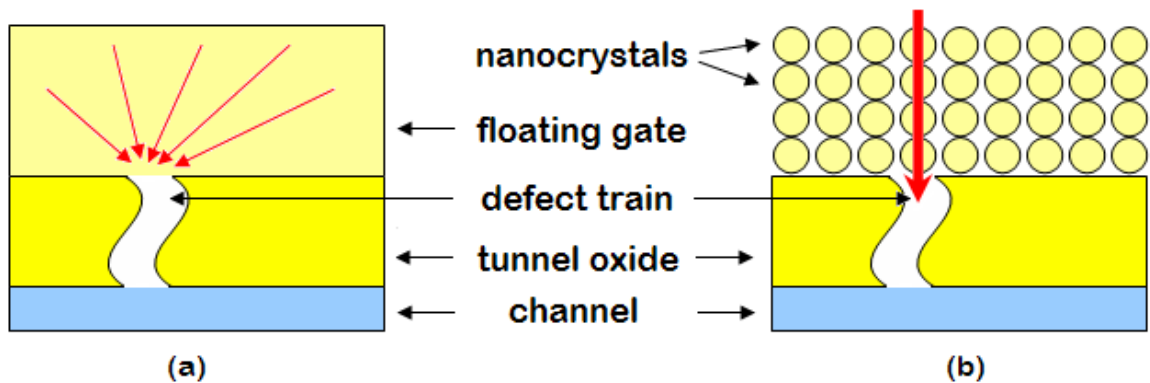


**Figure 4-1: A conventional NVM transistor.**

Scaling of CMOS means faster operating speed of memory devices, but also thinner gate dielectric, as discussed in Chapter One. A thinner gate dielectric can lead to an increase in leakage current and hence reduce the nonvolatile memory reliability and cause retention problems. If there is a defect in the thin tunnel oxide, all the stored charges can be drained out of the continuous floating gate.

In light of this, memory devices with silicon nanocrystals as the floating gate were introduced [58]. These silicon nanocrystals act as the charge storage units, and if there is a defect in the tunnel oxide, only the charges stored immediately on top of the defect would be lost. However, in order to avoid charge sharing between these unpassivated nanocrystals, the nanocrystals need to be separated from each other. This reduces the packing density of the nanocrystals, which decreases the amount of stored charges in the device.

In our group, cladded quantum dots (QDs) have been used as the floating gates of the memory devices [47, 55-57]. The oxide claddings on these dots insulate the QDs from each other in a closely-packed setting, and this prevents charge sharing among dots. This also allows the QDs to be placed directly next to each other, which can maximize the density of QDs and the stored charges in the device. Figure 4-2 illustrates the defect train that can generate in the tunnel insulator, and how the data can be lost through the defect train in a conventional NVM and a cladded-QD-gated NVM [61].



**Figure 4-2: Data loss paths in (a) conventional NVM and in (b) cladded-QD-gated NVM [61].**

In a NVM metal-oxide-semiconductor (MOS) capacitor, the threshold voltage,  $V_{TH}$ , is given by Equation (4-1) [62]:

$$V_{TH} = 2\Phi_F + \Phi_{ms} - \frac{Q_{in}}{C_{in}} - \frac{Q_{dep}}{C_{in}} - \frac{Q_{FG}}{C_{CG \rightarrow QD}} \quad (4-1)$$

In the equation,

$\Phi_F$  = the semiconductor Fermi level at the surface

$\Phi_{ms}$  = the metal-semiconductor work function difference

$Q_{in}$  = the fixed charge at the semiconductor-insulator interface

$Q_{dep}$  = the charge in the semiconductor depletion layer

$C_{in}$  = the capacitance of the dielectric layer

$Q_{FG}$  = the charge in the floating gate

$C_{CG \rightarrow QD}$  = capacitance between the control gate and the floating gate

When charges are stored in the floating gate, only the last term in Equation (4-1) can be affected, and so the change in the threshold voltage,  $\Delta V_{TH}$ , is, given in Equation (4-2) as

$$\Delta V_{TH} = -\frac{Q_{FG}}{C_{CG \rightarrow QD}} \quad (4-2)$$

In a NVM that comprises of cladded QDs as the floating gate, Equation (4-2) can be rewritten as:

$$\Delta V_{TH} = -\frac{\Delta Q}{C_{CG \rightarrow QD}} \quad (4-2a)$$

In the equation,  $\Delta Q$  is the change in the stored charges in the QDs. The number of charges in the QDs depends on the current density flowing into the QDs during the charging time,  $t_w$ , of the QD floating gate, and the current density in turn depends on the number of electrons stored in each QD ( $n_q$ ), the charge of an electron ( $q$ ), the number of QDs per unit area ( $d_{qd}$ ), and the tunneling rate  $R_t$  of the electrons from the channel to the QDs, as shown in Equation (4-3) [47].

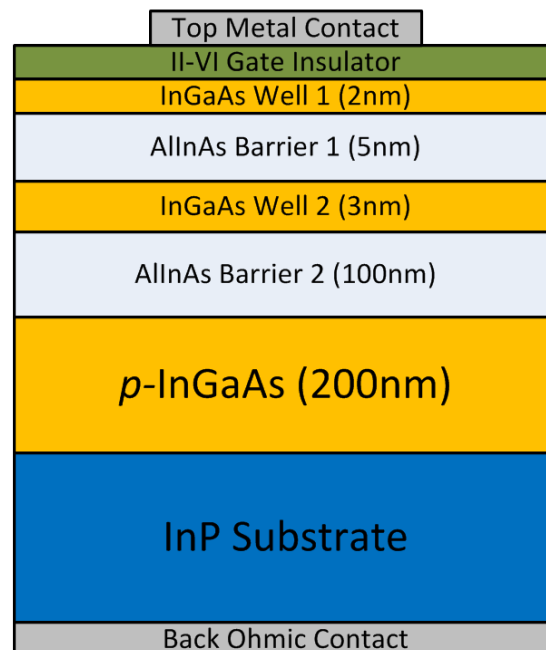
$$\Delta V_{TH} = -\frac{\Delta Q}{C_{CG \rightarrow QD}} = -\frac{\int_0^{t_w} j(t) \cdot A \cdot dt}{C_{CG \rightarrow QD}} \quad (4-3)$$

$$j(t) = q \cdot n_q \cdot d_{qd} \cdot R_t \quad (4-3a)$$

In our QD devices, electrons are being stored as the gate voltage increases, which is shown as a positive shift in a capacitance-voltage characteristic.

## 5. Spatial Wavefunction Switching (SWS) Effects

The spatial wavefunction switching (SWS) effect has been previously introduced by Jain, *et. al.* [59-60]. This phenomenon appears in transport channels comprising of quantum well/barrier structures. Figure 5-1 shows a cross-sectional view of such a structure consisting of an upper InGaAs well 1 (2nm well width), an upper AlInAs barrier 1 (5nm barrier width), a lower InGaAs well 2 (3nm well width) and a lower AlInAs barrier 2 (100nm barrier width). The InGaAs layers, which have a smaller bandgap, are sandwiched between the wider-bandgap AlInAs barriers, forming quantum wells that act as transport channels for charge carriers.



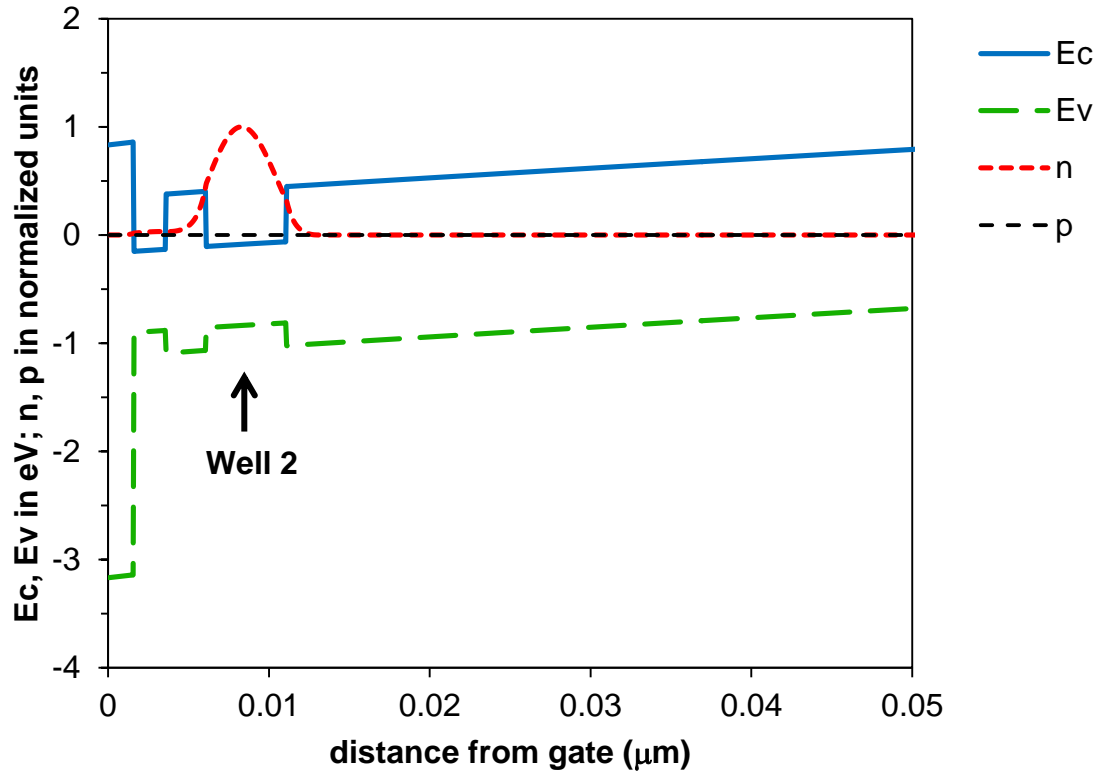
**Figure 5-1: Cross-sectional view of a two-well SWS structure**

The SWS effect can be illustrated in a metal-oxide-semiconductor (MOS) capacitor using the SWS structure. An appropriate gate insulator, e.g. II-VI gate dielectric, is deposited on top of the upper InGaAs well 1. The quantum well transport channels have different threshold voltages, which makes it possible to selectively activate one or both channels depending on the applied gate voltage. When the applied voltage,  $V_G$ , is greater than the threshold voltage,  $V_{TH1}$ , of the lower channel (lower InGaAs well 2), charge carriers appear in the lower transport channel, as shown by the red curve labeled “ $n$ ” in Figure 5-2. The symbols  $E_c$ ,  $E_v$ ,  $n$  and  $p$  represent the conduction energy band, valence energy band, electron carrier concentration, and hole carrier concentration respectively. In this simulation,  $V_G$  was -3.15V.

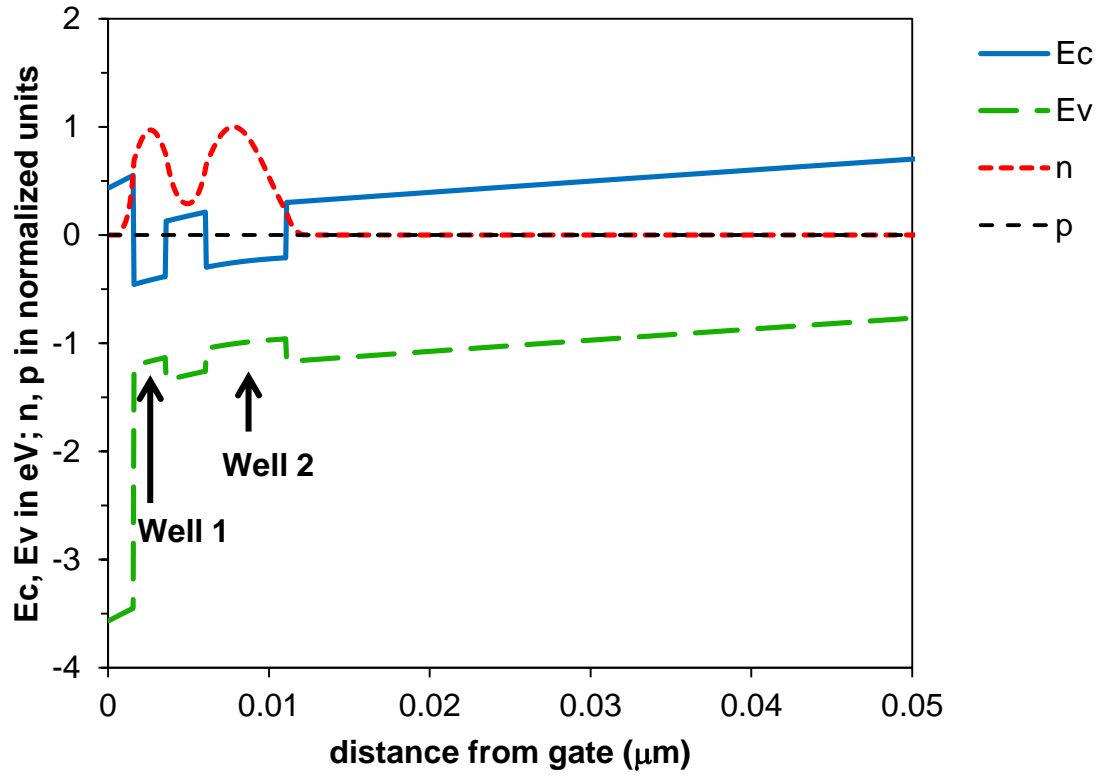
As  $V_G$  continues to increase (to -2.75V in this case), the charge carriers spatially-switch from the lower InGaAs well 2 to the upper InGaAs well 1, occupying both channels as shown in Figure 5-3. The electrons will eventually only be confined in the upper InGaAs well 1, as shown in Figure 5-4, when  $V_G$  was increased further to -2.15V.

The asymmetry of the InGaAs transport channels allows us to design the structure such that the channels can have distinct ranges of voltages that control the presence of charge carriers in each quantum well transport channels [59]. For better noise immunity and minimal overlap, a three-well SWS structure can be used to create the three states using the top and the bottom channels.

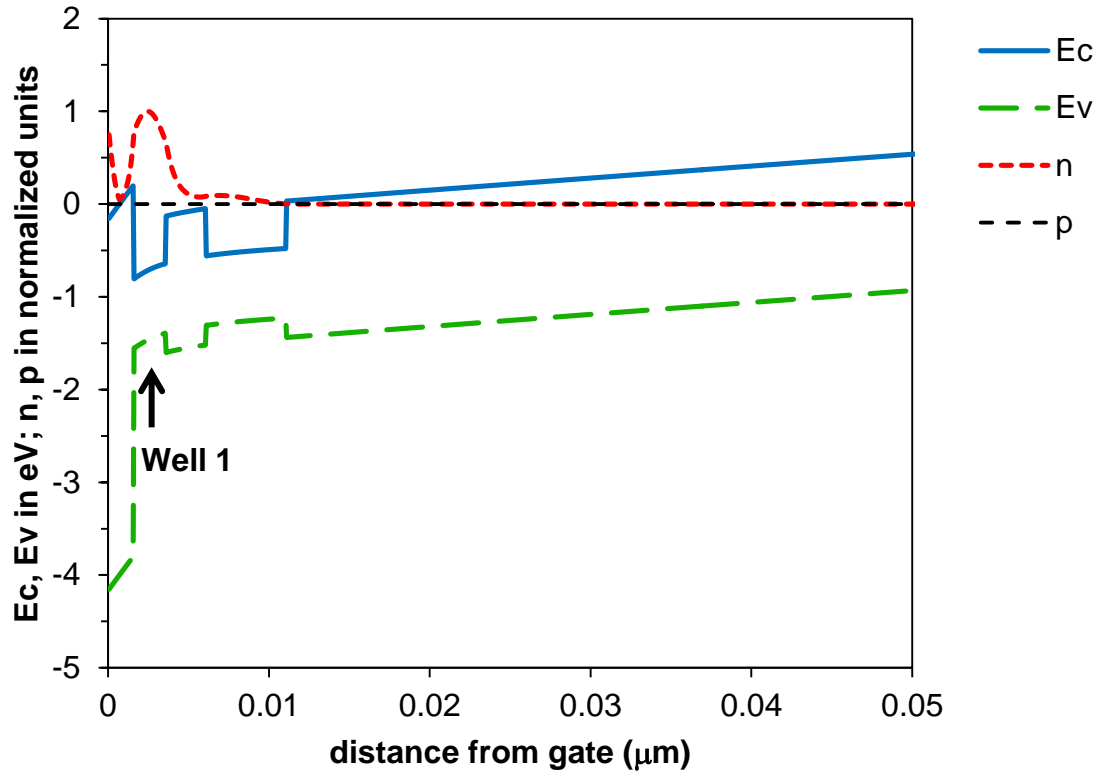




**Figure 5-2: Band diagram showing electrons in the lower InGaAs well 2, when the applied voltage,  $V_G$ , is greater than the threshold voltage of the well 2 channel ( $V_G$  is -3.15V in this case).**



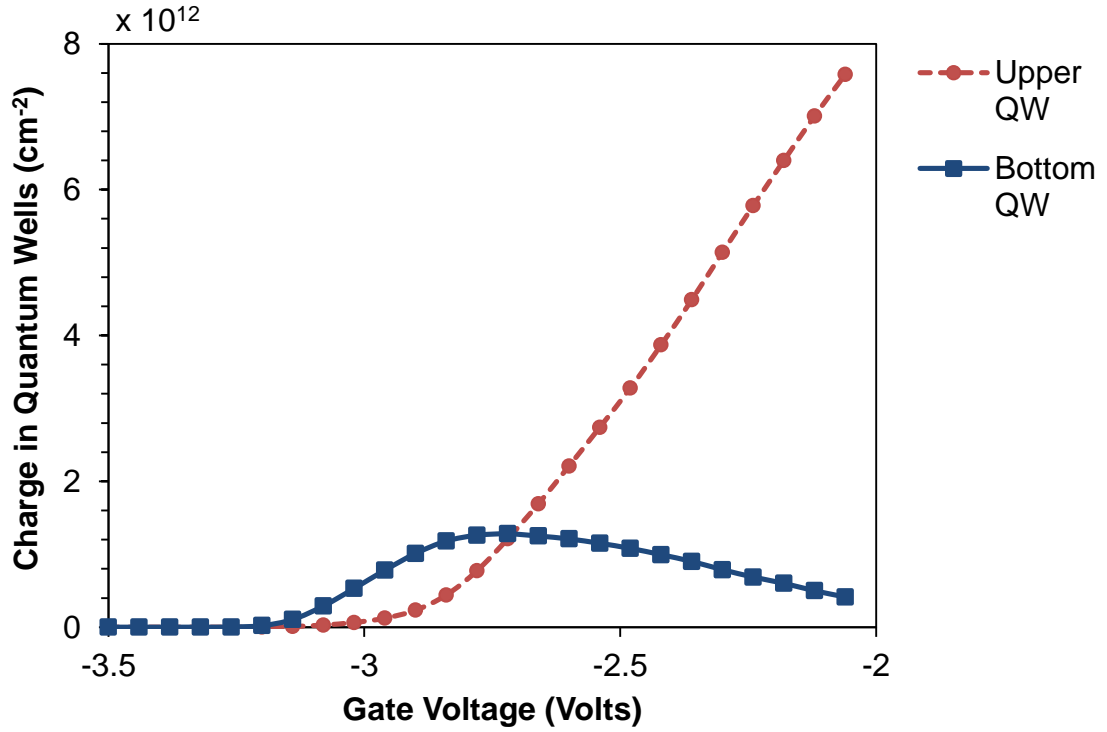
**Figure 5-3: As  $V_G$  continued to increase to  $-2.75\text{V}$ , electrons were spatially switched to the upper InGaAs well 1, occupying both quantum well transport channels.**



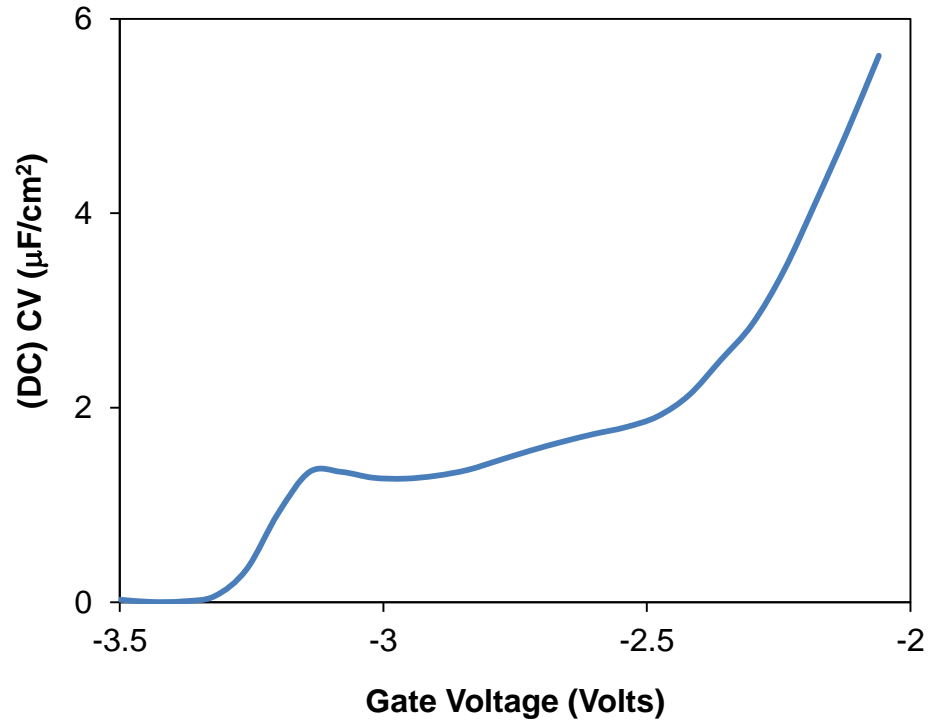
**Figure 5-4:** Band diagram showing electrons confined only in the upper InGaAs well 1 as  $V_G$  continued to increase to -2.15V.

Figure 5-5 shows the charge carrier density in the two quantum wells as a function of the applied gate voltage. This plot shows that for  $-3.15\text{V} < V_G < -2.75\text{V}$ , charges were primarily in the bottom well 2, and when  $V_G > -2.75\text{V}$ , charges were in the upper well 1, further illustrating the charge switching between the two wells with respect to the applied gate voltage.

The charge switching action can also be demonstrated in the capacitance-voltage (C-V) relationship of the SWS device. Figure 5-6 shows the simulated quasi-static C-V plot of the device in the inversion regime. A peak appeared when  $V_G$  is  $-3.15\text{V}$ , when the carriers appear in the bottom well 2. When  $V_G$  is between  $-3\text{V}$  and  $-2.75\text{V}$ , charge carriers start to tunnel into the upper well 1, as shown in Figure 5-5. This corresponds to the disappearance of the characteristic peak in the C-V plot.



**Figure 5-5: Charge carrier density as a function of the applied gate voltage in the two quantum wells. For  $-3.15\text{V} < V_G < -2.75\text{V}$ , the charges were primarily in the bottom well 2, and for  $V_G > -2.75\text{V}$ , the charge carriers were spatially switched to the upper well 1.**



**Figure 5-6: Simulated quasi-static capacitance-voltage (C-V) characteristic of the two-well SWS device showing a distinct peak around  $V_G$  of -3.15V, indicating charge carriers transferring from the lower well 2 to the upper well 1, giving rise to the spatial-switching of charge carriers in the structure.**

The SWS effect can also be realized in an FET. The quantum well transport channels will locate between the source and drain regions of the FET. In an SWS-FET, the drain current expression is the same as the standard drain-to-source current expression for a conventional FET, and is given by Equation (5-1) [59]:

$$I_{DS} = \left(\frac{W}{L}\right) \mu_n C_{ox,eff} \left[ (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (5-1)$$

The quantities  $C_{ox,eff}$ , and  $V_{TH}$  vary according to which transport channel the charge carriers are present. When the carriers are present only in the lower quantum well at  $V_{GS1}$ ,  $C_{ox,eff}$  and  $V_{TH}$  will be small, giving rise to a lower  $I_{DS}$ . At a much higher  $V_{GS2}$ , the carriers are in the upper quantum well, and  $I_{DS}$  will only be detected in the upper channel.

To harness the different currents in different channels, individual drain contacts must be implemented for each channel, while all channels can share the same source contacts. Applying the channel-specific  $V_{GS}$  to the channels, it is possible to activate one or both the channels as desired, and control where the charge carriers reside. For a two-channel SWS-FET with individual drain contacts, four different logic states as outputs are possible: **00** when no charge carriers are present in either quantum well; **01** when charge carriers are in the lower well 2; **11** when charges are found in both wells; and **10** when charge carriers are only in the upper well 1.

## 6. Device Fabrication

This chapter describes the experimental procedures of the fabrication of various devices used in this research. Device fabrication usually includes sample cleaning, photolithography, wet etching, InGaAs regrowth in the source and drain regions, deposition of II-VI gate dielectric stack, self-assembly of GeO<sub>x</sub>-cladded Ge QDs, and metallization. Standard recipes for each step are given below, with the more detailed description of each device to follow.

All the InGaAs and SWS wafers used in this research were epilayers grown on lattice-matched *p*-type InP substrate. For photolithography purposes, 1200Å of plasma-enhanced chemical vapor deposition (PECVD) SiO<sub>2</sub> was deposited on the wafer as the masking oxide.

### **6.1.      *Standard wafer cleaning procedures***

- a) Cleaned in boiling trichloroethylene for 5 minutes.
- b) Cleaned in boiling acetone for 5 minutes.
- c) Cleaned in boiling methanol for 5 minutes.
- d) Rinsed in deionized water (resistivity of 18.2 MΩ·cm) for 1 minute.
- e) Dehydrated on a 200°C hotplate for 5 minutes.



## **6.2.        *Standard photolithography procedures***

- a) Mounted the sample on a pre-cleaned 2-inch mounting wafer using S1813 positive photoresist from Shipley.
- b) Applied S1813 on the sample at 5000RPM for 30 seconds.
- c) Soft-baked the sample on a 115°C hotplate for 2 minutes.
- d) Aligned sample with a photomask.
- e) Exposed the aligned sample to ultraviolet (UV) light for 30 seconds.
- f) Baked the sample on a 115°C hotplate for 1 minute [pre-develop bake].
- g) Developed the patterned sample in a solution consisting of 1 part 351 developer (Shipley) and 3.5 parts deionized water between 15 to 30 seconds.
- h) Hard-baked the developed sample on a 115°C hotplate for 10 minutes.
- i) Etched the sample in an etchant solution.
- j) Removed photoresist with acetone.

## **6.3.        *Metal Lift-off procedures***

- a) Mounted the sample on a pre-cleaned 2-inch mounting wafer using S1813 positive photoresist from Shipley.
- b) Applied S1813 on the sample at 5000RPM for 30 seconds.
- c) Soft-baked the sample on a 100°C hotplate for 2 minutes.
- d) Aligned sample with a photomask.
- e) Exposed the aligned sample to ultraviolet (UV) light for 30 seconds.

- f) Developed the patterned sample in a solution consisting of 1 part 351 developer (Shipley) and 3.5 parts deionized water between 15 to 30 seconds.
- g) Etched the sample in an etchant solution.
- h) Evaporated metal on the sample.
- i) Soaked the metallized sample in acetone until all the photoresist was removed.

#### **6.4.        *Gate Dielectric Stack Deposition***

The II-VI gate dielectric stack was deposited by metal-organic chemical vapor deposition (MOCVD) in an EMCORE reactor [63-64]. This is a stainless steel vertical vapor phase epitaxy reactor, which is equipped with a molybdenum susceptor (capable of rotating) for sample holding that is resistively heated with a graphite heater. The growth chamber and the load lock are separated by a gate valve to minimize atmospheric contamination. The transfer of samples from the load lock to the growth chamber is facilitated by a mechanical arm.

Hydrogen gas is used as the carrier gas in the system. It is passed through a palladium cell that is heated to 400°C to reach a 99.99999% purity. This purified H<sub>2</sub> gas is then passed through the bubblers containing various metal-organic alkyl-based precursors used in the experiments, and the different precursor-saturated H<sub>2</sub> gases are subsequently introduced into the growth chamber. The mole fractions of the metal-organic reactants are determined by the temperatures of the precursor bubblers (which

determine the vapor pressures of the precursors), the flow rates of the precursor species, and the flow rate of the H<sub>2</sub> gas.

The flow of precursor-saturated H<sub>2</sub> reaches the growth chamber as laminar flow, and the molybdenum susceptor rotates the sample to create uniform lateral growth over the sample.

During the deposition, the chamber pressure was maintained at 250 Torr, the molybdenum susceptor motor speed was 350 RPM, and the palladium-diffused hydrogen carrier gas had a flow rate of 14.25 standard liters per minute (slm). The precursor bubbler pressures were kept at 650 Torr.

The operating parameters of the metal-organic liquid precursors used in the growths were different depending on the composition of the II-VI dielectric stack.

#### **6.5. *Self-Assembly of GeO<sub>x</sub>-cladded Ge Quantum Dots***

The self-assembly of GeO<sub>x</sub>-cladded Ge quantum dots was carried out in a solution. It was performed immediately after the growth of the II-VI gate dielectric stack deposition, and the procedure was previously described by Gogna et al. [55]. The formation of these quantum dots started with milling 99.999% pure germanium powder using steel spheres with constant agitation for 5 hours, producing ultra-fine Ge powder.

This powder was then allowed to oxidize in a solution of ethanol and benzoyl peroxide for 2 days. The solution vessel was kept in a sonicator, and the pH was maintained between 3 and 4. This solution underwent several centrifugations at various speeds to separate the supernatant liquid from the precipitate, and the supernatant containing the quantum dots was etched using 8-part-per-million 10:1 buffered oxide etch in 100% ethanol to obtain a uniform quantum dot size of 6 nm.

The self-assembly process was carried out by immersing the sample in the 6nm-quantum-dot solution for 3 minutes, followed by rinsing in methanol and drying with a nitrogen jet. To maintain the stability of these quantum dots and the GeO<sub>x</sub> cladding, the sample was annealed in argon at 350°C for 10 minutes. In this three-minute time interval, two layers of dots self-assembled over the *p*-type regions on the sample.

## **6.6. Metallization**

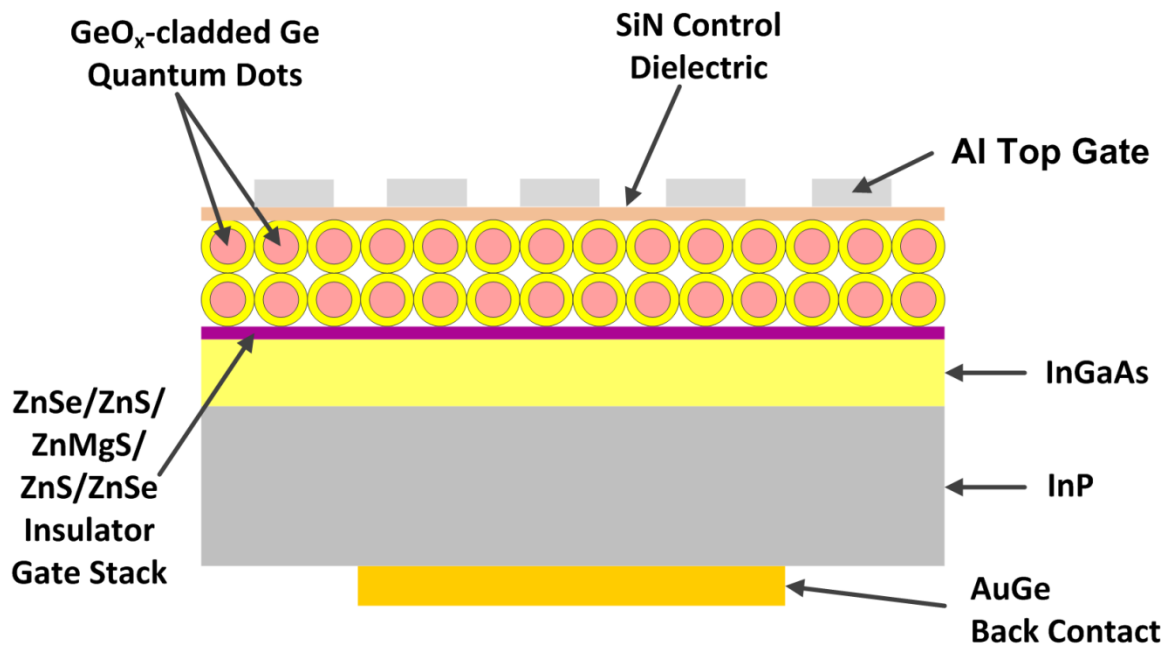
Metal evaporation for all the samples was performed using a Veeco metal evaporator. The system uses a diffusion pump to maintain a chamber pressure in the low  $10^{-7}$  Torr range prior to evaporation. Solid metal sources were placed on either a tungsten coil or a molybdenum boat, and under the sample holder equipped with a manual shutter. The coil or the boat was then heated resistively to melt and vaporize the metal. The evaporating pressure was usually in the  $10^{-5}$  Torr, with an evaporation rate at about 2 Å/sec for lift-off metallization and 10 Å/sec for non-lift-off procedures. This type of metallization is non-

directional, and the film thickness is determined using a crystal oscillator thickness monitor. About 1000Å of metal was usually evaporated on the sample for front and back contacts.

For backside contacts and contacts made on the source and the drain regions of an FET, post-metallization annealing in a sliding furnace was required to form ohmic contacts. In these cases, the metal used was either AuGe or AuGeNi, and the annealing temperature was kept at around 300°C for an annealing duration of 1 minute. The annealing gas was nitrogen.

#### **6.7. *InGaAs Non-volatile Memory MOS capacitors***

Figure 6.7-1 shows the structure of InGaAs NVM MOS capacitors. The processing started with a *p*-type InGaAs epi-layer with  $N_D = 1 \times 10^{16}/\text{cm}^3$  on a *p*-type InP substrate. An InP cap layer was initially deposited on the wafer for protection, and there was no PECVD SiO<sub>2</sub> for masking purposes. The standard wafer cleaning procedures were used to prepare the wafer, and the InP cap layer was removed using an InP etch that is selective from InGaAs consisting of 3 parts phosphoric acid and 1 part hydrochloric acid [65]. The etch rate of this etchant is approximately 0.75 μm/min [66]. The wafer was thoroughly rinsed in deionized water and stored in boiling propanol for the deposition of the dielectric materials, which included the II-VI dielectric stack and GeO<sub>x</sub>-cladded Ge QDs.



**Figure 6.7-1: InGaAs NVM MOS capacitors with GeO<sub>x</sub>-cladded Ge quantum dots**

The II-VI dielectric stack consisted of ZnSe, ZnS and ZnMgSe, and the growth conditions for the metal-organic precursors (run# 2055) are recorded in Table 6.7-1.

**Table 6.7-1: Metal-organic precursor growth parameters used for InGaAs NVM MOS capacitors (run #2055)**

<b>Precursor</b>	<b>Pressure (Torr)</b>	<b>Bubbler Temperature (°C)</b>	<b>Gas Flow (sccm)</b>
Dimethylzinc (DMZn)	57.1	-20	20
Dimethylselenide (DMSe)	37.9	-5	30
Diethylsulfide (DES)	60	45	20
Bis(methyl-cyclopentadienyl) magnesium [(MeCp) <sub>2</sub> Mg]	0.9	60	20

The first layer of the gate dielectric stack was a thin buffer layer of ZnSe, and the metalorganic precursors were DMZn and DMSe. The growth time was 30 seconds at 505°C. The next layer was a ZnS buffer layer, deposited at 333°C for 1 minute, using precursors DMZn and DES. The third layer, which is the main high- $\kappa$ , wide-bandgap insulator in the stack, was Zn<sub>0.95</sub>Mg<sub>0.05</sub>S. This layer was deposited at 333°C for 3 minutes, using precursors DMZn, DES and (MeCp)<sub>2</sub>Mg. The fourth layer was ZnS, with the same growth conditions as before. The insulator stack was then capped with ZnSe,

deposited at 333°C for 2 minutes. All layers were deposited with an ultra-violet (UV) radiation of 35 mW/cm<sup>2</sup>.

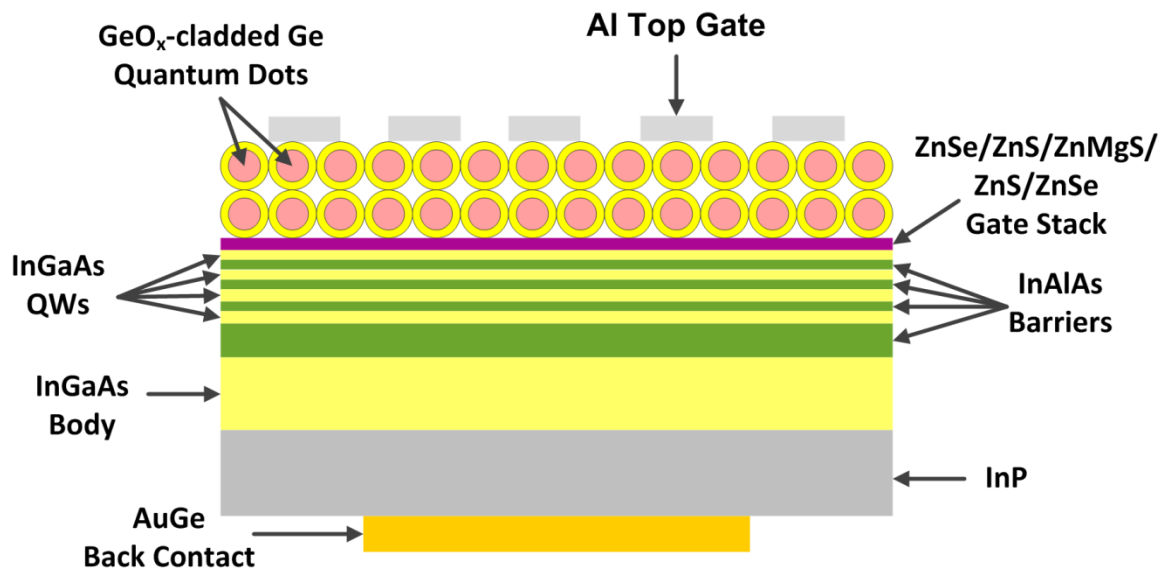
Self -assembly and annealing of GeO<sub>x</sub>-cladded Ge QDs followed the deposition of the II-VI gate materials. After the self-assembly, a control dielectric in the form of a thin SiN layer (~87.5Å) was deposited using PECVD over the sample. The gases for the deposition included SiH<sub>4</sub> at 36.4 sccm, NH<sub>3</sub> at 200 sccm, and N<sub>2</sub> at 200 sccm. The deposition temperature was 200°C, and the pressure was at 2.6 Torr. At a deposition rate of about 350Å/min, the deposition time was 14 seconds.

AuGe back contact and aluminum gate contact were evaporated using a shadow mask and annealed to finish the processing.

#### **6.8.      *Four-Well SWS MOS capacitors***

The fabrication of the 4-well SWS MOS capacitors was similar to that of the InGaAs NVM MOS capacitors presented in Section 6.7, with the exclusion of the PECVD SiN layer after self-assembly. The MOCVD run number was 2056. The structure of the 4-well SWS MOS capacitors is shown in Figure 6.8-1. Table 6.8-1 shows the composition of the SWS wafer, the layer thicknesses and the functions of the individual layers.





**Figure 6.8-1: Structure of 4-well SWS MOS capacitors**

**Table 6.8-1: Compositional information of the four-well SWS wafer**

Layer	Thickness (nm)	Description
InGaAs	2	Well 1
InAlAs	2	Barrier 2
InGaAs	2	Well 2
InAlAs	2	Barrier 2
InGaAs	2.5	Well 3
InAlAs	2	Barrier 3
InGaAs	2.5	Well 4
InAlAs	100	Barrier 4
InGaAs	200	Body
InP	300	Substrate

### 6.9. *InGaAs QDG-FET*

The fabrication of an InGaAs QDG-FET started with the same *p*-type InGaAs epi-layer on a *p*-type InP substrate as in the MOS capacitor. Masking oxide was deposited onto the wafer in the form of PECVD SiO<sub>2</sub> (Figure 6.9-1). The standard wafer cleaning and photolithography procedures were used. Source and drain regions were defined by etching the masking oxide using 10:1 buffered oxide etch (J.T. Baker), with an etch rate of 60nm/min at room temperature. The etching of the InP cap was performed using the InP etchant described earlier (Figure 6.9-2). The formation of the *n*-type regions was achieved by etching the InGaAs material in the defined source and the drain areas using a

mixture of 1 part phosphoric acid, 1 part hydrogen peroxide and 38 parts water (Figure 6.9-3). This solution etches InGaAs and InAlAs but does not attack InP, and it has an etch rate of 0.1  $\mu\text{m}/\text{min}$  at 21.5°C [65]. About 0.1 $\mu\text{m}$  of the material was removed from the source and the drain regions. After the etching, the source and the drain regions were re-filled by regrowing  $n^+$  InGaAs in the regions (Figure 6.9-4). PECVD SiO<sub>2</sub> was again deposited onto the sample for isolation purposes (Figure 6.9-5). The gate region was defined next, with the masking PECVD SiO<sub>2</sub> and the InP cap removed similarly as before (Figure 6.9-6). The gate dielectric stack was deposited immediately (Figure 6.9-7).

The growth conditions of the II-VI gate dielectric stack (run# 1973) is listed in Table 6.9-1. It is similar to the conditions in Table 6.7-1, except the flow rate of precursor DES was different.

**Table 6.9-1: Metal-organic precursor growth parameters used for InGaAs QDG-FET**

Precursor	Pressure (Torr)	Bubbler Temperature (°C)	Gas Flow (sccm)
Dimethylzinc (DMZn)	57.1	-20	20
Dimethylselenide (DMSe)	37.9	-5	30
Diethylsulfide (DES)	60	45	25
Bis(methyl-cyclopentadienyl) magnesium [(MeCp) <sub>2</sub> Mg]	0.9	60	25

The deposition of the gate dielectric stack was followed by the self-assembly of  $\text{GeO}_x$ -cladded Ge quantum dots as described before (Figure 6.9-8). Metal contact openings were defined in the *n*-type source and drain regions by removing the II-VI gate dielectric materials that was deposited in the areas (Figure 6.9-9). The etchant used to remove the II-VI gate dielectric stack was a mixture of 100mL cold  $\text{H}_2\text{O}_2$  and 22mL of  $\text{NH}_4\text{OH}$ , and the etching time was between 30 seconds to 1 minute. Lift-off metallization of AuGeNi and post-metallization annealing were subsequently performed in the source and the drain regions (Figure 6.9-10). Aluminum was then evaporated onto the sample and defined as the gate contacts (Figure 6.9-11).

Figure 6.9-12 shows the four masks that were used in this fabrication process.



**Figure 6.9-1: Masking PECVD oxide on wafer.**

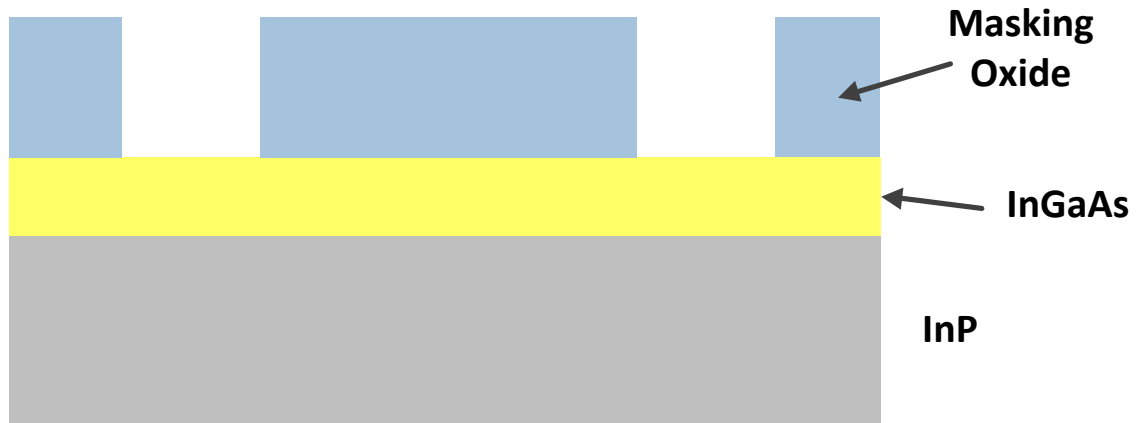


Figure 6.9-2: Defining the source/drain regions.

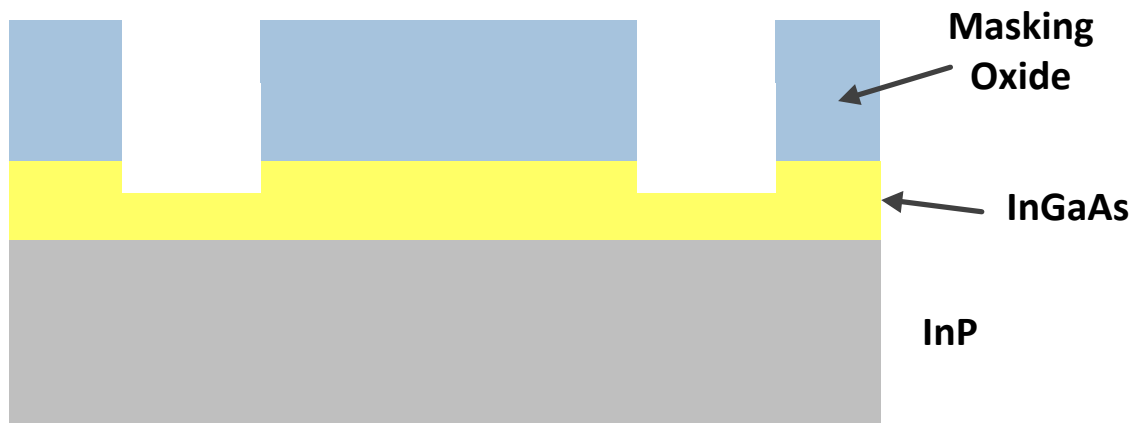


Figure 6.9-3: InGaAs in the source/drain regions was etched.

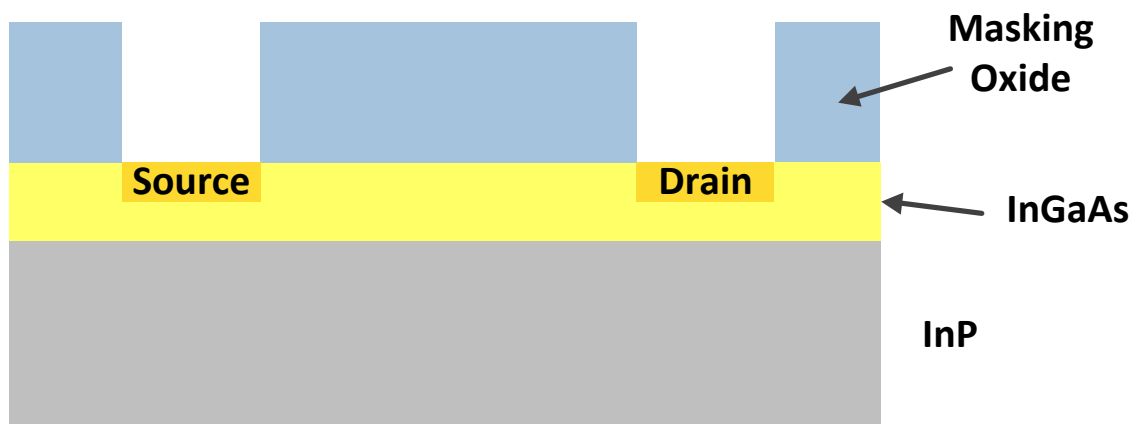


Figure 6.9-4: Regrowth of  $n^+$  InGaAs in the source/drain regions.

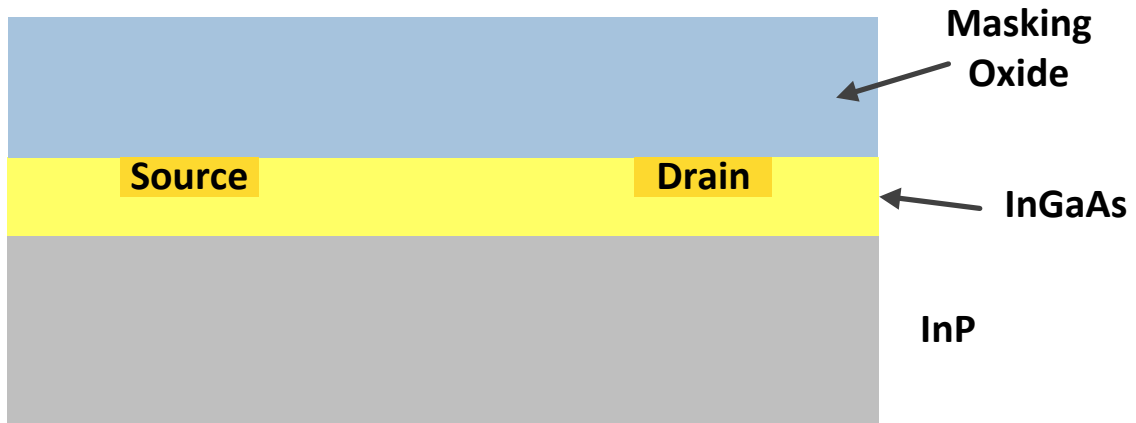


Figure 6.9-5: Re-deposition of PECVD SiO<sub>2</sub>.

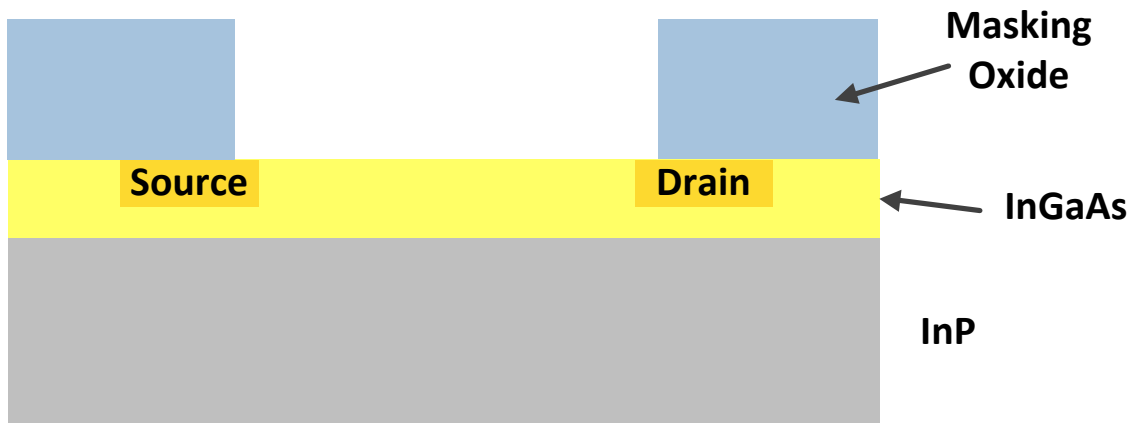


Figure 6.9-6: Gate definition.

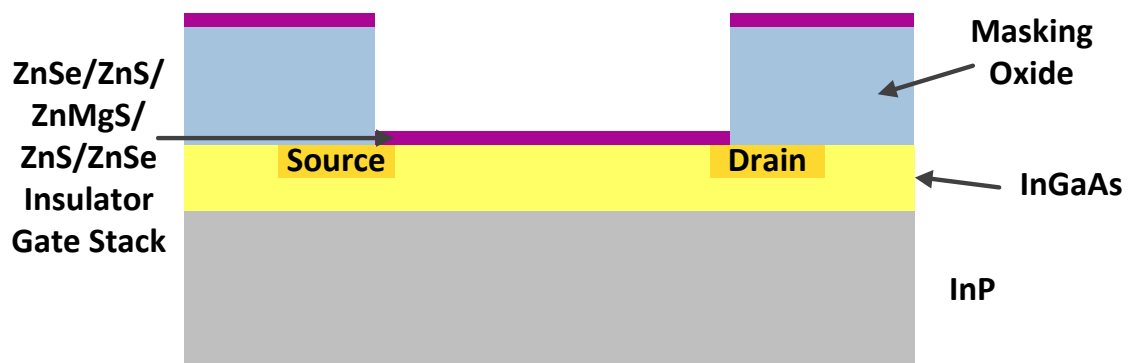


Figure 6.9-7: II-VI gate dielectric stack deposition.

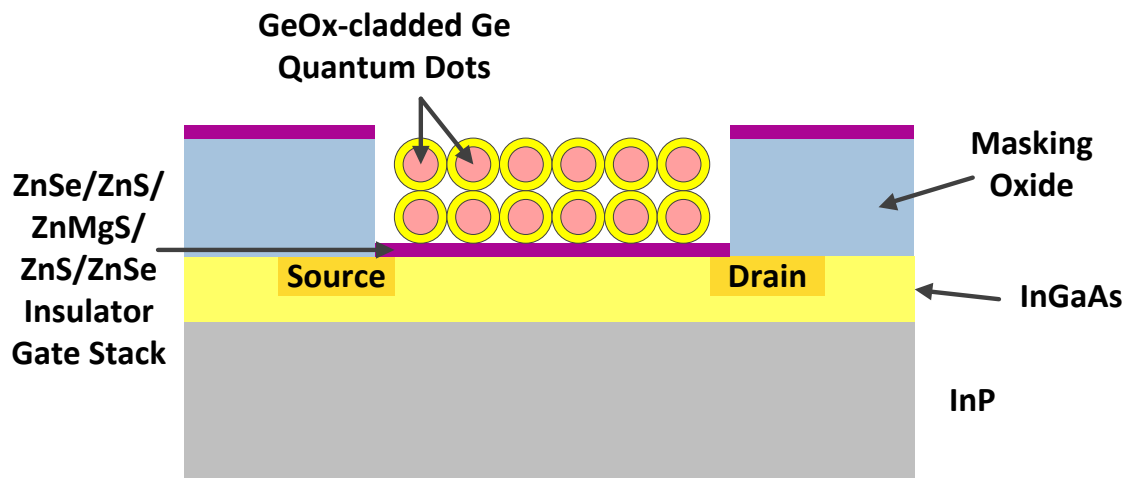


Figure 6.9-8: Self-assembly of GeO<sub>x</sub>-cladded Ge QDs in the gate region.

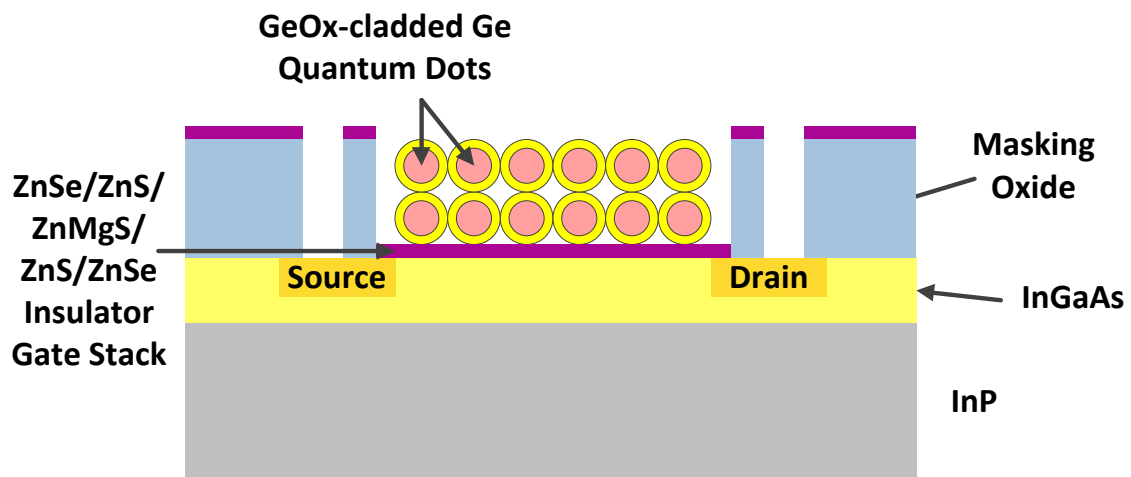


Figure 6.9-9: Metal contact window openings in the source/drain regions.

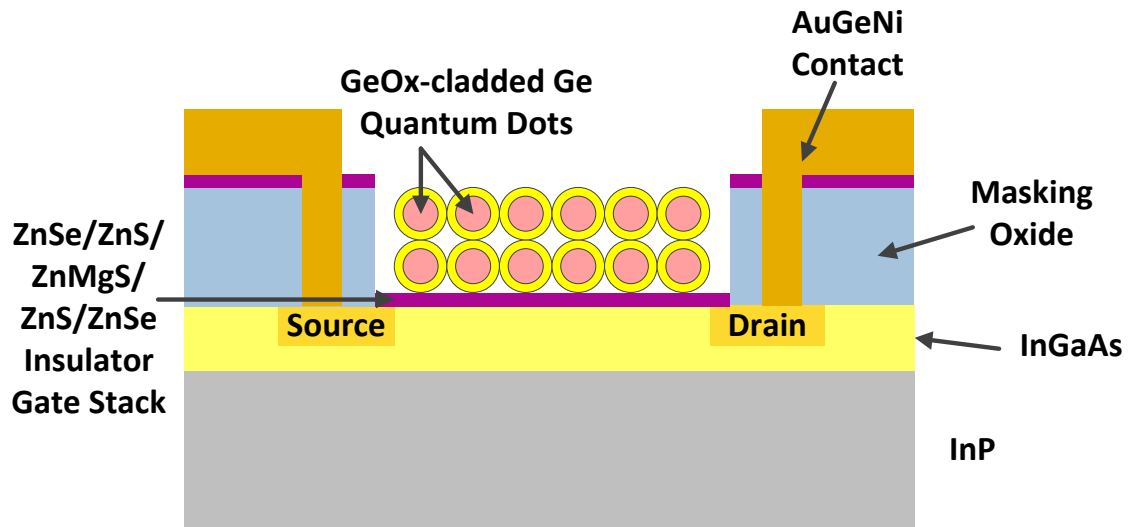


Figure 6.9-10: AuGeNi metal contacts in the source/drain regions.

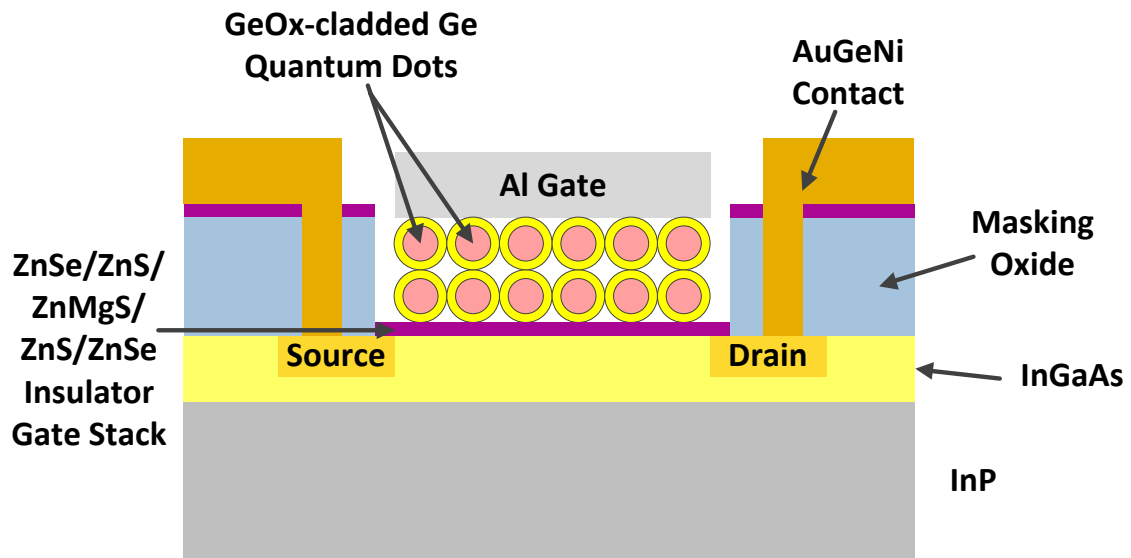
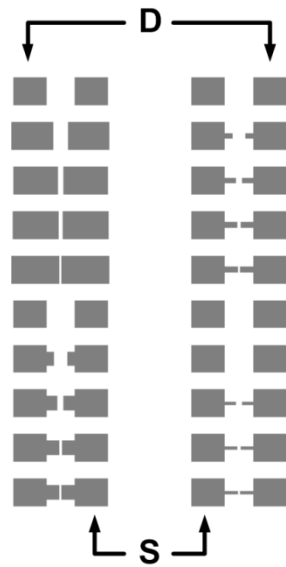
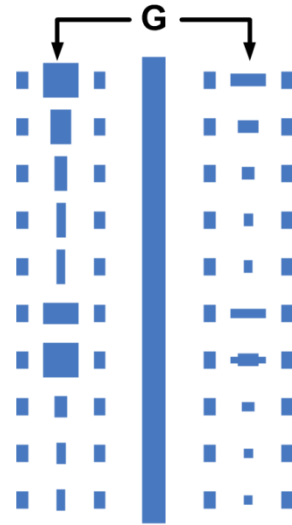


Figure 6.9-11: Al gate contact over the gate materials.





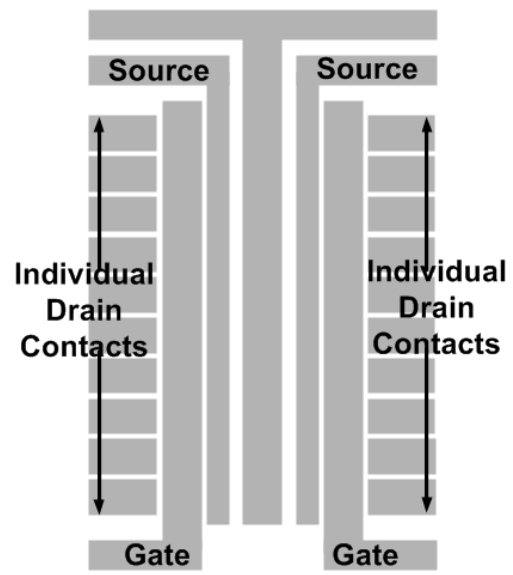
(a)



(b)



(c)



(d)

**Figure 6.9-12: Mask set used for the fabrication of InGaAs QDG- FET.**  
**(a) Source (S) and Drain (D) definitions; (b) Gate (G) definitions; (c) Metal contact window definitions in S/D regions; and (d) Interconnect definition.**

#### 6.10. QDG-FET using a 3-well SWS wafer

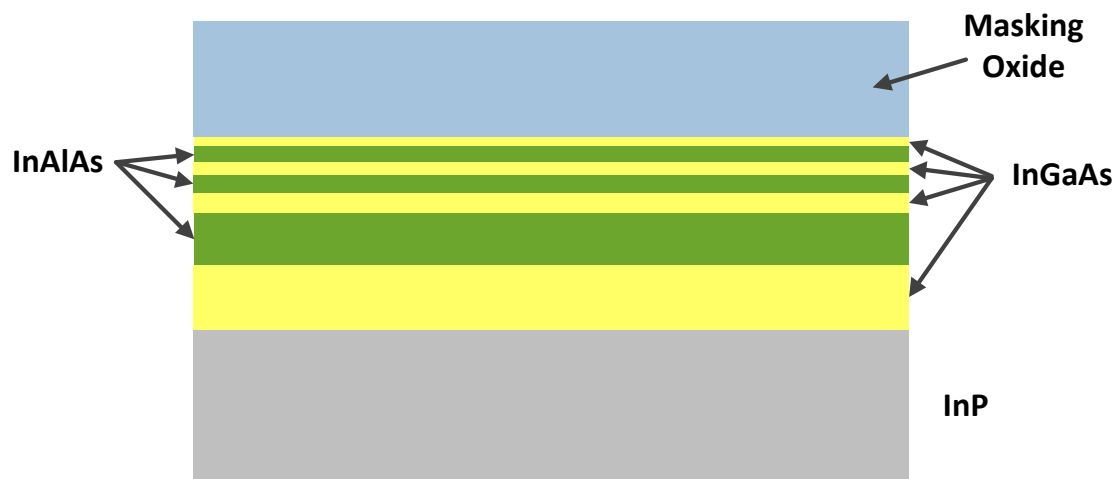
The composition of the 3-well SWS wafer is listed in Table 6.10-1.

**Table 6.10-1: Composition of the 3-well SWS wafer used for QDG-FET.**

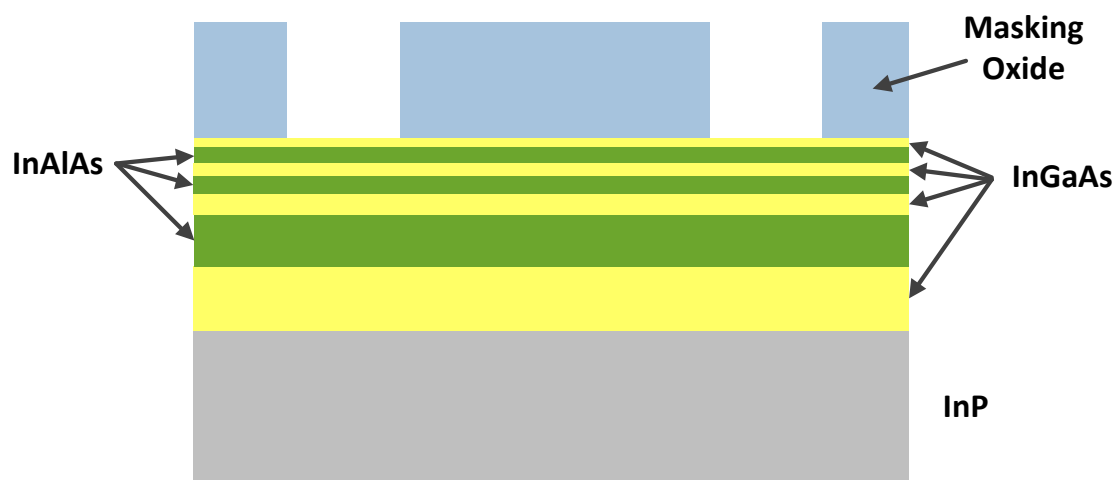
Layer	Thickness (nm)	Description
InP	100	Cap
InGaAs	2	Well 1
InAlAs	3	Barrier 1
InGaAs	2.5	Well 2
InAlAs	3.5	Barrier 2
InGaAs	4	Well 3
InAlAs	100	Barrier 3
InGaAs	200	Body
InP	300	Substrate

The fabrication process was similar to that for the InGaAs QDG-FET presented in Section 6.9 but with one difference. The etching in the source and the drain regions required the etching of the InGaAs/InAlAs quantum wells/barriers in the defined areas. The layers etched included well 1 all the way through well 3. The etchant used for InGaAs and InAlAs was the same used in the previous section.

Figure 6.10 shows the process flow for the QDG-FET using a 3-well SWS wafer.



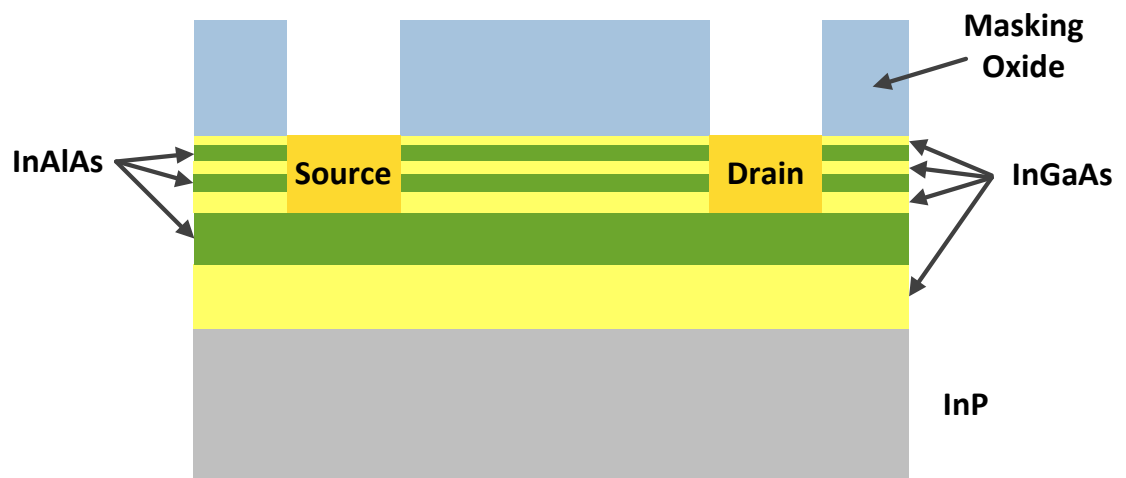
**Figure 6.10-1: Masking PECVD oxide on wafer.**



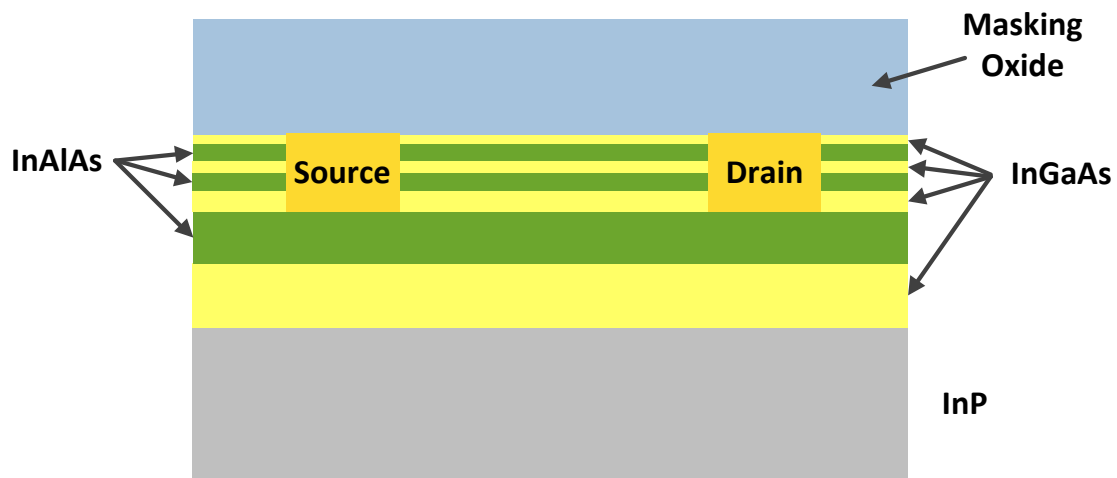
**Figure 6.10-2: Defining the source/drain regions.**



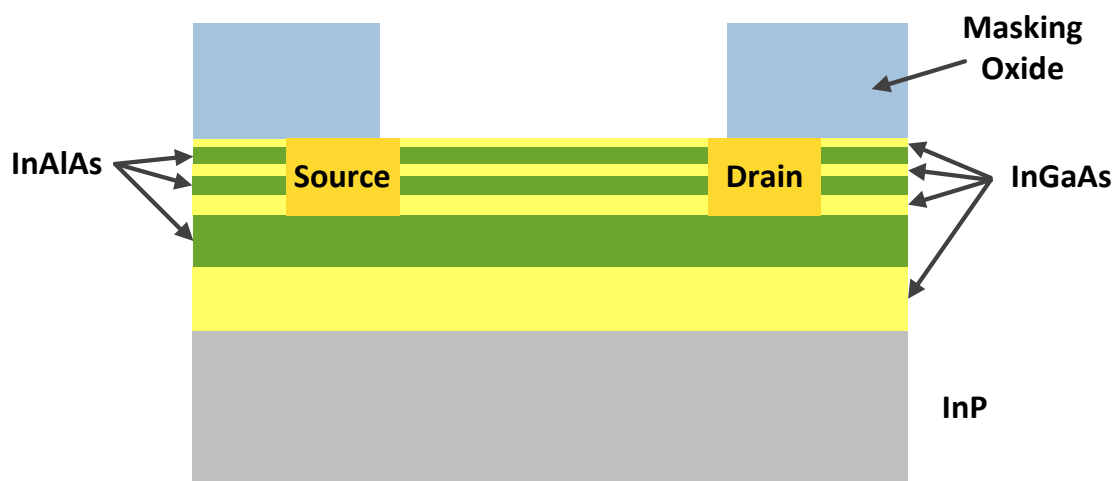
**Figure 6.10-3: InGaAs and InAlAs in the source/drain regions was etched.**



**Figure 6.10-4: Regrowth of  $n^+$  InGaAs in the source/drain regions.**



**Figure 6.10-5: Re-deposition of PECVD SiO<sub>2</sub>.**



**Figure 6.10-6: Gate definition.**

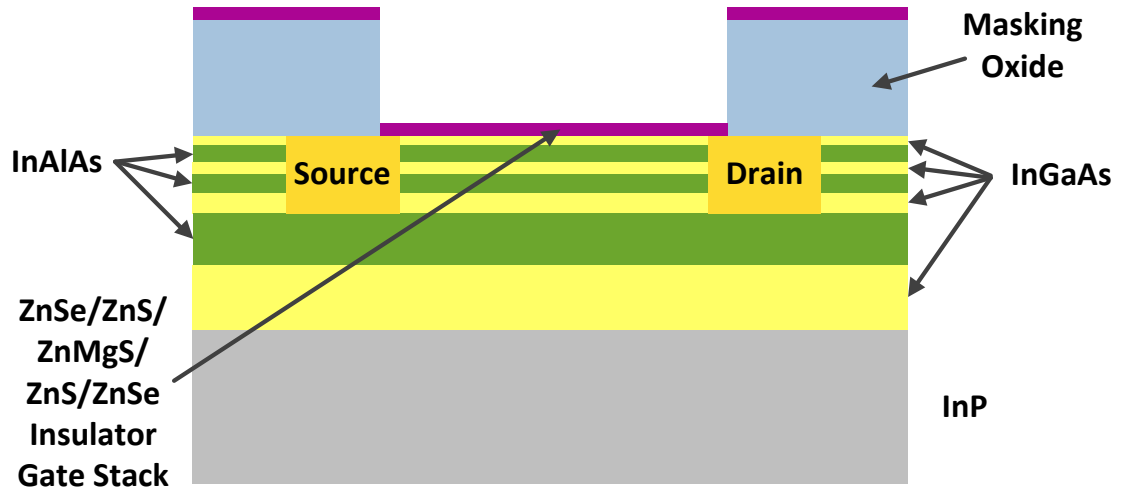


Figure 6.10-7: II-VI gate dielectric stack deposition.

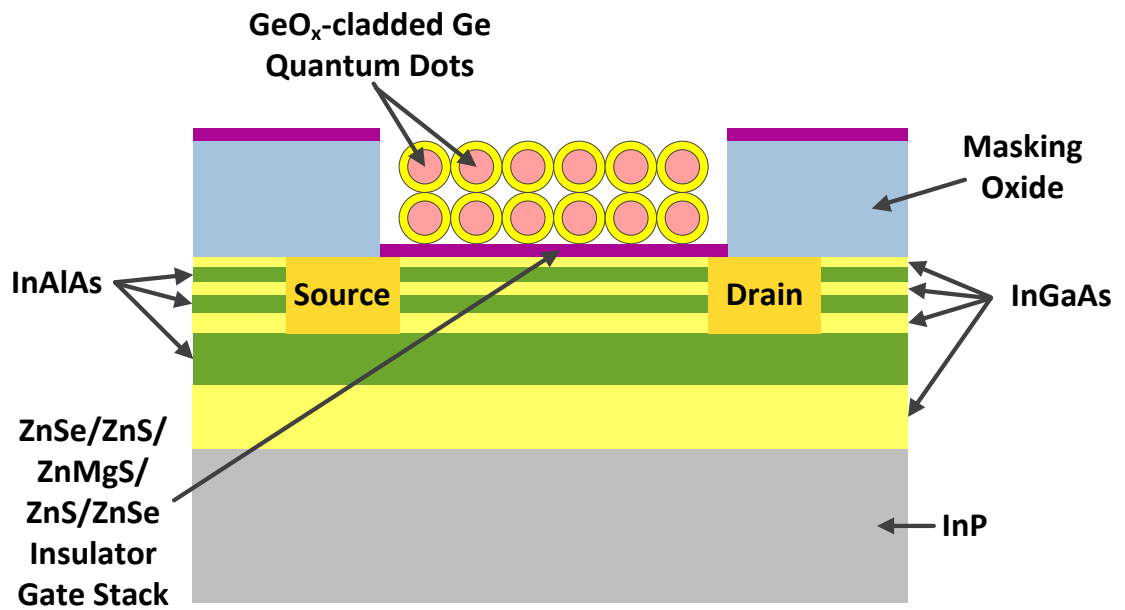


Figure 6.10-8: Self-assembly of GeO<sub>x</sub>-cladded Ge QDs in the gate region.

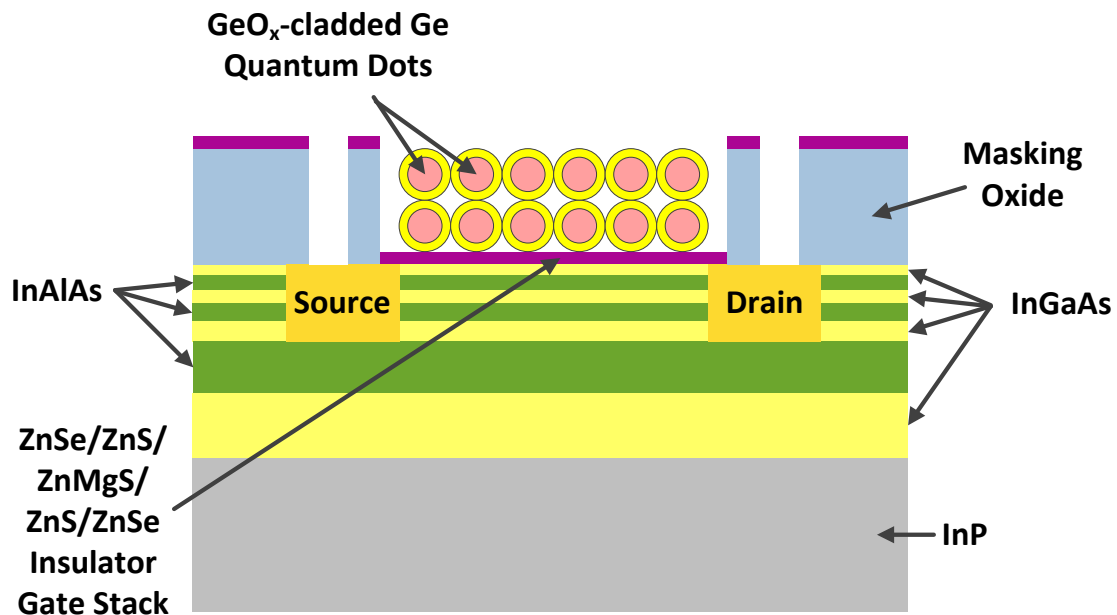


Figure 6.10-9: Metal contact window openings in the source/drain regions.

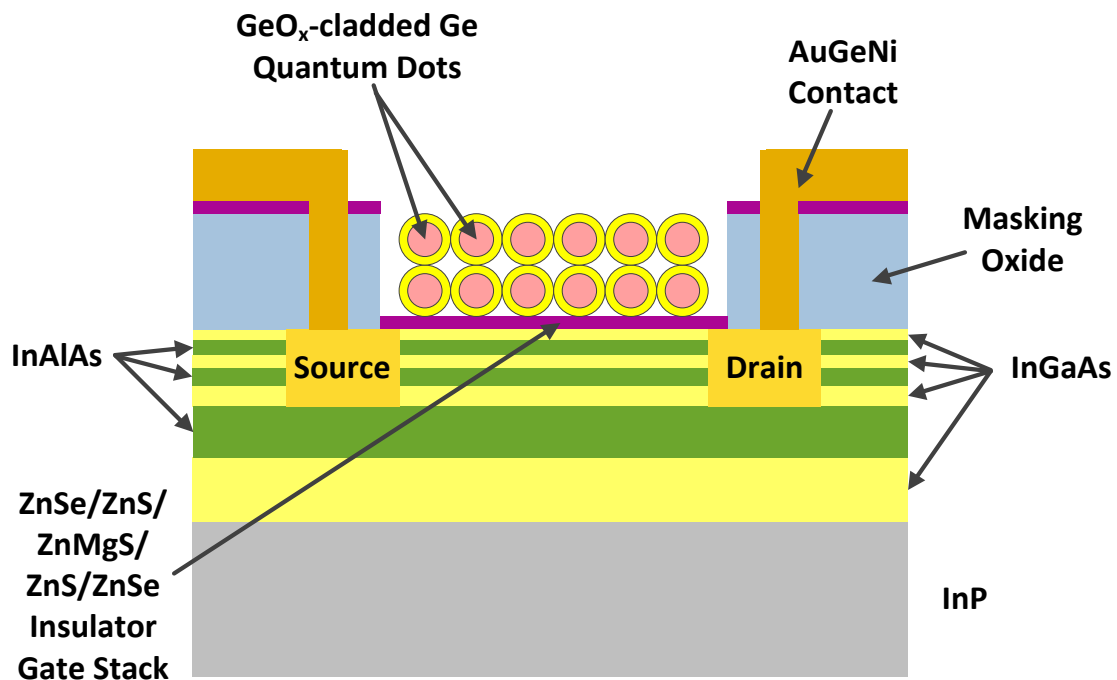
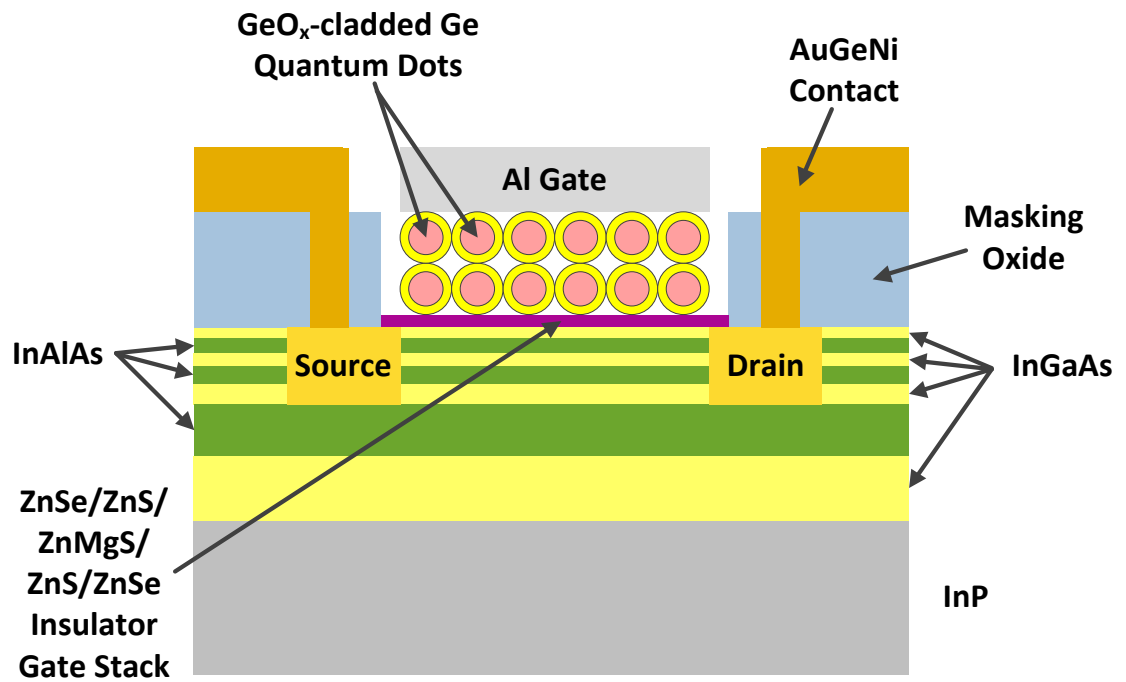


Figure 6.10-10: AuGeNi metal contacts in the source/drain regions.



**Figure 6.10-11: Al gate contact over the gate materials.**



## 7. Discussion on the Gate Materials

### 7.1. II-VI Gate Dielectric Stack Selection

High- $\kappa$  II-VI materials were chosen based on their bandgap energies ( $E_g$ ) and lattice constants ( $a$ ). Figure 7.1-1 shows the relationship between  $E_g$  and  $a$  for various II-VI and semiconductor materials [67]. The black dotted line indicates the lattice constant for the  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  materials (lattice-matched to InP) used in this research.

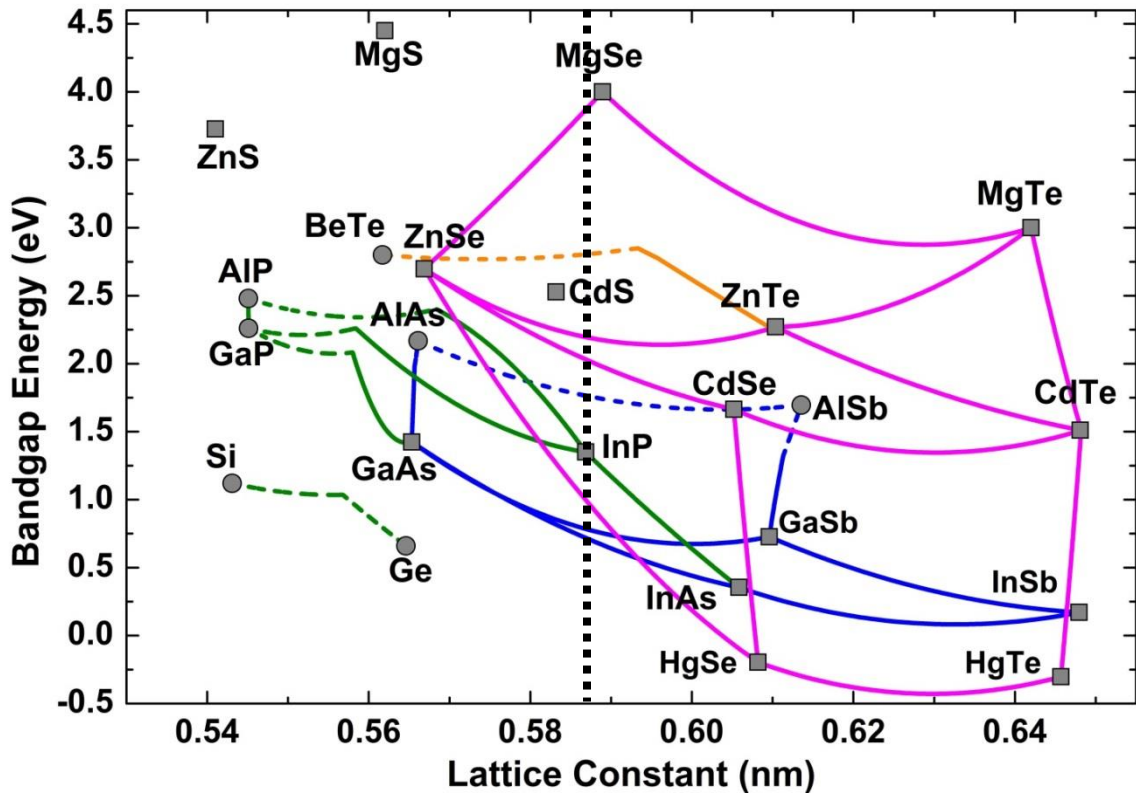


Figure 7.1-1: Relationship between bandgap energies and lattice constants for various II-VI and semiconductor materials. The black dotted line shows the lattice constant for  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  used in this research.

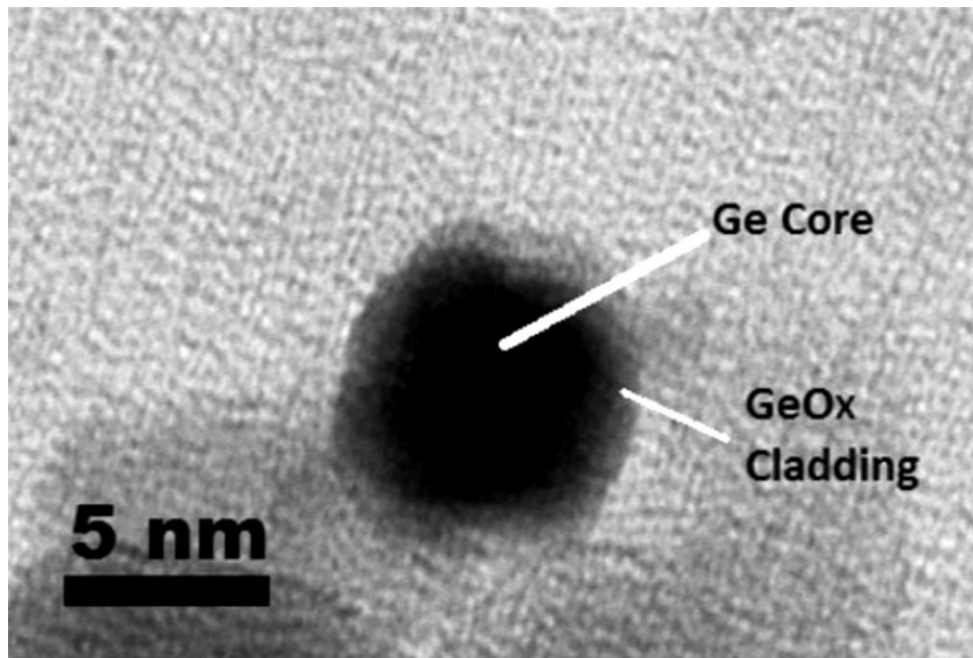
At 300K, the lattice constants for  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  and  $\text{InP}$  are  $5.8687\text{\AA}$  [68]. The choice of II-VI gate stack started with a thin layer of  $\text{ZnSe}$  as a buffer layer. Buffer layers have been used in defect engineering as a mediating medium between the substrate and the device layer to minimize the density of dislocations in the device layer [69]. The thickness of the  $\text{ZnSe}$  buffer layer is less than the critical layer thickness, and so it can be regarded as pseudomorphic. Previous experimental results also showed that a thin  $\text{ZnSe}$  buffer layer aided in the adhesion of the subsequent gate materials to the  $\text{InGaAs}$  channel [51].

In this research, the main high- $\kappa$  materials were the  $\text{ZnS}/\text{ZnMgS}/\text{ZnS}$  stack, with an  $E_g$  of about 4 eV. Even though this combination is not perfectly lattice-matched to  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ , experimental results have shown that this selection of gate materials offered acceptable gate control for  $\text{InGaAs}$  FETs with good drain currents. Previously, Jain et al. presented an  $\text{InGaAs}$  FET using  $\text{ZnSeMgTe}$  as the main high- $\kappa$  material in the gate stack [47]. This choice of II-VI material has a lattice constant closer to that of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ , but the bandgap energy is lower (between 3 - 3.5 eV), and the output characteristic of this FET showed rather low output currents.

UV irradiation was used in the growth to help break down the metal-organic precursors, allowing the growths to be done at a lower temperature [70].

## 7.2. *GeO<sub>x</sub>-cladded Ge QDs*

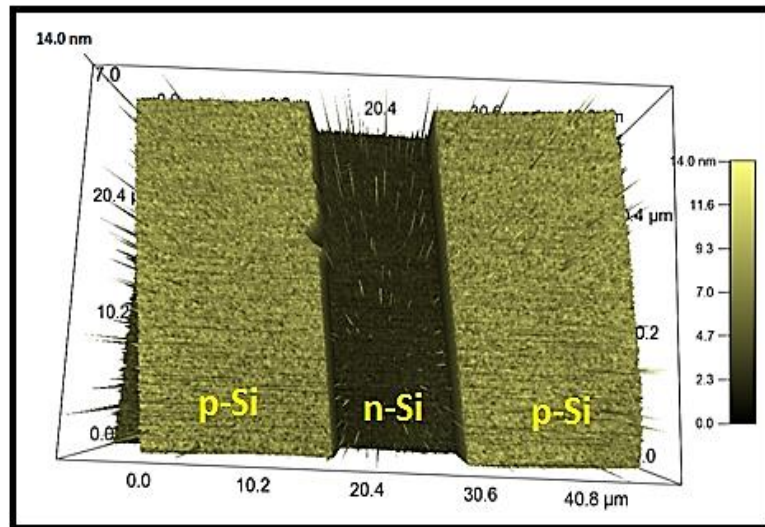
Evidence of oxide-cladded QDs and the size distribution has been presented previously [55]. Figure 7.2-1 shows a high-resolution transmission electron microscopy (HR-TEM) image of a GeO<sub>x</sub>-cladded-Ge quantum dot, showing a core size of about 4nm and a cladding thickness of 1nm.



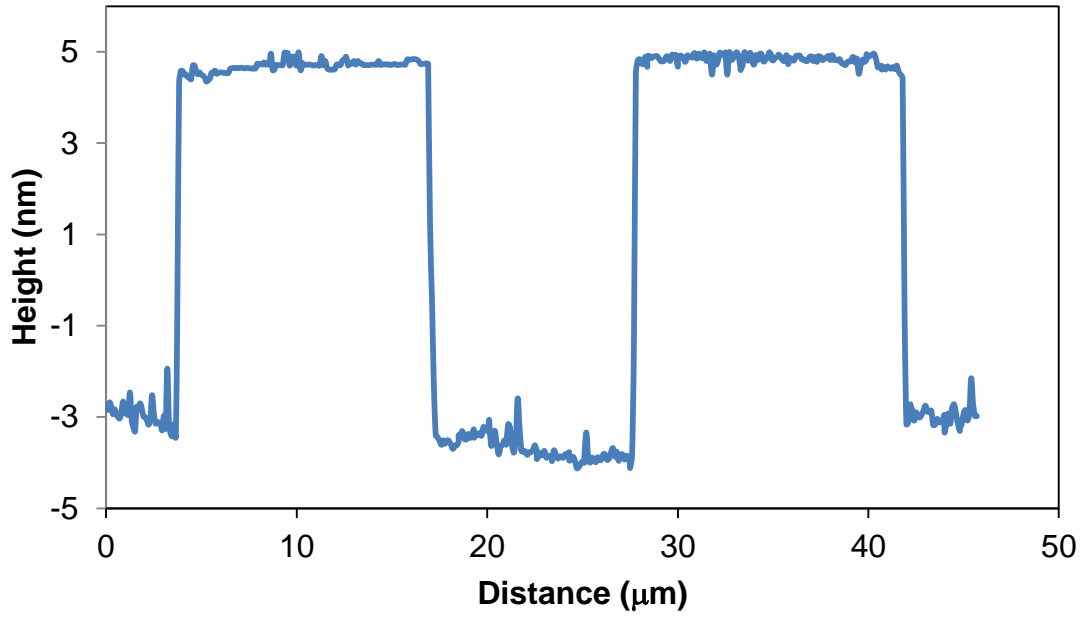
**Figure 7.2-1: High-resolution transmission electron microscopy (HR-TEM) image of a GeO<sub>x</sub> cladded-Ge quantum dot [55].**

These QDs have a partially positive charge on the cladding surface, which are attracted to the negative space charges in the depletion region, and so they readily self-assemble on *p*-type regions on a semiconductor wafer.

Figure 7.2-2 shows an atomic force microscopy (AFM) image of a silicon substrate with alternating lines of *p*-type and *n*-type doped regions [55]. Since the QDs gather themselves only over the *p*-type regions, these regions are thicker and show up in the lighter (yellow) shade in the figure. Figure 7.2-3 shows the height profile of these lines, indicating that there were two layers of QDs that self-assembled over the *p*-type regions.

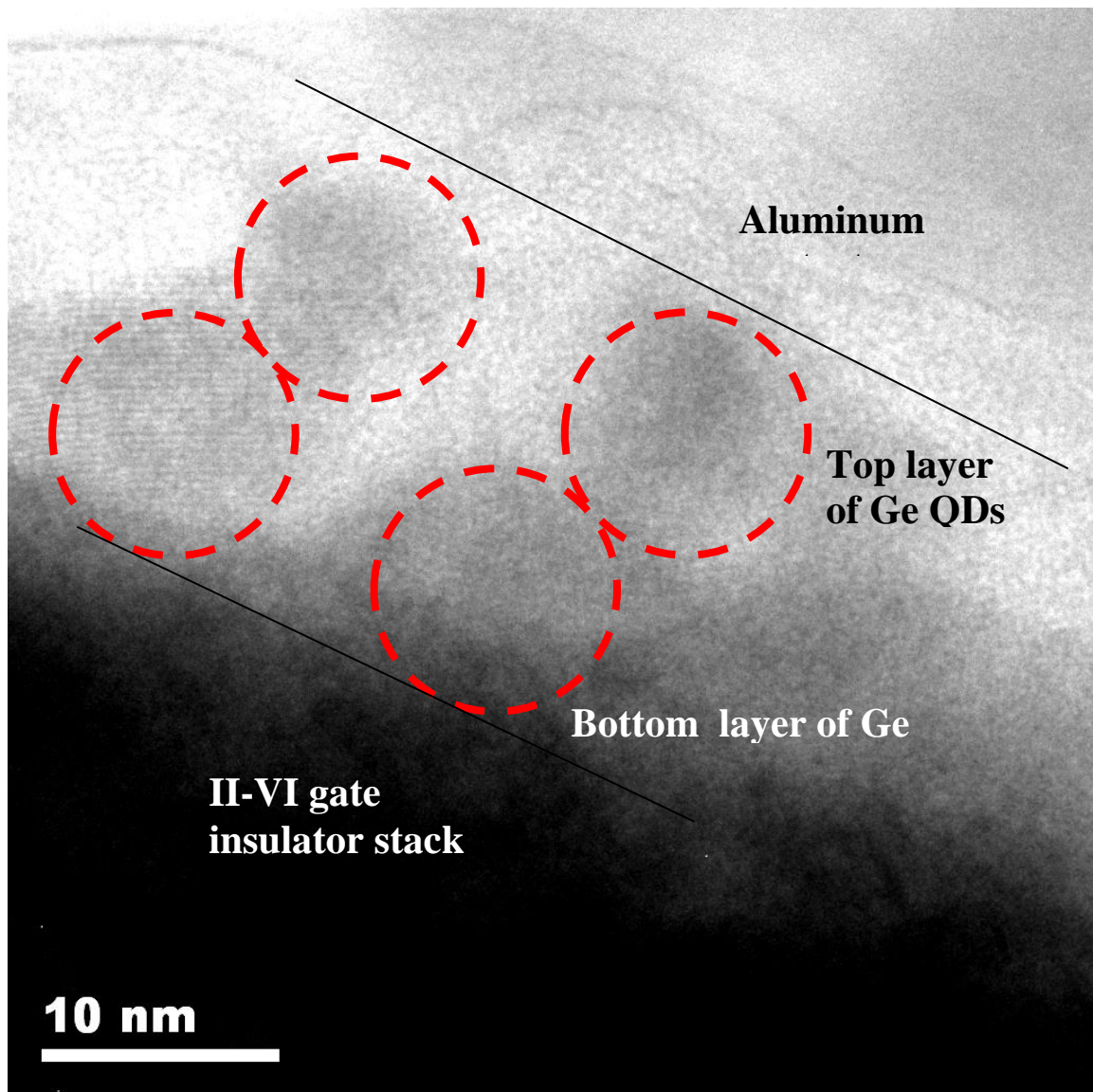


**Figure 7.2-2:** Atomic force microscope (AFM) image of GeO<sub>x</sub> cladded-Ge dots site-specifically self-assembled on *p*-type region of a Si wafer [55].



**Figure 7.2-3: Height profile of the lines in Figure 7.2-2, showing two layers of self-assembled GeO<sub>x</sub>-cladded Ge quantum dots [55].**

Figure 7.2-4 shows an HR-TEM image of the InGaAs QDG-FET (run #2001) at the gate region. In the figure, it is shown that two layers of cladded Ge QDs are situated over the gate insulator stack. Because of the site-specificity of the assembly of these QDs over only the *p*-type regions, this FET is self-aligned, and the fabrication process is CMOS compatible.



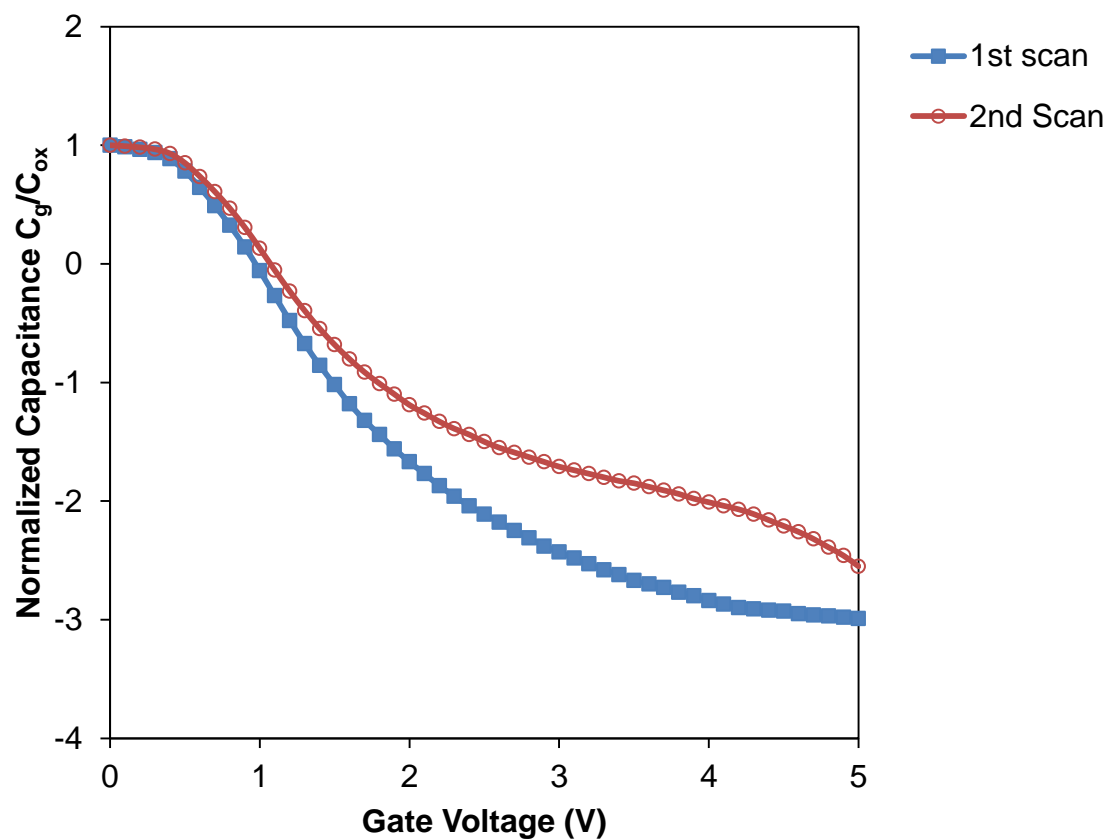
**Figure 7.2-4: HR-TEM image of the InGaAs QDG-FET at the gate region.**

## 8. Experimental Results and Discussion

### 8.1. InGaAs NVM MOS Capacitors

The fabricated InGaAs MOS capacitors were tested using an HP 4284A Precision LCR meter, and the data were recorded using a LabView program. For each capacitor, two capacitance measurements were performed consecutively over an applied gate voltage from 0 V to 5 V. Figure 8.1-1 shows the normalized capacitance-voltage (C-V) characteristics for one of the InGaAs MOS capacitors. The blue (with solid squares) curve shown is for the first capacitance scan, and the red curve (with open circles) gives the data from the second scan.

As it is shown in the figure, the two scans gave two different C-V characteristics. When the first scan was being performed, the applied voltage became more positive, which inverted the *p*-type InGaAs, and there was an accumulation of negative charges at the InGaAs surface. The negative charges were then being injected into, and subsequently stored in, the GeO<sub>x</sub>-cladded Ge QDs through the thin II-VI tunnel insulator layer by channel hot electron injection.



**Figure 8.1-1:** Capacitance-Voltage characteristics of the fabricated InGaAs MOS capacitor. The blue curve (with solid squares) and the red curve (with open circles) represent measurements from the first and the second scans respectively.



Due to the newly stored negative charges in the QDs,  $\Delta Q$  in Equation (4-2a) becomes negative, and  $\Delta V_{th}$  becomes positive. This coincides very well with the experimental data shown in Figure 8.1-1 with the second CV characteristic (red curve with open circles) shifting to the right.

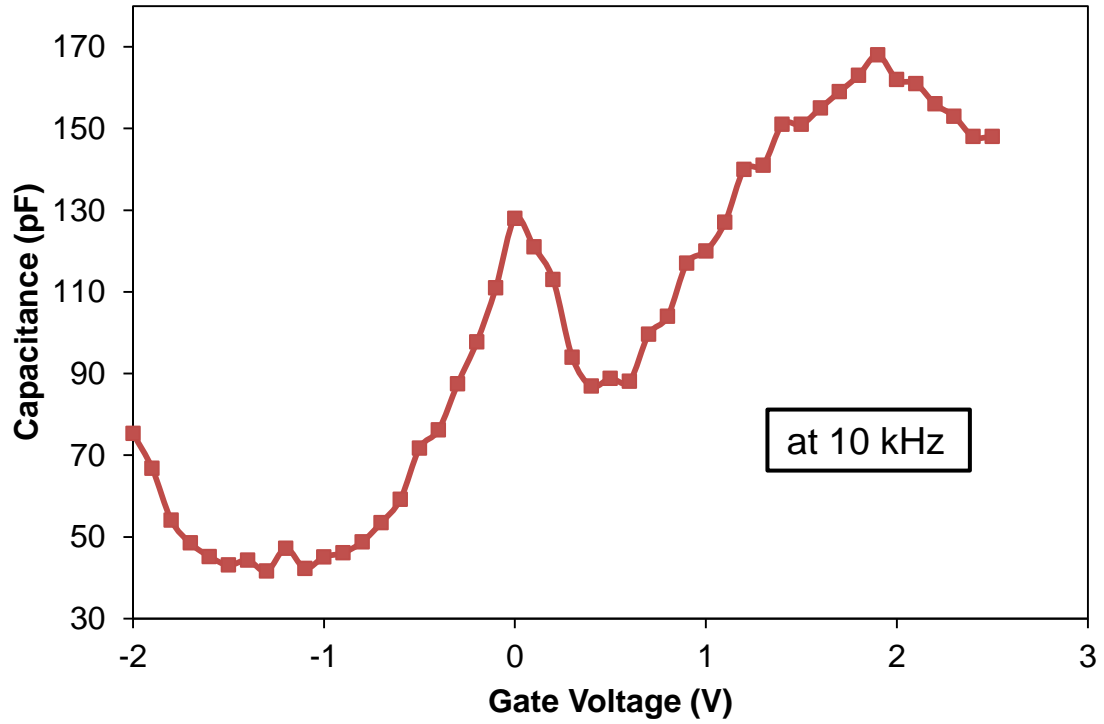
When a positive voltage was applied to the fabricated NVM MOS capacitors, the capacitor was undergoing the “WRITE” process of a non-volatile memory, with charges (or data) stored in the device (in this case, in the QDs). If a large negative voltage is to be applied to the same device, the stored negative charges will be forced out of the QDs, and the device will undergo the “ERASE” process of a non-volatile memory.

## ***8.2. Four-Well SWS MOS Capacitor***

Figure 8.2-1 shows the C-V characteristic of the four-well SWS MOS capacitor in the inversion regime at a frequency of 10 kHz [71]. There is a very characteristic peak appearing at  $V_G$  at about 0 V. This peak indicates the transition of electrons from the substrate to the bottom quantum well channel. As the electrons tunnel to the upper channels at higher gate voltages, the charge carriers become closer to the gate, and an increase in capacitance is expected.

Theoretically, there should be a corresponding peak for each quantum well channel in the MOS capacitor, but in this case, only one peak appeared. This can be

explained by the lack of resolution in the QW channels, and the subsequent effects of their charge transfers in the device.



**Figure 8.2-1: C-V characteristic of the 4-well SWS MOS capacitor at a frequency of 10 kHz. A characteristic peak appears at a gate voltage of about 0 V, indicating electrons tunneling from the substrate to the bottom QD channel.**

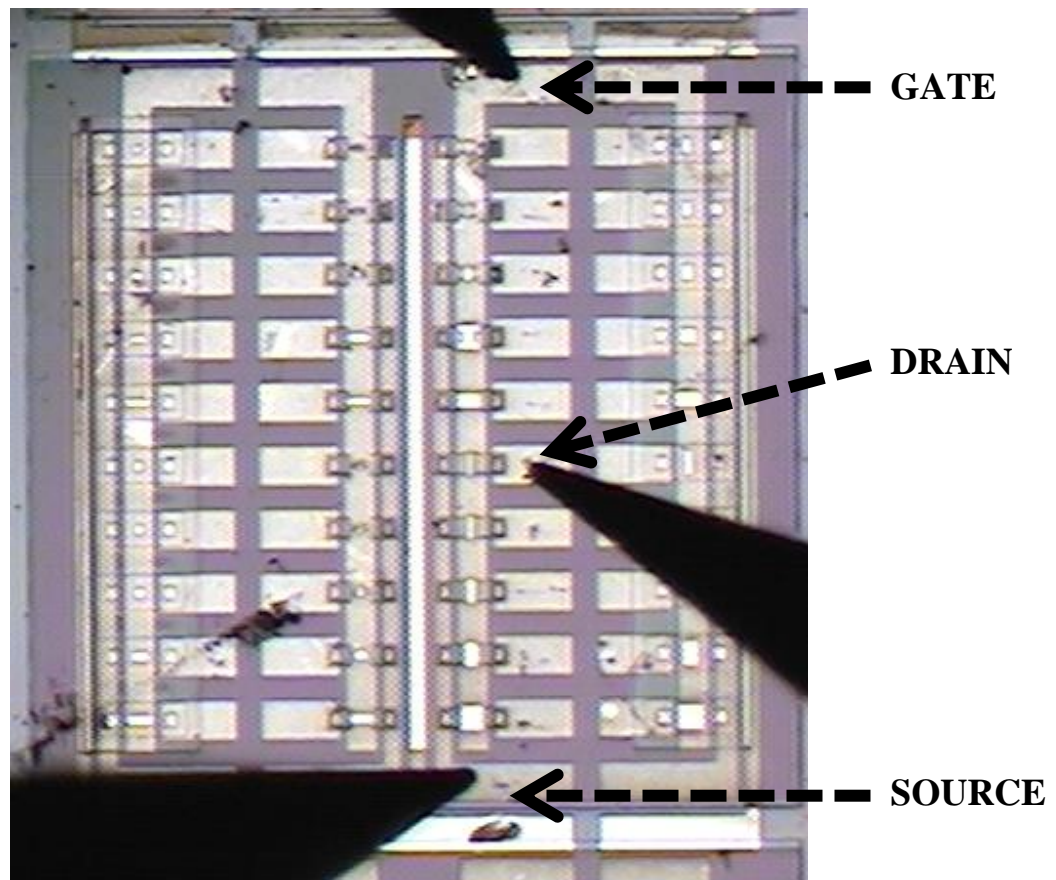
### 8.3. QDG-FET

#### 8.3.1. Output and Transfer Characteristics

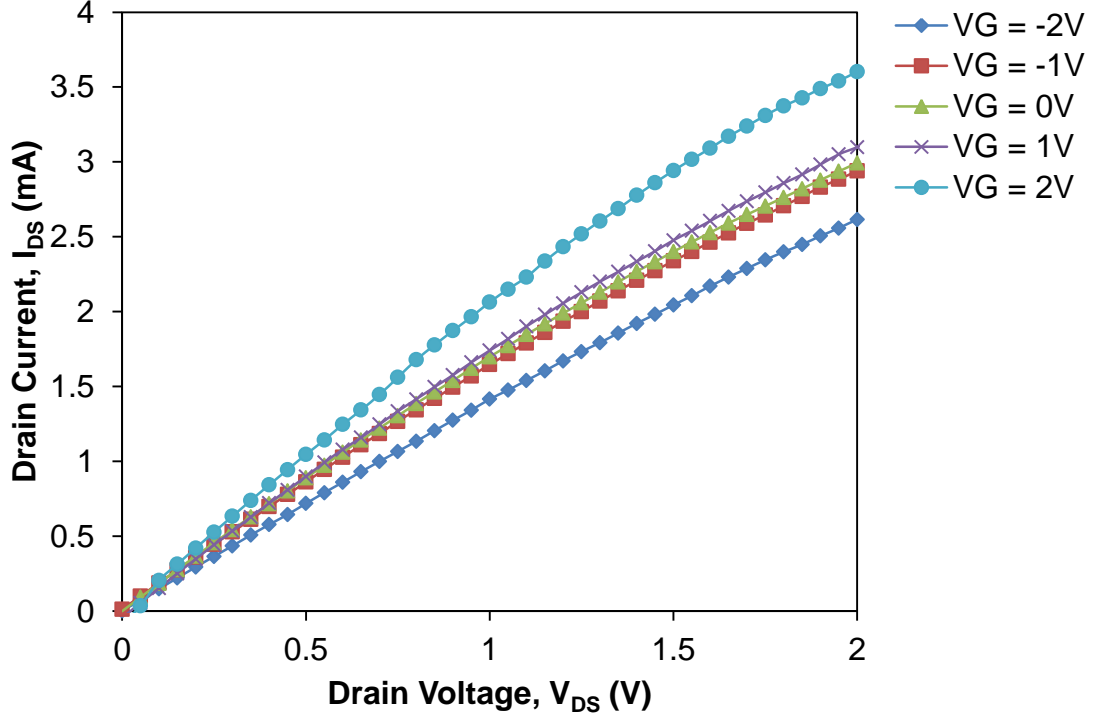
QDG-FETs were fabricated using bulk InGaAs (run #1973) and 3-well SWS substrate (run #2001) respectively. It should be noted that the QDG-FET using the 3-

well SWS substrate did not have individual drain contacts, and so no SWS effects were expected to show in the output or transfer characteristics of the device.

Figure 8.3.1-1 shows the fabricated QDG-FET (run #2001) showing the source, the drain and the gate of the device being tested. The testing was performed on an HP 4145B Semiconductor Parameter Analyzer.



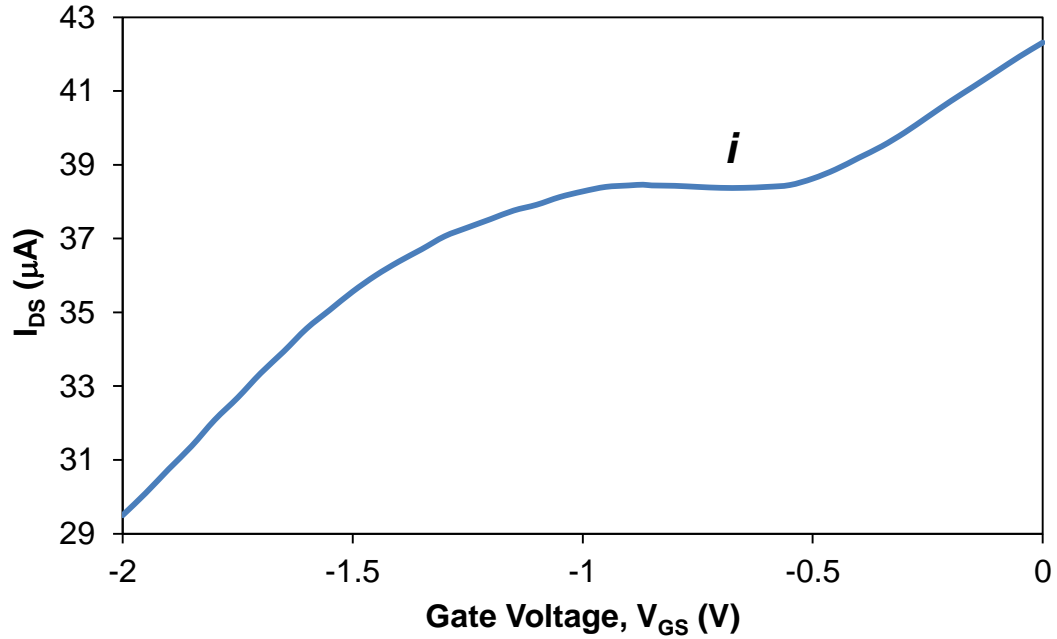
**Figure 8.3.1-1: An image of the fabricated QDG-FET (run #2001) under testing.**



**Figure 8.3.1-2:  $I_{DS}$ - $V_{DS}$  characteristic of the QDF-FET (run #2001) with a  $W/L$  ratio of  $50\mu\text{m}/10\mu\text{m}$ .**

Figure 8.3.1-2 shows the  $I_{DS}$ - $V_{DS}$  characteristic of the QDG-FET (run #2001) with  $W/L$  ratio of  $50\mu\text{m}/10\mu\text{m}$ . As  $V_{DS}$  increased,  $I_{DS}$  increased as expected with increasing  $V_{GS}$ . However, there was a bunching effect of the characteristics for  $V_{GS}$  between  $-1V$  and  $1V$ . The drain current,  $I_{DS}$ , only increased slightly over this range of  $V_{GS}$ . This corresponds to the intermediate “i” state of device according to Equations (3-4) and (3-5).

The same effect can also be observed from the  $I_{DS}$ - $V_{GS}$  characteristic of the QDG-FET (run #1973) shown in Figure 8.3.1-3.



**Figure 8.3.1-3:  $I_{DS}$ - $V_{GS}$  characteristic of a QDG-FET (run #1973).**

As shown in the  $I_{DS}$ - $V_{GS}$  characteristic, the  $I_{DS}$  is insensitive to  $V_{GS}$  when  $V_{GS}$  was between -1V and -0.5V, corresponding to the intermediate “i” state.

In both FETs,  $I_{DS}$  increases slowly with respect to  $V_{DS}$  for a specific range of  $V_{GS}$  values, giving rise to the intermediate “i” state of the three-state FET. As  $V_{GS}$  continues to increase and electrons continue to tunnel into the quantum dots layers, the quantum dots will eventually become full of electrons. The terms  $(V_{TH} + \Delta V_{TH})$  and  $C_{ox,eff}$  in Equation (3-4) will become constant once the QDs are filled with electrons. When this happens, the FET device will behave as a conventional FET and will eventually go into saturation at high  $V_{GS}$ , giving the ON state of the device.

### **8.3.2. High- $\kappa$ Materials and Gate Leakage**

Both a high  $\kappa$  value and a wide bandgap of a dielectric aid in reducing the leakage current in the device, but in high- $\kappa$  dielectric materials, it is observed that the dielectric constant is inversely proportional to the band gap [72-74]. A high  $\kappa$  value allows for a thicker dielectric gate material, which reduces the leakage current of the device. A wider band gap for the dielectric usually means a higher barrier at the semiconductor-dielectric interface, and this can reduce current leakage in the form of thermionic emission [74]. Because of this, a compromise has to be made in the perfect candidate for InGaAs FET devices.

It is observed that the leakage current in the QDG-FET devices was quite high, and is most likely due to the choice of II-VI gate dielectric for the FETs. As previously mentioned, the selection of ZnSe/ZnS/ZnMgS/ZnS/ZnSe did not match the lattice constant of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  perfectly, but it gave good gate control, high drain current and has a wider bandgap compared to other II-VI dielectric choices.

### **8.3.3. Source and Drain Regrowth**

In these QDG-FETs, the source and the drain regions were formed by regrowth of  $n^+$  InGaAs in the regions instead of ion implantation, which is common in silicon technology. Source access resistance requirement becomes more important in scaled devices because it could dramatically reduce  $I_{DS}$ . A low source access resistance requires

a very high source doping, however, this usually cannot be achieved in InGaAs devices due to the limited activation efficiency of conventional ion implantation [44]. Because of this, regrowth of high doping InGaAs in the source and the drain regions has been used to obtain low parasitic resistance and ohmic contacts [44, 75-76].

## 9. Modeling Simulation and Applications

### 9.1. Modeling Simulation Theory

The modeling simulation was made possible by solving one-dimensional Poisson's equation and Schrödinger equations self-consistently [59, 77].

Equation (9-1) shows the 1-D Poisson's equation for a heterostructure:

$$\nabla \cdot (\varepsilon \nabla \varphi) = q(n_{s2D} + n - N_D^+ + N_A^- - p) \quad (9-1)$$

where  $\varepsilon$  is the relative permittivity of the material,  $\varphi$  is the electrostatic potential,  $n_{s2D}$  is the two-dimensional electron concentration in the quantum wells,  $n$  and  $p$  are the three-dimensional electron and hole concentrations, and  $N_D^+$  and  $N_A^-$  are the ionized donor and acceptor concentrations. The quantity  $n_{s2D}$  can be determined once the wavefunctions and the bound states in the quantum well are calculated. The equation for determining  $n_{s2D}$  is given in Equation (9-2):

$$n_{s2D} = \sum \frac{4\pi k T m^*}{h^2} \Theta(E_F - E_n) \ln \left[ 1 + \exp \left( \frac{E_F - E_n}{k T} \right) \right] |\Psi_n|^2 \quad (9-2)$$

In the equation,  $k$  is the Boltzmann's constant,  $T$  is the temperature,  $m^*$  is the effective mass of electrons,  $h$  is the Planck's constant,  $\Theta$  is the Heaviside step function,  $E_F$  is the



Fermi level, and  $E_n$  and  $\psi_n$  are the energy level and the wavefunction of the quantum well. In order to determine  $E_n$  and  $\psi_n$  first, we can use the Schrödinger equation for confined electrons, presented in Equation (9-3), to solve for the quantities:

$$\frac{\hbar^2}{8\pi} \nabla \cdot \left( \frac{1}{m^*} \nabla \psi_n \right) + (E_n - V) \psi_n = 0 \quad (9-3)$$

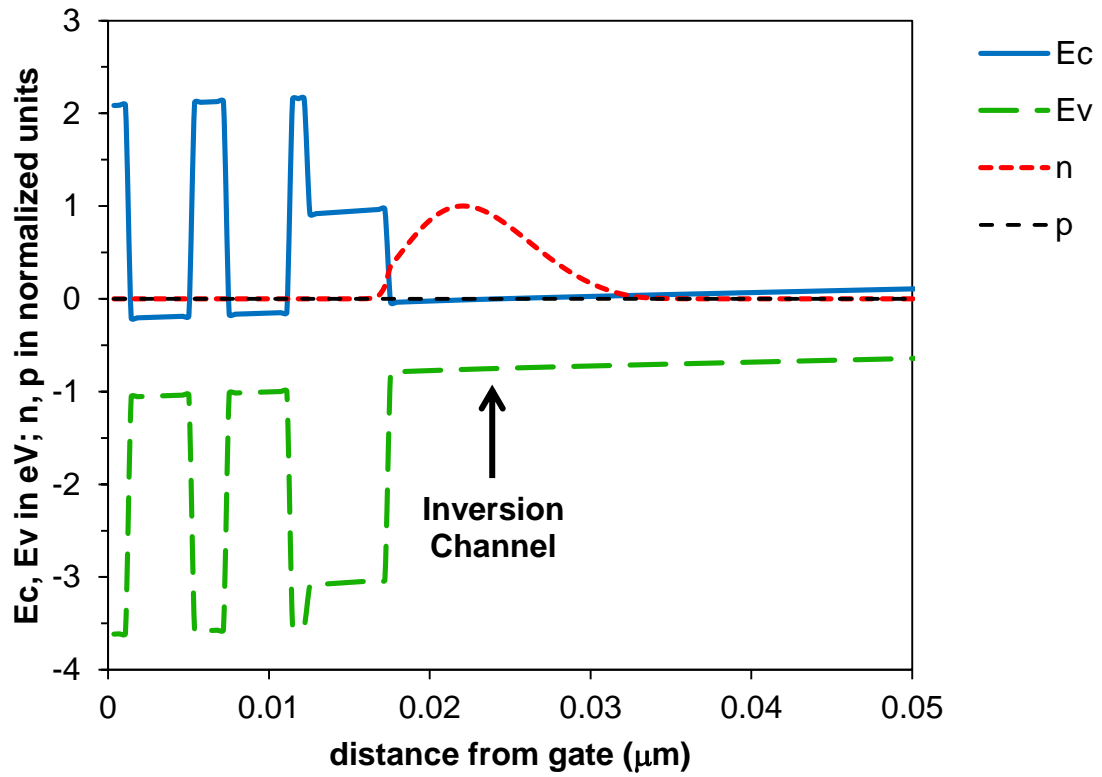
Finally  $V$  in Equation (9-3) is related to the electrostatic potential,  $\phi$ , in the Poisson's equation in Equation (9-1) by Equation (9-4):

$$V = q\phi \quad (9-4)$$

In all the simulation results, the  $V_{GS}$  ranges are different from the actual voltage range obtained experimentally. This is largely due to the differences in work functions and interface traps that are present in the fabricated devices.

## **9.2. Bulk-InGaAs QDG-FET**

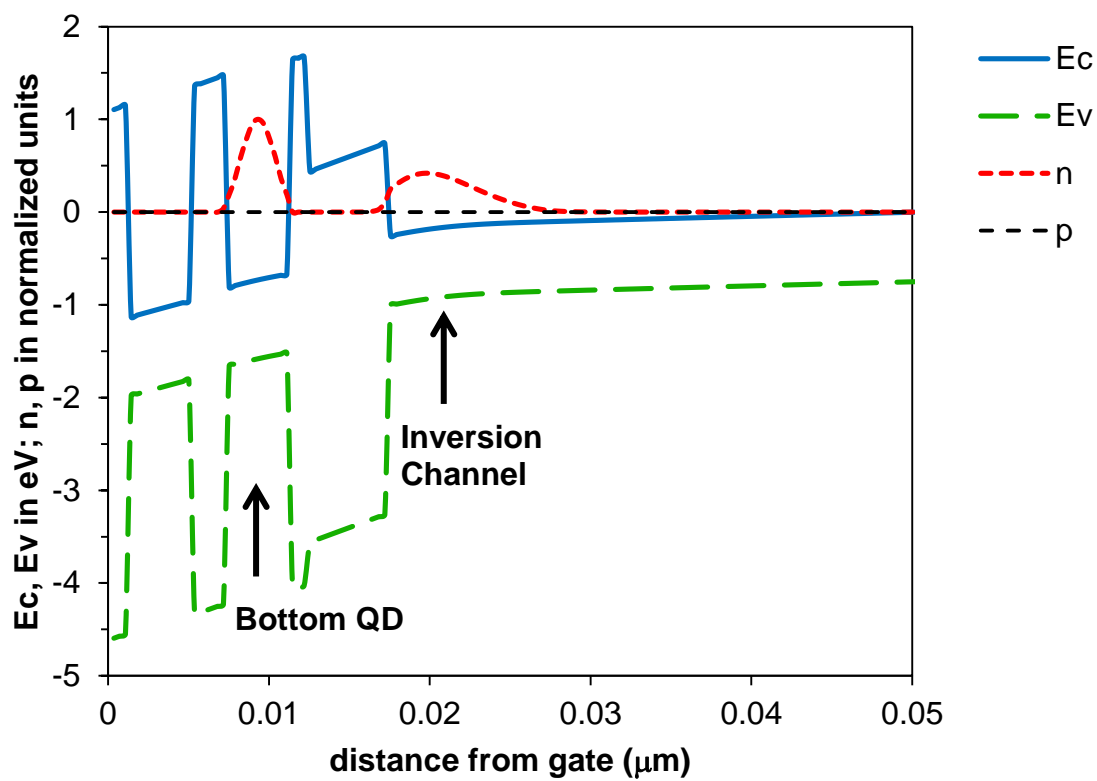
The QDG-FET using bulk InGaAs shown in Figure 6-9.11 was simulated to understand how electrons tunnel from the inversion channel to the quantum dots. Figure 9.2-1 presents the band diagram of the QDG-FET, showing electrons in the inversion channel of the device when  $V_G$  was at -3.5V.



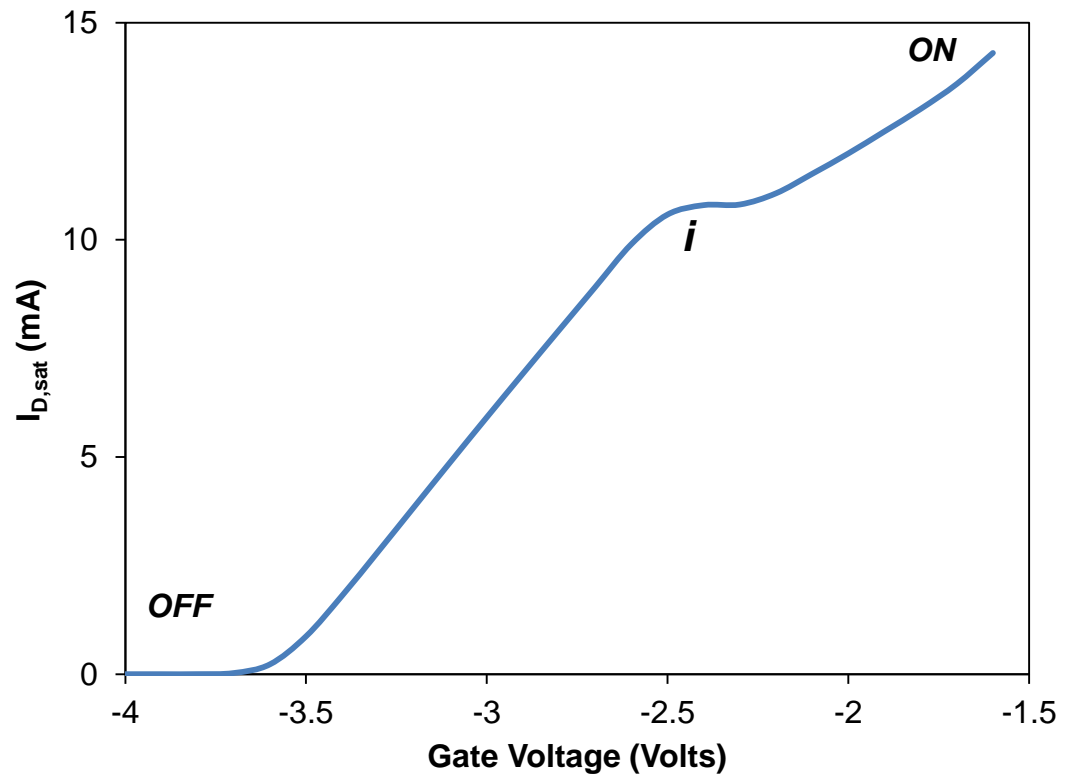
**Figure 9.2-1: Band diagram of an InGaAs QDG-FET with electrons accumulating at the inversion channel when  $V_G$  was -3.5V.**

As  $V_G$  continued to increase, more carriers were found at the inversion channel, and when  $V_G$  reached -2.5V, the electrons started to tunnel into the bottom QD layer through the gate dielectric, as shown in Figure 9.2-2.

As previously mentioned, when electrons start to tunnel into the QD layers, the quantities  $\Delta Q$  and  $\Delta V_{TH}$  will change, but the increase in  $\Delta V_{TH}$  is negated by the increase in  $V_{GS}$ , leading to the insensitivity of  $I_{DS}$  for that range of  $V_{GS}$ . As shown in Figure 9.2-2, the electrons started to enter the QD layers at  $V_{GS} = -2.5V$ . Figure 9.2-3 presents the  $I_{DS}$ - $V_{GS}$  relationship, showing the intermediate “i” state of the QDG-FET. This simulation also shows the “i” state commencing at  $V_{GS} = -2.5V$ , showing that the intermediate “i” state is the result of charge carriers entering the QDs. This  $I_{DS}$ - $V_{GS}$  simulation result matches closely with our experimental result shown in Figure 8.3.1-3.



**Figure 9.2-2:** When  $V_G$  reached -2.5V, electrons started to tunnel from the inversion channel into the bottom QD layer.



**Figure 9.2-3:**  $I_{DS}$ -  $V_{GS}$  relationship of the QDG-FET showing the intermediate “i” state starting at  $V_{GS} = -2.5$  V, coinciding with the charge carriers entering the QDs.

### 9.3. InGaAs NVM-FET

Simulation was also done on an InGaAs NVM-FET, which has a cross-sectional structure shown in Figure 9.3-1. This structure builds on the results of the InGaAs NVM MOS capacitors and the InGaAs QDG-FET.

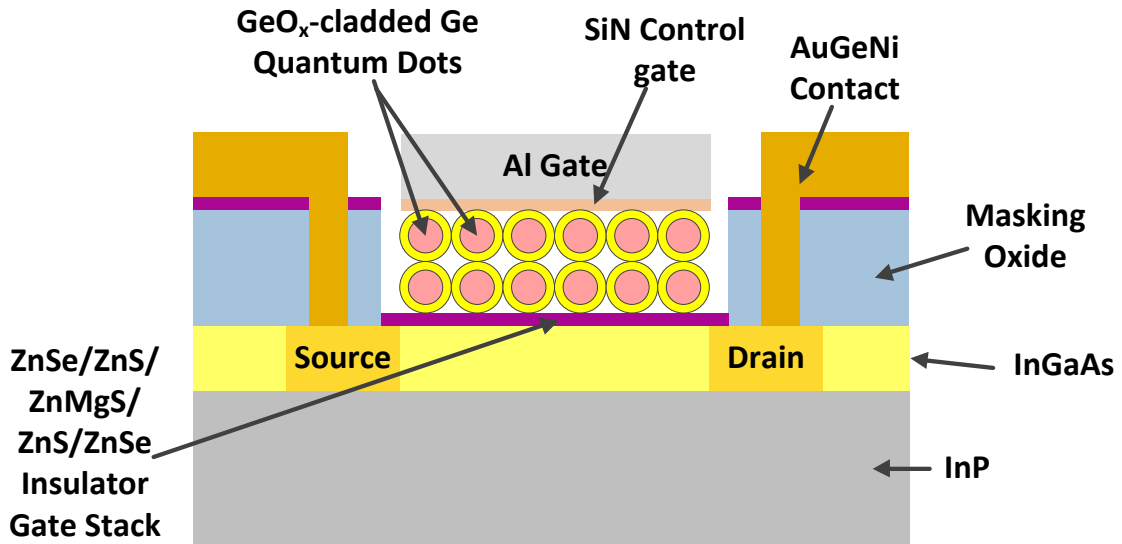
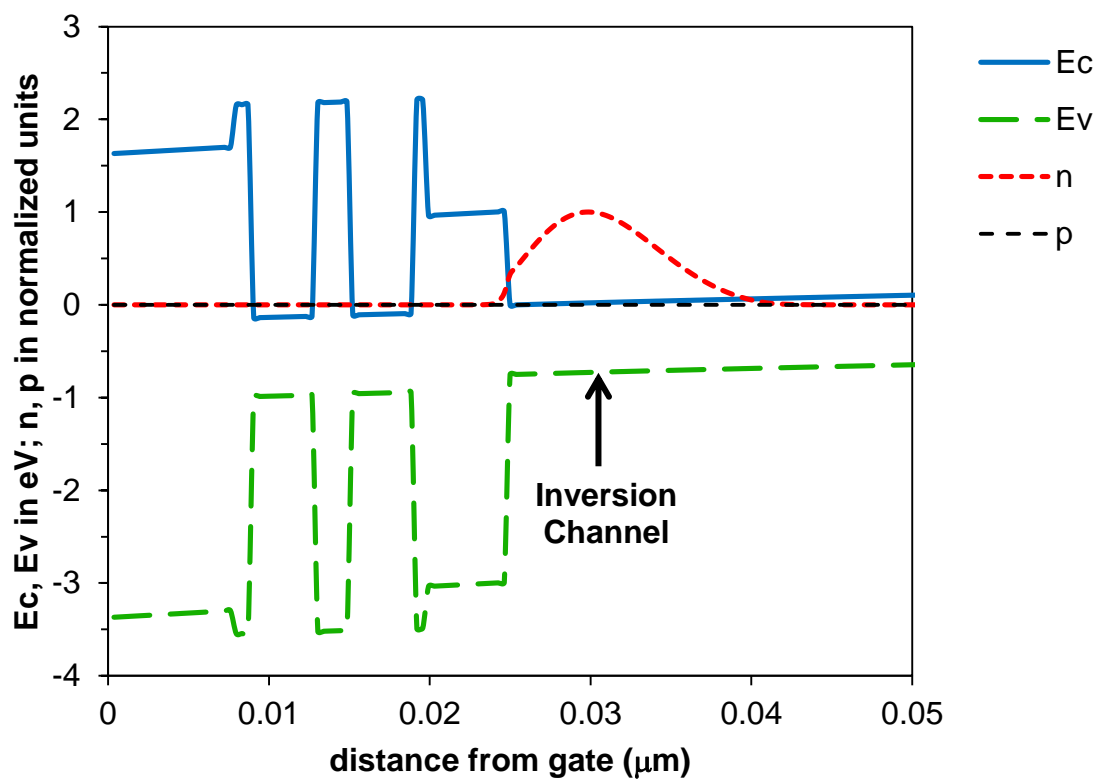
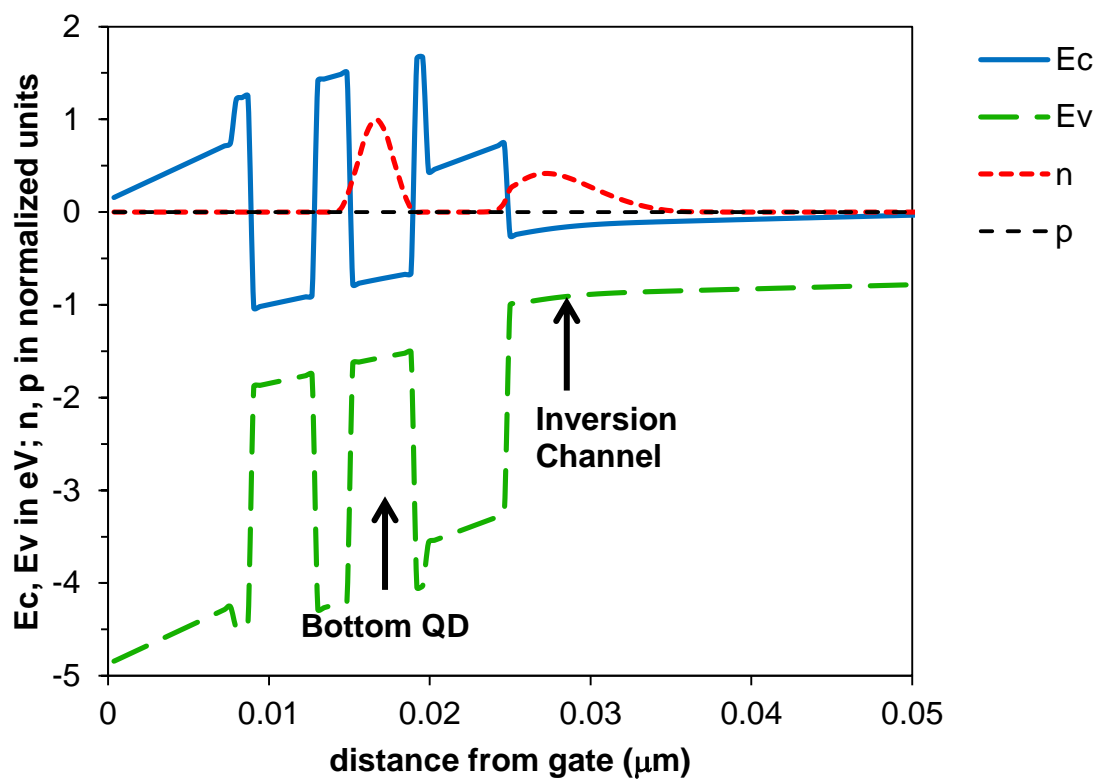


Figure 9.3-1: Cross-sectional structure of an InGaAs NVM FET

Figure 9.3-2 shows the electron wavefunction in the inversion channel of the FET at  $V_{GS} = -3.4V$ , and when  $V_{GS}$  was increased to  $-1.9V$ , electrons started to tunnel into the bottom QD layer (Figure 9.3-3). Due to the presence of the SiN control gate, high  $V_{GS}$  values were required for the electrons to tunnel into the QDs, when compared to the InGaAs QDG-FET.



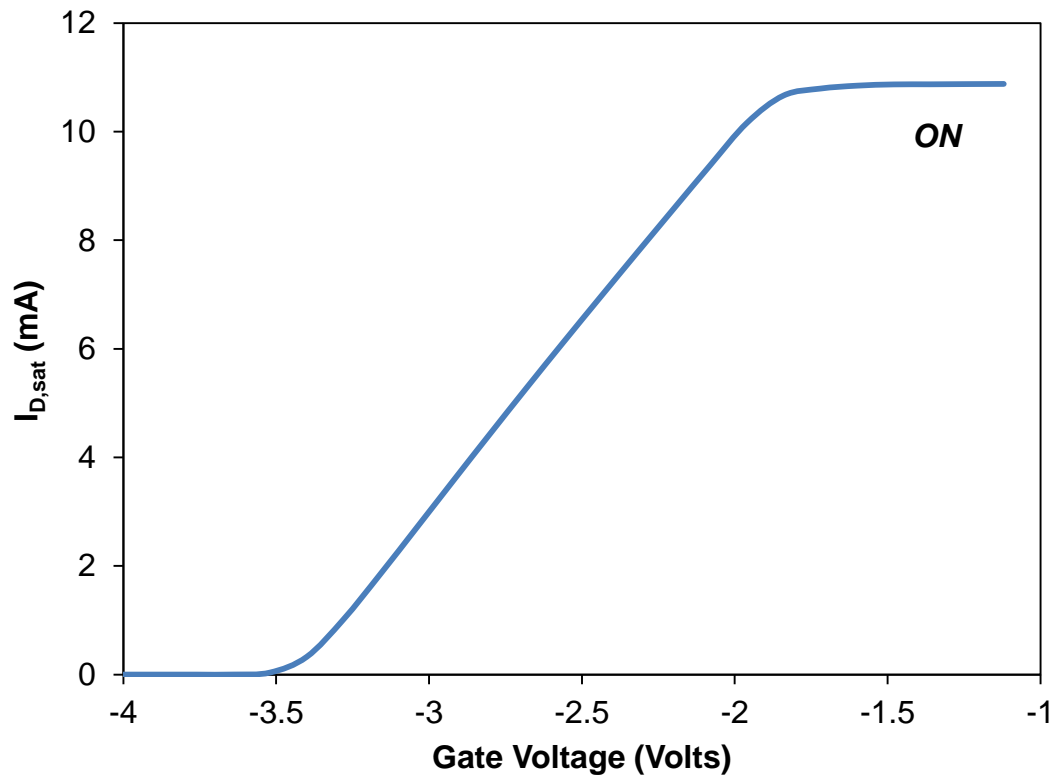
**Figure 9.3-2: Band diagram of an InGaAs NVM-FET with electrons accumulating at the inversion channel when  $V_G$  was  $-3.4V$**



**Figure 9.3-3:** When  $V_G$  reached  $-1.9\text{V}$ , electrons started to tunnel from the inversion channel into the bottom QD layer.



Figure 9.3-4 shows the  $I_{DS}$ -  $V_{GS}$  relationship of the InGaAs NVM-FET. Unlike the QDG-FET, the NVM-FET does not show any intermediate “i” state in its transfer characteristic. The inclusion of the SiN control gate prevents the electrons from escaping from the quantum dots to the gate electrode, and the FET eventually goes into saturation.

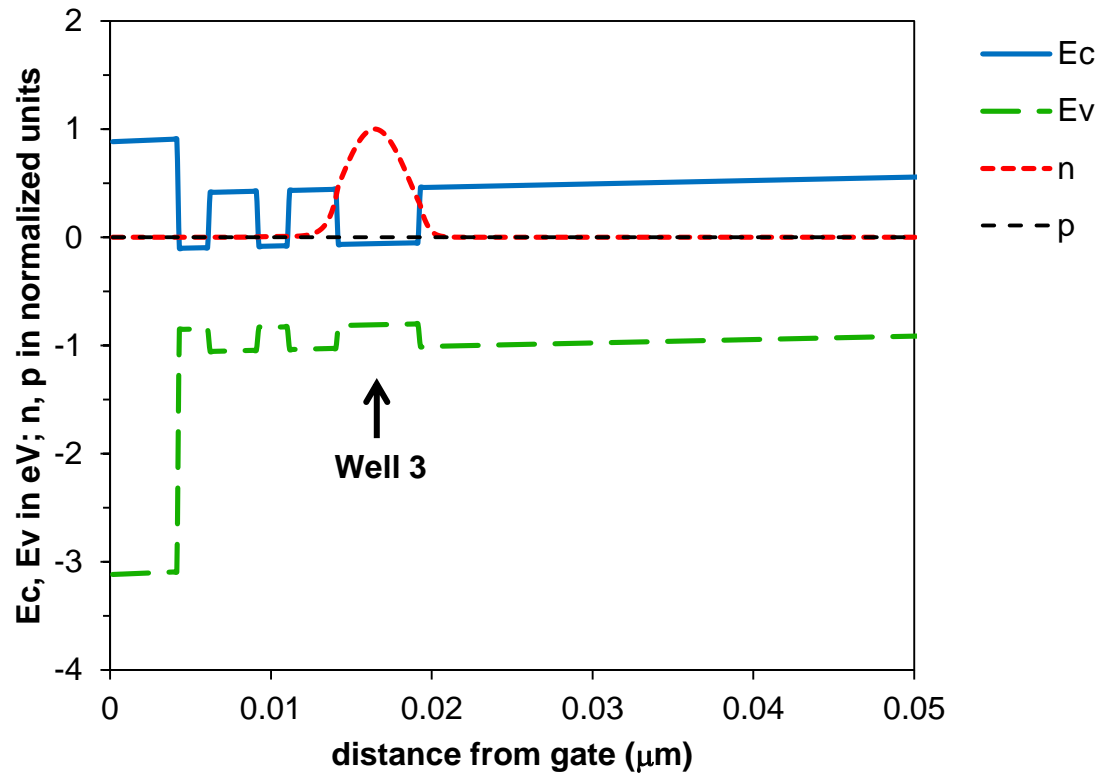


**Figure 9.3-4:**  $I_{DS}$ -  $V_{GS}$  relationship of the InGaAs NVM-FET. No intermediate “i” state was observed in this device.

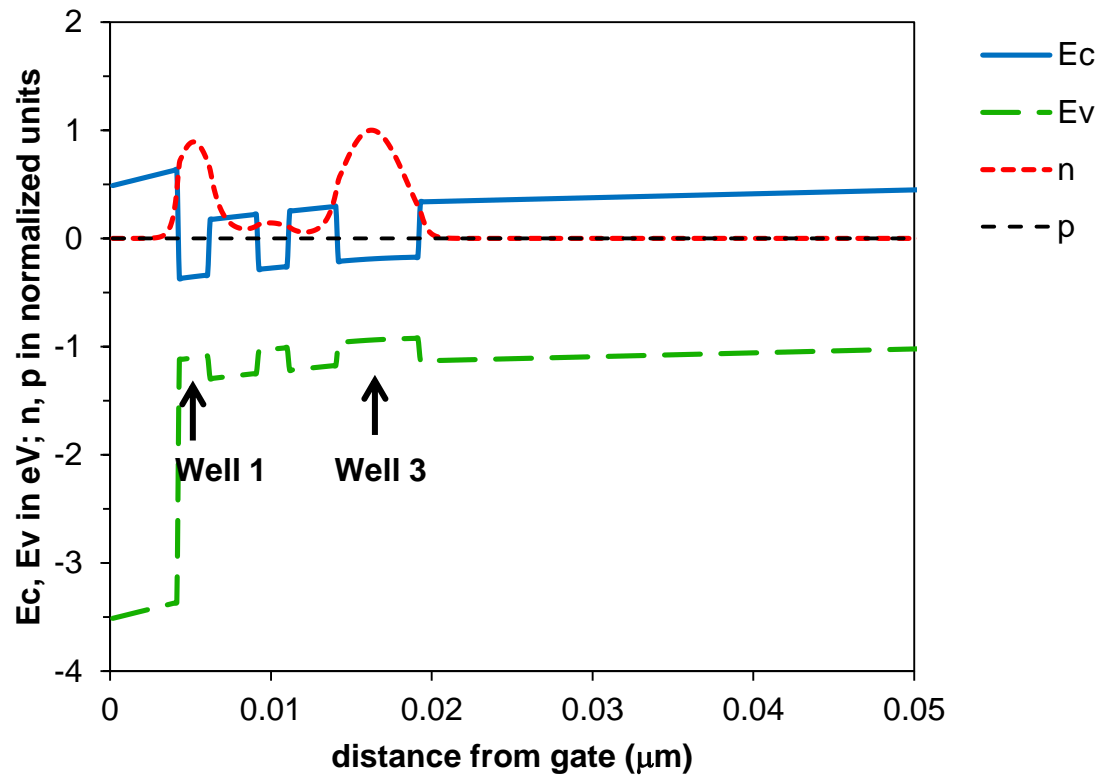
#### **9.4. SWS QDG-FET**

Simulations were performed on the 3-well SWS substrate presented in Table 6.10-1. First of all, to show the SWS phenomenon alone, the modeling was done with no QDs in the gate region. Figure 9.4-1 shows the electrons appearing in the bottommost well, Well 3, of the SWS FET at  $V_{GS} = -3.2V$ . As expected, the electrons would tunnel towards the gate with increasing  $V_{GS}$ . As  $V_{GS}$  reached  $-2.8V$ , electrons were found in both the uppermost Well 1 and the bottommost Well 3, as shown in Figure 9.4-2.

When comparing Figure 9.4-2 with the two-well SWS simulation results shown in Figure 5-3, which also shows electrons in two wells, we can see that the electron confinement in a three-well substrate is better than that in the two-well situation. Because of this resolution problem, it is better to use a three-well SWS device to obtain four distinct states.



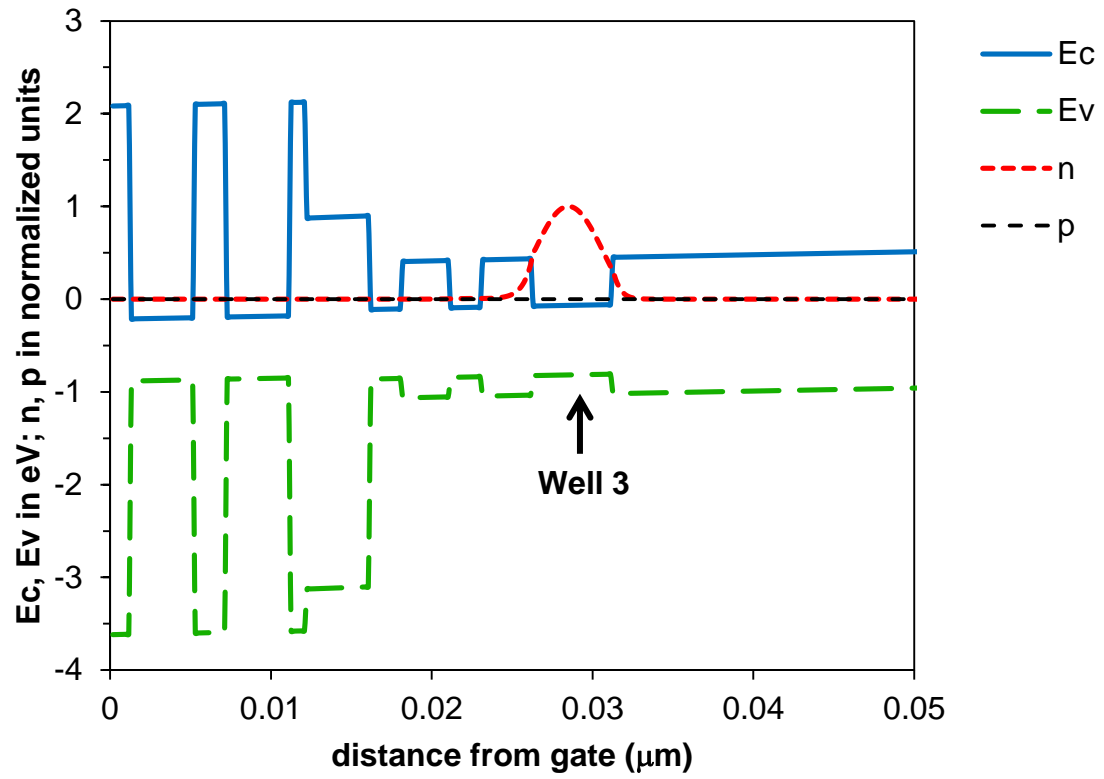
**Figure 9.4-1:** In a three-well SWS FET, electrons appeared in the bottommost Well 3 when  $V_{GS}$  was -3.2V.



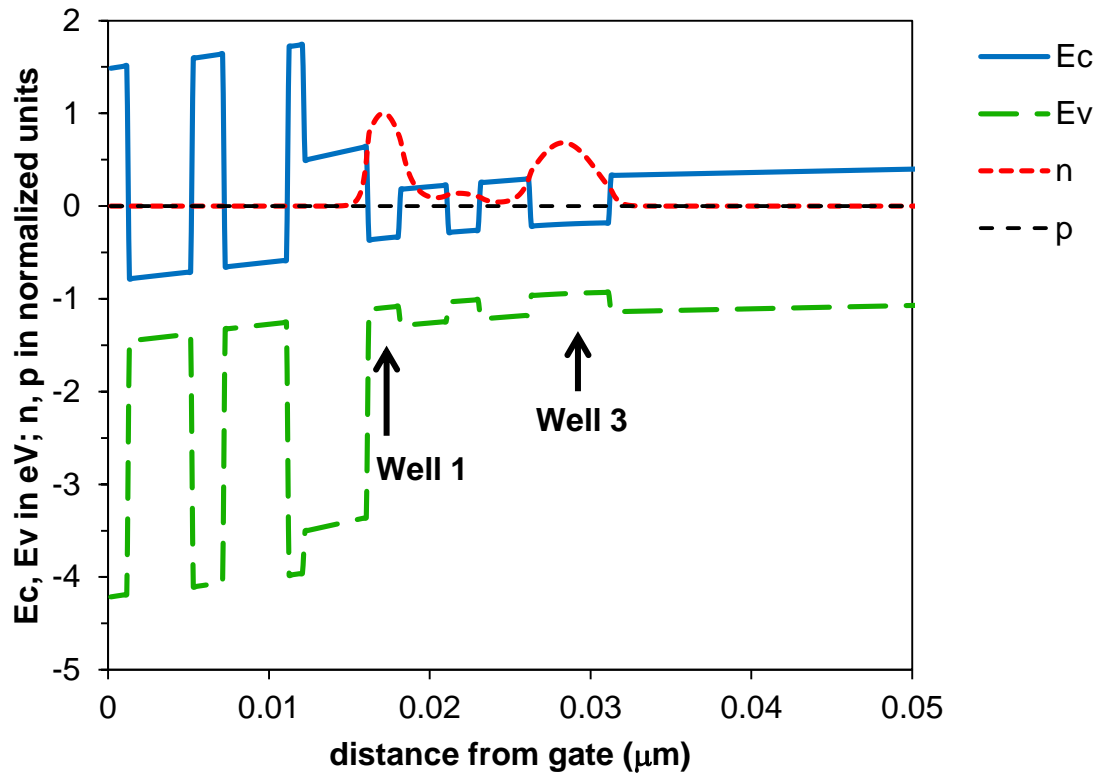
**Figure 9.4-2:** When  $V_{GS}$  is -2.8V, electrons appeared in both the bottommost Well 3 and the uppermost Well 1.

When QDs are incorporated in the SWS FET, it is possible to obtain another output state as previously explained. The transition of electrons in a SWS QDG-FET is as follows. When  $V_{GS}$  was -3.5V, the electrons appeared in the bottommost Well 3 (Figure 9.4-3), and at a  $V_{GS}$  of -2.9V, electrons appear in both Well 1 and Well 3 (Figure 9.4-4). It should be noted that the addition of QDs cause the critical  $V_{GS}$  values to decrease slightly.

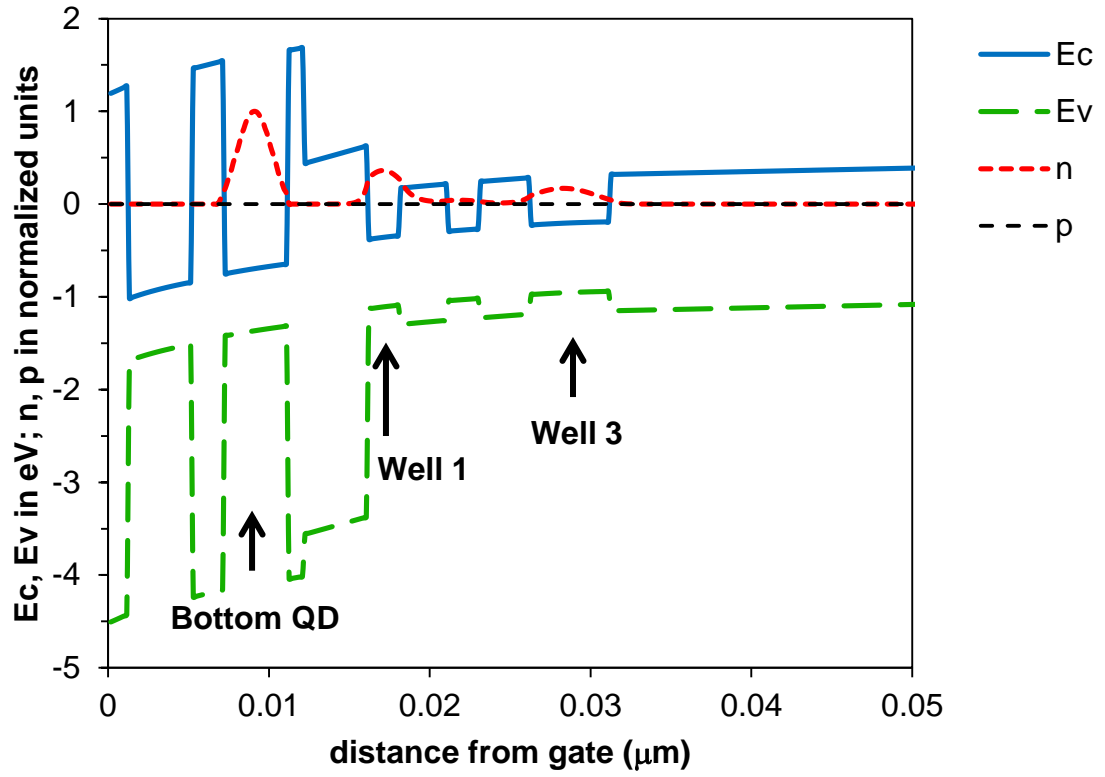
The tunneling of electrons from the SWS channels into the QDs started when  $V_{GS}$  reached -2.6V (Figure 9.4-5). The electron densities in the quantum wells decreased as electrons migrated into the QDs. At  $V_{GS} = -2.5V$ , electrons could no longer be found in Well 3, but they remained residing in the SWS channel Well 1 and the QDs above the gate region (Figure 9.4-6).



**Figure 9.4-3:** In a three-well SWS QDG-FET, electrons started to appear in the bottommost Well 3 when  $V_{GS}$  was -3.5V.

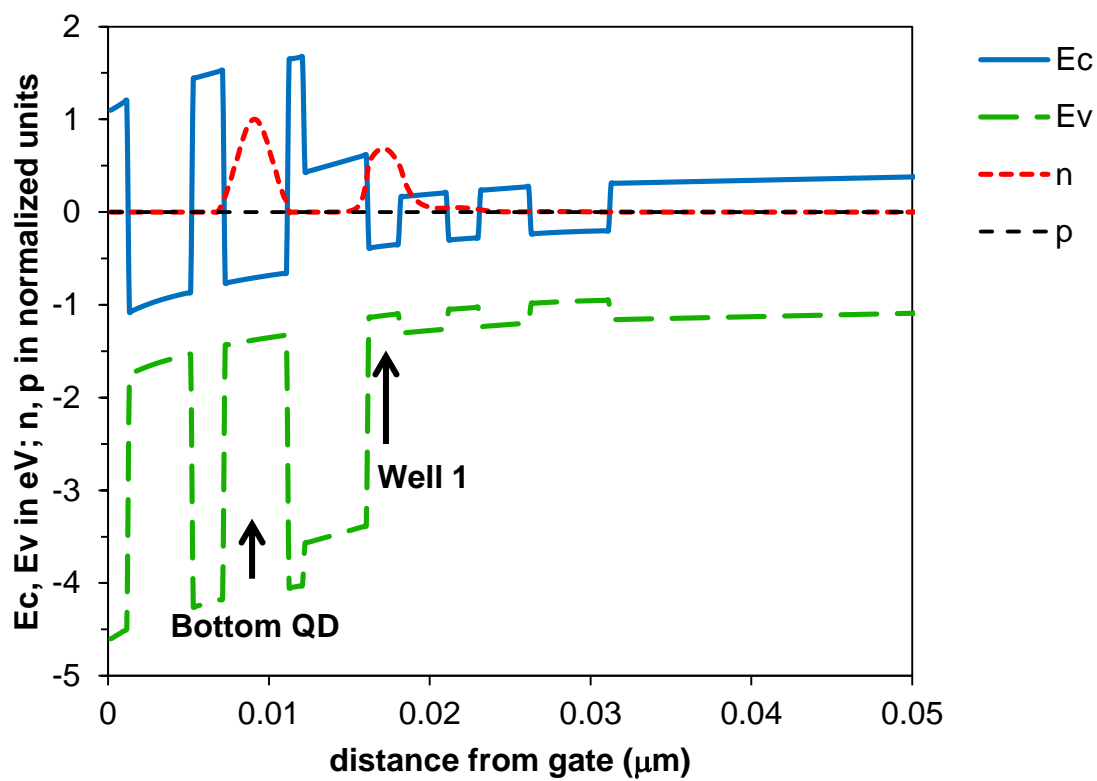


**Figure 9.4-4:** When  $V_{GS}$  was at -2.9V, electrons appeared in both the bottommost Well 3 and the uppermost Well 1 of the SWS QDG-FET.



**Figure 9.4-5:** The tunneling of electrons from the quantum well channels into the QDs started when  $V_{GS}$  reached -2.6V. At the same time, the electron densities in the wells decreased.





**Figure 9.4-6:** When  $V_{GS}$  was -2.5V, electrons only resided in the SWS channel Well 1 and the QDs above the gate region.

### ***9.5. Application in Multi-value Logic***

Both QDG-FETs and SWS-FETs are capable of generating multiple output states. This unique property can be harnessed to create multi-bit logic. Various researchers have already presented circuits using QDF-FETs and SWS-FETs.

Multi-bit logic applications using QDG-FETs include inverters [78], ternary logic gates [79], and six-bit analog-to-digital converters and digital-to-analog converters [80].

SWS-FETs have been used in a variety of logic circuit designs such as a two-bit SRAM using two four-channel SWS-FET [81], a three-bit analog-to-digital converter using a three-well SWS-FET [82], and a unipolar inverter using a two-well SWS-FET and an n-channel MOSFET [83].

Gogna et al. has presented logic cells (AND gate, OR gate and NOT gate), a full adder, a quaternary latch and SRAM using SWS-FET [84-85]. A comparison of device counts for these logic applications using CMOS FETs and SWS-FET was made [84]. Using SWS-FETs, the reduction in device counts for most of the described applications was 75%, and the device count for a full adder went from 80 for CMOS to 11 for SWS-FET. The decrease in device counts using SWS-FETs will reduce chip footprint and power consumption of the circuit [85].

## 10. A Look into the Near Future

InGaAs has shown good performance in n-channel MOSFETs. However, in order to make InGaAs a more appealing option to replace silicon CMOS technology, development of p-channel MOSFETs is needed. The sad news is that the hole mobility for InGaAs is not high enough, and so it would not be a viable choice. This led researchers into looking into other materials for possible p-channel MOSFET development. Currently, compressively-strained Ge has shown to have a higher hole mobility [19], and would be an ideal partner for InGaAs in the future CMOS development.

Intel has started working on InGaAs FET in the past few years, and their integration of InGaAs on Si shows the industry's determination to move in the direction of III-V CMOS. To make InGaAs compatible with current Si CMOS technology, Si substrate has been used as a handler for InGaAs epilayer, with a GaAs/graded-InAlAs buffer layer in between as an interfacial layer [37]. In addition to retrofitting InGaAs to the current Si CMOS technology, another motivation to deposit InGaAs on Si substrate is to add robustness to InGaAs materials. Currently most InGaAs epilayers are deposited on brittle InP substrate, and because of the fragile InP substrate, large InGaAs wafers are not readily available or feasible. With the development of InGaAs on Si, there is no need to develop methods to obtain large InGaAs wafers [42, 44].

As mentioned before, a gate dielectric material that is lattice-matched to the InGaAs channel is desired. Instead of finding a material that is perfectly lattice-matched to InGaAs, researchers have started to turn to metamorphic InGaAs material [86-91]. Metamorphic InGaAs is compositionally graded so that the lattice constant changes throughout the metamorphic layers. The lattice mismatch in the graded layers is relaxed by the introduction of misfit dislocations in the layers [87]. Using metamorphic InGaAs materials will allow a wider selection of II-VI dielectric materials, giving more flexibility in the design of the devices.

## 11. Conclusion and Future Work

This dissertation presented the fabrication processes for a number of InGaAs-based MOS devices utilizing II-VI materials as the gate dielectric material, along with the addition of  $\text{GeO}_x$ -cladded Ge quantum dots as charge storage centers to introduce three-state capability in the devices. The addition of spatial wavefunction switching quantum well channels in the substrate further increases the opportunity for multi-bit operations in SWS-FETs. Modeling simulations also show the multi-state operations of these devices. Output and transfer characteristics of the fabricated QDG-FETs show that the selection of II-VI gate dielectric stack is in fact an acceptable candidate for InGaAs-based MOS devices.

To improve on this project, a more suitable II-VI gate dielectric material should be selected, with a high  $\kappa$  value and a wide bandgap, and this can be aided by using metamorphic InGaAs substrates to maximize the selections. To show that II-VI gate dielectric material can really stand up against the more popular  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$ , devices using all three types of gate dielectric should be fabricated and compared.

To further extend the non-volatile memory performance of InGaAs MOS capacitors, the fabrication of an InGaAs NVM FET is the next logical step. Figure 9.3-1 shows the cross-sectional structure of such a device.

Finally, to truly harness the SWS ability of an SWS-FET, separate drains must be made to the individual quantum well channels. This fabrication process will require precise etching of the quantum well channels in the nanometer range. Wet chemical etching usually has too many variables, and so to get accurate etching profiles down to the nanometer range, reactive ion etching of InGaAs/InAlAs should be used instead.

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